INSTRUCTION MANUAL

DOVETRON MPC-1000CR REGENERATIVE

RTTY TERMINAL UNIT

MULTIPATH CORRECTION

SIGNAL REGENERATION - SPEED CONVERSION

DIGITAL AUTOSTART

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MPC-1000CR.500 and up.

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MPC-1000CR REGENERATIVE RTTY TERMINAL UNIT

DESCRIPTION

The DOVETRON MPC-1000CR is a Signal Regenerating, Speed-Converting, In-Band Diversity RTTY Terminal Unit that features Multipath Correction, a high level keyer and an internal loop supply.

The Polar data Inputs and Outputs are available in two low-level configurations (EIA and MIL).

The input Mark and Space channels are continuously variable from 1200 Hz to 3100 Hz. Other frequency ranges are available.

The Regenerator Section consists of a Dovetron TSR-200D, which may be operator-programmed for 5, 6, 7 or 8 level codes, with 1.0 or 1.5 CU structure. Parity is also selectable.

A front panel Signal Speed switch selects 45.45, 50.0, 56.88, 74.2 (75.0) or 110 Baud communication baud rates.

The Loop output baud rate may be programmed internally to a fixed speed, permitting up-down Speed Conversion in the Half-Duplex mode.

The MPC-1000CR provides nominal loop currents of 20, 40 or 60 milliamperes. A rear panel Loop Adjustment potentiometer is provided to set loop currents precisely.

Programming instructions of all switches are etched right on the printed circuit boards.

The audio input is transformer coupled and has a nominal 600 impedance.

The Mark and Space tone frequencies are phase-continuous and continuously adjustable from the rear panel over a range of 1200 Hz to 3100 Hz. Nominal output is \emptyset dbm.

Rear panel connectors provide Dual-Diversity operation of two or more Dovetron terminal units without the need for an external comparator unit.

Additional connectors permit interconnecting a Dovetron SCR-1000 Selective Calling-Recognition unit.

Three remote control lines are provided, which are part of an isolated deck on the front panel ON-STANDBY switch. On some units, this switch is labeled REC-SEND. When supplied with Spanish front panels, this switch is labeled: REC-TRANS.

Two rear panel fuses are provided for the Power and Loop power circuits.

A Third fuse is mounted under the main board and protects the CRT's high voltage power supply.

This manual is complete when the following prints are attached:

75100: Assembly Main Board, E-Series.

75103: Schematic Main Board, E.Series.

75164: Schematic TSR-200D Regenerator.

75171: Assembly TSR-200D Regenerator.

ORGANIZATION

The MPC-1000CR consists of two basic, easy to identify sections:

- 1) Main Board A75100-E.
- 2) TSR-200D Signal Regenerator Assembly.

Each Section consists of a separate printed circuit board and associated wiring and external components.

MAIN BOARD A75100-E

The main board assembly is the same as that used in the MPC-1000C RTTY Terminal Unit.

It is thoroughly discussed and detailed in the rear section of this manual, pages 1 thru 58.

TSR-200D SIGNAL REGENERATOR ASSEMBLY

The TSR-200D assembly consists of four sections:

- 1) Signal Regenerator (UART).
- 2) Dual Crystal-Controlled Clock.
- 3) Bilateral Steering Circuits.
- 4) Character Recognition-Speed Determination Digital Autostart circuit.

SIGNAL REGENERATOR

The Signal Regenerator section regenerates all signals passing thru it to less than 0.5% bias distortion, significantly reducing the error rate of the RTTY communication system.

When used in Half-Duplex operation, both the incoming and outgoing signals are processed thru the Regenerator. Since the TSR-200D is a half-duplex device, it must be switched between Transmit and Receive by the front panel ON(Receive)-STANDBY (Send) switch or by the rear panel remote LOCK line.

Signal Regeneration is accomplished by an Intersil IM6402CPL CMOS 40-pin UART (Universal Asynchronous Receiver/Transmitter) located at Z2. This UART is a dual chip. One half is a Serial/parallel converter and the other half is a parallel/ serial converter. Although both sides of this UART are programmed simultaneously by the UART Program Switch S3, they have separate clock input ports. When a single clock is used at both ports, straightthru regeneration is achieved, i.e., no change in baud rate.

If the Speed Conversion Switch S5 is set to ON, the two sides of the UART can be clocked at different baud rates, providing up/down Speed Conversion.

Since the UART contains only a single character of Memory, the Output Clock (Loop) should always be set as fast or faster than the Input Clock to prevent character over-runs.

Speed Conversion is convenient if the local teleprinter is set for 100 WPM, because the front panel switch may be used to select slower incoming baud rates, which will be up-converted by the UART to 100 WPM. The UART in this mode of operation is an effective electronic gear shift.

DUAL CRYSTAL-CONTROLLED CLOCK

The Dual Clock circuitry consists of a CMOS oscillator (Z1) and a very low frequency crystal (60.000 KHz), whose output is divided by two identical frequency dividers: Z7/Z8 and Z9/Z10.

When the Speed Convert switch (S5) on the TSR-200D assembly is OFF, both sides of the UART regenerator are driven by the output of Clock 1 Divider, which is controlled by the front panel Signal Speed select switch.

If this switch is set to 75 bauds, an incoming signal will be processed thru the UART at 75 bauds.

If the Speed Convert switch is set to ON, the Signal Speed switch will select the input baud rate (baud rate of the incoming signal) and the 8-pole DIP switch (S2) will select the baud rate at which the regenerated signal will be clocked out of the UART and sent to the local teleprinter.

This output clock may be programmed for baud rates from 37.5 bauds to 3750 bauds. Poles 1 thru 4 represent the Most Significant Digit (MSD) and Poles 5 thru 8 represent the Least Significant Digit (LSD). The BCD weight of each switch pole is etched on the PC board just below the switch.

Assuming that the local teleprinter is geared for 100 WPM (74.2 or 75 baud operation), S2 must be programmed for 75 Baud operation.

To determine the proper divisor number for a baud rate, use the following formulae:

- 1) BAUD RATE X 16 = CLOCK FREQUENCY (HZ).
- 2) 60,000/CLOCK FREQUENCY = DIVISOR.

Example: 75 Baud X 16 = 1200 Hz. $\frac{60,000}{1200} = 50$.

Therefore, if S2 is programmed with a divisor (BCD number) 50, the frequency dividers of Clock 2 will divide the 60.000 KHZ oscillator signal down to 1200 Hz, and the UART will output the regenerated signal at 75 Bauds.

BILATERAL STEERING CIRCUIT

When used in the Half-Duplex mode, the two clocks are inverted when the terminal unit is switched between Receive and Send, which permits effective Speed Conversion of both incoming and outgoing signals. If the UART is up-converting in Receive, it will be down-converting in Send.

This switching of Input and Output ports of the UART and the automatic inversion of the two clocks is accomplished by the Bilateral Steering Circuit, which consists of Z3, Z4, Z5 and Z6.

UART PROGRAMMING

The UART may be programmed for various code levels and functions.

Assuming that the MPC-1000CR is to be used for Radio TTY communications with the 5 level Baudot (Murray) code, program the UART via the 8-pole DIP switch at S3:

SWITCH POLE	FUNCTION	MODE	SWITCH POSITION
8	EPS	ZERO	LEFT
7	SBR	NO	LEFT
' 6	NBl	ZERO	LEFT
5	NB2	ZERO	LEFT
4	TSB	ONE	LEFT
3	SP CAL	OFF	RIGHT
2	PARITY	NO	LEFT
1	FSK	EIA	LEFT

If other coding is desired, the UART may be re-programmed per the coding charts on the TSR-200D Schematic Print 75164.

UART OPTIONS

STOP BIT REQUIRED (SBR): Normally it is best to leave this function in the NO position. There is no reason to force the UART to dump a good character just because the Stop Bit was not detected on the incoming signal. Since all languages are highly redundant in structure, it is always better to print a character, even if it is wrong. The precise Stop Bit generated at the end of each regenerated character will prevent the local teleprinter from losing signal sychronization.

TOTAL STOP BITS (TSB): The UART offers the option of attaching a 1.0 or 1.5 Character Unit stop bit to the end of the regenerated character. Selecting a 1.0 CU stop bit guarantees no character over-runs with Baudot teleprinters operating with 7.0, 7.42 and 7.5 CU coding.

<u>PARITY & EPS</u>: Baudot Coding does not require Parity, so Pole 2 of the UART Program Switch should be set to NO (LEFT). With Parity set to NO, ESP has no function, so Pole 8 can be left in either position.

<u>SPACE CAL (SP CAL</u>): It is the nature of a UART to always set high, that is MARK. Pole 3 permits the UART's output to be forced low for calibration purposes.

TEST POINTS

Seven Test Points have been provided on the TSR-200D assembly to assist in rapid signal tracing and trouble shooting:

TP-1: CRYSTAL OSCILLATOR OUTPUT

The oscillator circuit is comprised of a Statek quartz crystal, sealed in a gold-plated TO-5 type can and a CMOS 14007 DIP package. It is not unusual for this type of oscillator to take up to four seconds to start oscillating after initial turn-on. The nominal frequency of this crystal is 60.000 KHz ±0.05%.

TP-2: CLOCK 1 OUTPUT

The frequency at TP-2 is the 60 KHz clock divided by the Signal Speed Select dividers (Z7 and Z8). If the Signal Speed switch (S1) is set for a division of 82 (45.45 Baud), the output frequency will be 60,000/82 =732 Hz.

TP-3: CLOCK 2 OUTPUT

The frequency at TP-3 is the 60 KHz clock divided by

the Loop Speed Select dividers (Z9 and Z10). If the Loop Speed Switch (S2) is set for a division of 50 (74.2/75 Baud), the output frequency will be 60,000/50 = 1200 Hz.

TP-4: UART INPUT CLOCK

The frequency at TP-4 is the Input Clock to the UART at the output of the bilateral steering section. In Receive, it is Clock 1 and in Transmit, it is Clock 2.

TP-5: UART OUTPUT CLOCK

The frequency at TP-5 is the Output Clock to the UART at the output of the bilateral steering section. In Receive, it is Clock 2 and in Transmit, it is Clock 1.

TP-6: UART DATA INPUT

This test point is the same as Pin 20 on the UART, which is the DATA INPUT port. In Receive, it contains the unregenerated signal from Q6 (loop driver) in the MPC, and in Transmit, it contains the unregenerated signal as originated at the local teleprinter, TD, etc.

TP-7: UART DATA OUTPUT

This test point is the same as Pin 25 on the UART, which is the DATA OUTPUT port. In Receive, it contains the regenerated (and possibly speed-converted) data signal that is routed to the high level keyers. In Transmit, it contains the regenerated signal as generated by the local teleprinter.

DIGITAL AUTOSTART

Most terminal units utilize an analog form of autostart that is known as MARK Autostart. It responds to any amplitude energy in the Mark filter of the terminal unit. For this reason, it is susceptible to false starts caused by SSB, CW, noise crashes, static and swish-thru carriers. It does not respond to energy in the Space channel.

In addition to Mark autostart, all Dovetron terminal units offer a second form of analog autostart: FSK Autostart. This type of autostart ignores constant amplitude energy in either the Mark or Space channel, but responds to changes in amplitude in either channel. It is a very useful autostart system when the transmitting station maintains a "marking" carier for long periods of time. It permits the terminal unit to "time-out" the teleprinter during those long periods of inactivity. A complete description of these autostart forms is contained in the MPC-1000C section of this manual, pages 21 and 22.

A third form of autostart is available in the MPC-1000CR: Digital Autostart (DAS).

The DAS circuitry is located on the TSR-200D assembly and consists of Z11, Z12 and their associated components.

This unique circuit monitors the contents of the UART's parallel output register. Whenever it senses a Space Character, which is configured in the Baudot Code as SPACE-SPACE-MARK-SPACE-SPACE, is generates a logic 1 to the Autostart circuitry on the main board, enabling the autostart relay KL.

The Digital Autostart circuit is always connected to the MPC-1000CR autostart circuit, but in the MARK and FSK positions of the Autostart Select switch, is over-ridden by either the MARK or FSK Autostart commands. When the Autostart Select switch is in the DIGITAL position, the MARK and FSK modes are disconnected and the DIGITAL Autostart functions as the sole control source.

Both Character Recognition and Speed Determination are accomplished in the DAS, because Baudot characters sent at speeds other than what the UART has been set for, do not generate the necessary Mark/Space bit combinations to duplicate a Space Character.

If the front panel Signal Speed switch is set for 45.45 baud operation, a Space Character will not be detected if the incoming signal is operating at 56.88, 74.2 or 75 bauds, and probably not at 50.00 bauds. The latter depends somewhat on the amount of bias distortion on the incoming signal, etc.

If the baud rate is correct, but the signal inverted, the FIGS character will duplicate the coding of a Space Character but generally not often enough to enable the Digital Autostart Threshold.

The Threshold of the DAS is set by R53 on the TSR-200D assembly.

Although this form of Digital Autostart is not Selective Calling, it may be used in a Selective Calling mode by setting the Turn-On threshold to mid-scale or above, requiring the initial receipt of 10 or more consecutive Space Characters to achieve Turn-On.

Statistically, the Space Character will be generated at random by static and noise crashes. If the Threshold is set too low, one of these noise pulse combinations may load the output register of the UART with a SPACE-SPACE-MARK-SPACE-SPACE combination and "fake" the DAS into a false start. The next noise crash will change this coding in the UART's output register and the DAS will proceed to Time-Out and turn off.

If by chance only one noise crash came thru and duplicated the Space Character, the teleprinter would be turned on and left on, as long as the Space Character was in the UART's output register. But with no other noise crashes coming thru, the printer will stay idle and not print garble.

Either way, the Digital Autostart performs its function in a much superior way to any analog form of autostart.

CALIBRATION PROCEDURE

MAIN BOARD CALIBRATION

The calibration procedures in the MPC-1000C Section of this manual should be followed for calibrating the main board of the MPC-1000CR.

AFSK TONE KEYER CALIBRATION

If the TSR-200D Regenerator is turned off at S4 on the TSR-200D assembly, the Mark and Space tones may be calibrated per the main board section.

Another and easier approach, with the TSR-200D turned on, is to switch Pole 1 of the UART Program Switch S3 from EIA to MIL (or vice-versa), which will invert the tones.

After calibration of the second tone, remember to put S3 back in its original position.

TSR-200D REGENERATOR TESTS

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Check the crystal oscillator for an output of 60.000 KHz ±5 Hz at TPL.

Check Clock 1 output frequency at TP2. The output frequency will be determined by the setting of the front panel Signal Speed Select Switch:

45	Baud		732	Hz.
50	Baud		800	Hz.
57	Baud		910	Hz.
75	Baud		1200	Hz.
110	Baud	(ASCII)	1765	Hz.

These frequencies will have an accuracy of ±1 Hz.

Check Clock 2 output frequency at TP3.

The frequency will be determined by the setting of the 8-pole DIP switch located at S2, and will be identical to the frequencies listed above.

To check various frequencies, remember that the frequency at TP3 is determined by the following formula:

60,000 BCD DIVISOR SET IN S2

E-Series

-- 213-682-3705



INSTALLATION INSTRUCTIONS

627 FREMONT AVE. SOUTH PASADENA, CALIFORNIA 91030

TSR-200 to E-Series Dovetron MPC-1000(C)

Install the two bolts with a nylon washer between the bolt-head and the bottom of the main board. Snip off any long component leads that might short to the head of the bolts. Slip on the nylon standoffs and lightly secure in place with the locking nuts.

The TSR-200 may be set on top of the locking nuts to give you a better idea of the cable routing requirements. Do not mount the TSR-200 in the TU until all the wires have been installed.

The following installation instructions pertain only to E-Series terminal units. Check the main board number on the bottom side of the TU. It should be A75100-E.

TSR-200 CONFIGURATION

The TSR-200 is manufactured in two different configurations depending whether it is to be used in the B/C or D/E Series Dovetrons.

Check the TSR-200 board and verify that $\frac{R27}{R29}$ near Jl socket is 200 ohms (not 2000 ohms) and that R40A (10K) is installed and that R40B is not installed.

CR6 is a bypass capacitor for the-V line and is not normally used when the TSR-200 is installed in any Dovetron terminal unit.

TU MODIFICATION

Remove the jumper wire installed between REGEN IN and REGEN OUT.
Remove the jumper wire installed between EIA and AFSK INPUT.

These jumpers are normally red, and their removal completes modification of the MPC-1000(C) E-Series terminal unit prior to installation of the TSR-200

CABLE INSTALLATION

The Power/Logic cable is terminated with a 14 pin connector and has 14 wires in the cable. Do not confuse it with the Speed Cable that has a 16 pin connector and only 8 wires.

Dress the Power/Logic cable along the rear of the terminal unit in such a way that the 14 pin connector will easily plug into the 14 pin socket on the TSR-200 at the left rear. Trim and connect the following wires as directed: (Se Schume the following assumes as funt panel "Referent pointch).

- 1) Connect J1-2 (Red-Ground) to E-50 directly below the terminal unit's Audio Input connector.
- 2) Connect J1-4 (Yellow-EIA FSK) to the rear panel EIA FSK connector.
- 3) Connect J1-1 (Brown-AFSK KEYER) to the rear panel AFSK INPUT connector.
- 4) Connect J1-7 (Violet-DATA INPUT) to the rear panel REGEN OUT connector.

Installation Instructions TSR-200 to E-Series MPC Page 2 of 2

- 5) Connect J1-14 (White/Yellow*-DATA OUTPUT) to the rear panel REGEN IN connector. *Do not confuse white/yellow (14) with white/brown (11).
- 6) Break-out the White/Brown (-15V) and White/Red (+15V) wires about three inches from the connector end of the cable and dress them forward to the +V and -V points near the right side of Z19 on the TU's main board.
- 7) Connect J1-11 (White/Brown-Neg 15 Volts) to the -V point at Z19.
- 8) Connect J1-12 (White/Red-Pos 15 volts) to the +V point at Z19.
- 9) Control Line #1 is going to be used in the E-Series. Breakout the Blue wire (J1-6) out of the cable right behind the CRT and route the blue wire in any convenient manner to a location directly in front of the Autostart Relay K1.

Locate the anode end of CR54 and CR55 locations. Diodes are not normally installed in these locations. Install the loose end of the Blue wire in either anode hole. The anode end is closest to the right side of the terminal unit.

J1-5 (Green) is SPACE CAL line and is not normally used, because a Space Cal control has been provided on the 8PST DIP Uart-programming switch. If Full-Shift CW ID is desired, this Space Cal line may be routed to a rear panel connector, and when externally grounded, will shift from Mark to Space.

If not used, it is best trimmed off or tied back.

The other five unused wires may also be trimmed off or tied back: Orange (Control Line #2), Gray (Parity Enable), White (No Circuit), Black (No Circuit) and White/Orange (No Circuit).

Cable installation is now complete.

Do not plug cable into TSR-200 yet. Turn on the terminal unit, and verify that +15 volts is available on Pin 12 and that -15 volts is available on Pin 11 of J1.

Mount the TSR-200 on the two upright bolts and secure tightly in place with the locking nuts. Install cable into Jl socket with the notch in the connector's corner (signifying Pin 1) lined up with Pin 1 of Jl socket. With proper installation, the notched corner of the plug will be closest to the REGEN ON-OFF (S4) switch and directly above the "1" indicator etched on the board.

If an external speed control switch is to be used, assemble the cable and switch per the assembly drawing 75131.

Consult TSR-200 OPERATING INSTRUCTIONS for proper programming of the Uart-function switch and the speed switches.



TSR-200 SPEED CONVERTER-REGENERATOR

OPERATING INSTRUCTIONS

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When installed in a Dovetron MPC-1000 or MPC-1000C terminal unit, the TSR-200 Speed Converter-Regenerator functions as a Signal Regenerator and an UP-DOWN Speed Converter.

UART PROGRAM

Assuming that the MPC/TSR-200 combination will be used for radio RTTY communication (5 level Baudot code), program the Uart via the 8 pole DIP switch at location S3:

Switch Pole	Function	Mode	Switch Position
8	EPS	Zero	Left
7	SBR	NO	Left
6	NB 1	Zero	Left
. 5	NB2	Zero	Left
4	TSB	Two	Right
3	SP CAL	Off	Right
2	Parity	No	Left
1	FSK	EIA	Left

The Uart may be re-programmed per the coding charts on the schematic print, Drawing No. 75134, if other coding is desired.

Switch pole 7 sets the SBR (Stop Bit Required). Normally, it is best to leave this function in the NO position. There is no reason to force the Uart to dump a good character just because the Stop bit on the incoming signal was not detected.

With the redundancy of the English language, it is always better to print a character, even if it is wrong, because the automatic stop bit generated by the Uart will prevent the local teleprinter from loosing signal synchronization anyway.

Switch pole 4 sets the TSB (Total Stop Bits attached to the end of each regenerated character) and with all Uarts may be set for ONE. If using a Uart that can be programmed for 1.5 Stop Bits when using the 5 level code (AY-3-1014, AY-3-1014A or IM6402), the TSB may be set for TWO stop bits, in which case, a 1.5 CU stop bit will be affixed to the end of each regenerated character.

Switch pole 3 (SPACE CAL) <u>must</u> be OFF during normal operation. When in the ON position, the output line to the AFSK tone keyer is "forced" to Space for AFSK tone calibration purposes.

Switch pole 2 (Parity) will normally not be used with a 5 level code. When Parity is inhibited (NO), switch pole 8 (EPS) really serves no function and may be left in either position.

Switch pole 1 (FSK) permits the operator to select either RS232C or MIL STD 188C FSK polarities.

In B, C and D Series Dovetrons, the AFSK Tone Keyer was originally driven by the output of the MIL STD 188C op-amp. In order for the SPACE CAL switch (Pole 3 of S3) to function properly, the AFSK tone keyer should be driven by the EIA (RS-232C) FSK signal.

For this reason, Switch Pole 1 of S3 should be left in the EIA (LEFT) position.

Since EIA is reverse-polarity from MIL STD 188C, it was necessary during installation of the TSR-200 to reverse the gray and violet wires attached to the rear panel AFSK Mark and Space tone potentiometers. Violet should go to the Mark pot, and the Gray should go to the Space pot. Recalibration of the Mark and Space tones may be necessary, although the tones will probably be within 1% of their previous frequencies.

REGEN ON-OFF SWITCH (S4)

S4 is provided to permit the TU to be used in the non-regenerating mode, i.e., just as if the TSR-200 is not installed, and has been provided mainly as a trouble shooting aid.

DUAL-CLOCK PROGRAM

The crystal-controlled clock consists of an oscillator section and two identical BCD/N divider sections. The crystal is a Statek Piezo-electric quartz tuning-fork crystal mounted in a three-lead TO-5 package and operates at 60,000 Khz.

Baud rates between 37.5 and 3750 may be programmed into both sections independently of each other. Programming is done by an 8 section DIP switch. Poles 1 thru 4 represent the Most Significant Digit (MSD) and poles 5 thru 8 represent the Least Significant Digit (LSD). The BCD weight of each switch pole is etched on the PC board directly in front of the switch.

The BCD number by which each clock will divide for the five most popular communication baud rates is etched on the board between the two switches.

Clock 1 is the left-most switch and must be programmed for the baud rate of the incoming signal by selecting the proper BCD divisor.

The required BCD divisor =

60,000 Baud Rate Desired X 16

Using this formula, the BCD divisor for 45.45 Baud (60 WPM) calculates as the BCD number 82. The proper divisors for 50.0, 56.88 and 74.2/75.0 Baud signal rates are also etched on the PC board. The fifth rate

(110 Baud) is the divisor for ASCII (8 level) 100 WPM operation and produces a clock frequency of 1765 Hz.

CLOCK PROGRAM

	POLE ON	1	2	3	4 X	5	6 X	7	8		45.45 Baud 60 WPM
60 WPM:	OFF	X	X	X		Х		х	x		BCD = 82
	MSD	1	2	4	8	1	2	4	X 8	LSD	Freq = 732 Hz
	POLE	1	2	3	4	5	6	7	8		50.00 Baud
- <u>-</u> -	ON	x	Х	Х		Х		Х			67 WPM
67 WPM:	OFF				X		х		Х		BCD = 75
	MSD	1	2	4	8	1	2	4	8	LSD	Freq = 800 Hz
	POLE	1	2	3	4	5	6	7	8		56.88 Baud
	ON		х	X			Х	X			75 -WPM
75 WPM:	OFF	Х			Х	Х			X	•	BCD = 66
	MSD	1	2	4	8	1	2	4	8	LSD	Freq = 909 Hz
	POLE	1	2	3	4	5	6	7	8		74.2/75.0 Baud
	ON	X		X							100/106 WPM
100 WPM:	OFF		X		X	Х	Х	X	Х	· · ·	BCD = 50
	MSD	1	2	4	8	1	2	4	8	LSD	Freq = 1200 Hz

Assuming that the local teleprinter is geared for 100 WPM operation, the right-most switch (Clock2) must be programmed to divide by 50. The division of 60.000 Khz by 50 yields 1200 Hz, which is the correct clock frequency for 100 WPM operation (75 Baud X 16 = 1200 Hz).

When the TSR-200 is switched from Receive to Transmit, Clock 1 and CLOCK 2 are interchanged via solid-state switching at the input and output clock ports of the Uart regenerator. This switching section also interchanges the Data Input and Output lines.

This action permits an incoming signal to be up-converted to a faster teleprinter during Receive, and the teleprinter's faster keyboard signal to be down-converted to the slower signal rate during Transmit.

RECEIVE MODE

All signals being demodulated by the MPC are now also being regenerated by the TSR-200. Output bias distortion to the teleprinter is less than 1%. If the dual clocks are being run at different speeds, the TSR-200 is also performing an UP or DOWN speed conversion.

Since the TSR-200 contains no buffer memory, Down Conversion is not practical, since characters will be dropped.

In other words, the companion teleprinter should be geared for a speed

equal to or greater than the fastest signal speed that is to be copied.

Many press stations operating at 50 Baud utilize a longer than normal stop pulse, and for this reason, these stations may be down-converted to a 45.45 Baud teleprinter without character loss.

TRANSMIT MODE

Some provision must be made to switch the TSR-200 into transmit when the MPC-1000(C) is put into transmit or standby, etc.

When the #2 control line was installed at the LOCK connector, the green wire to E65 was removed, because it is the nature of a Uart to be high on Mark, which now provides the Mark Lock on the high level keyer.

To control the Transmit/Receive mode from the front panel Standby switch, connect the Lock connector to Remote 3, and put a shorting plug in Remote 1. When the Standby switch is put in Standby, the Lock line will be pulled to ground via Remote 3 and Remote 1.

For remote control, a ground applied to the rear panel Lock connector will put the TU into Standby and put the TSR-200 into the Transmit mode.

MS-REV (RY GENERATOR)

With a TSR-200 installed in the MPC-1000(C), the MS-REV no longer functions as an RY Generator.

Since the Uart requires a valid start pulse to accept a character bit into its input register, only the letter Y is accepted and regenerated because Mark-Space reversals cannot by definition provide 2 sequential space pulses, which are required to generate the letter R.

In the Transmit mode, if the RY Generator (Z47) and Clock 2 of the TSR are set to the same speed, a continuous string of Ys will be outputted, regardless of the position of the position of the Normal/Reverse switch. For 100 WPM operation, Clock 2 is set for 75 Baud and the RY Generator is set for 37 Hz. At 60 WPM, Clock 2 is set for 45.45 Baud and the RY Generator is set for 23 Hz. The rule of thumb is to set the frequency of the RY Generator (in terms of Hz) to half the Baud rate (in terms of Baud).

In the Receive mode, if the RY Generator, the TSR's Clock 2 and the local teleprinter are set for 100 WPM, a continuous string of BLANKS will be received with the Normal/Reverse switch in the Normal Position. Since this is a non-typing function, it is useful for ribbon re-inking and machine maintenance.

In the Reverse position, the local teleprinter will receive a continuous string of LTRS. If the switching between NORMAL and REVERSE is done slowly, the TSR-200 may output a continuous string of the letter A. Switching back to NORMAL, and then quickly to REVERSE, will produce the LTRS character.

AFSK TONE KEYER CALIBRATION

The Mark tone can be calibrated at any time that the tone keyer is outputting a Mark tone.

To calibrate the Space tone, the TSR-200 must be forced into the Space condition. This can be done by switching Switch Pole 3 of the Uart Program switch to SHACE CAL ON (left), or by switching the TSR-200 OFF at S4 and removing the Loop Fuse at the rear panel.

The SPACE CAL line was left un-cut and Un-used (J1-5 Green) when the J1 cable was installed in the MPC. This line may be brought to the rear panel, and when grounded, will force the AFSK tone keyer into the Space condition for calibration of the Space tone.

This line may also be used for CW-ID with a "full-shift" of the AFSK tone keyer. The normal AFSK CW-ID option in the MPC is only "half-shift".

TEST POINTS

Seven Test Points have been provided on the TSR-200 board for rapid trouble shooting:

TP-1: CRYSTAL OSCILLATOR OUTPUT

The oscillator circuit is comprised of a Statek quartz crystal, sealed in a gold-plated TO-5 type can and a CMOS 14007A DIP package. It is not unusual for this type of oscillator to take up to four seconds to start oscillating after initial turn-on. The nominal frequency of this crystal is 60.000 KHz ±0.05%.

TP-2: CLOCK 1 OUTPUT

The frequency at TP-2 is the 60 KHz clock divided by the Signal Speed Select dividers (Z7 and Z8). If the Signal Speed switch (S1) is set for a division of 82 (45.45 Baud), the output frequency will be 60,000/82 =732 Hz.

TP-3: CLOCK 2 OUTPUT

The frequency at TP-3 is the 60 KHz clock divided by the Loop Speed Select dividers (Z9 and Z10). If the Loop Speed Switch (S2) is set for a division of 50 (74.2/75 Baud), the output frequency will be 60,000/50 = 1200 Hz.

TP-4: Uart INPUT CLOCK

The frequency at TP-4 is the Input Clock to the Uart at the output of the bilateral steering section. In Receive, it is Clock 1 and in Transmit, it is Clock 2.

TP-5: Uart OUTPUT CLOCK

The frequency at TP-5 is the Output Clock to the Uart at the output of the bilateral steering section. In Receive, it is Clock 2 and in Transmit, it is Clock 1.

TP-6: Uart DATA INPUT

This test point is the same as Pin 20 on the Uart, which is the DATA INPUT port. In Receive, it contains the unregenerated signal from Q6 (loop driver) in the MPC, and in Transmit, it contains the unregenerated signal as originated at the local teleprinter, TD, etc.

TP-7: Uart DATA OUTPUT

This test point is the same as Pin 25 on the Uart, which is the DATA OUTPUT port. In Receive, it con-

tains the regenerated (and possible speed converted) data signal that is routed to the high level keyer (Q7) in the MPC. In Transmit, it contains the regenerated, etc., signal as generated by the local teleprinter, TD, etc.

VARIABLE FEATURES

By removing R44 (15 ohms) and connecting TP-4 to TP-5 with a jumper, both the INPUT and OUTPUT CLOCK ports of the Uart (Pins 17 and 40) may be driven simultaneously from Clock 1. This modification permits the TSR-200 to be used as a single speed regenerator and for its thru-put speed to be controlled by a single Speed Select cable assembly.

A second control line has been provided (Control Line 1). The installation of CR6, R39 and R40A, and the necessary removal of R40B, permits the Transmit/Receive function of the TSR-200 to be controlled by inverted logic, i.e., Receive = zero, and Transmit = +5 to +15 volts. This configuration is used in the Dovetron E-Series terminal units.

VOLTAGE MEASUREMENTS

The TSR-200 has been designed to operate from ± 15 to ± 18 volt sources. All voltage measurements are made in respect to chassis ground, which is also power ground.

Pin 1 of the Uart should measure approximately +5.1 volts, which is the zener level of CRL Pin 2 of the Uart should measure approximately -12 volts. C6 is not normally installed, because the MPC supplies clean, regulated voltage to the TSR. If an unregulated supply is used for the minus line at J1-11, C6 should be installed. A 10 Mfd, 20 volt tantalum is suggested.

PARITY

Although Parity is not generally used in RTTY radio communications, the ability to select Odd or Even Parity is inherent in the Uart, and provisions have been made to utilize it, should a future need for Parity arise.

If Parity is required, consult the manufacturer's spec sheet on the particular Uart installed in the TSR-200.

Parity Select is usually:

NP Ø	EPS Ø	Mode ODD
ø	1	EVEN
1	Ø or l	NO

Parity Select has been inhibited in the TSR-200 by switching the Uart Switch Pole 2 to NO (Left). With Parity inhibited in this way, Switch 8 (EPS) may be left in either position.

The front panel Signal Speed switch of the Dovetron MPC-1000R/TSR-500D combination contains five positions: 45, 50, 57, 75 and 110 baud.

The first four are the standard BAUDOT baud rates for 60, 66, 75 and 100 WPM operation.

The 110 baud position is intended for 100 WPM ASCII operation.

With a SBR-100 Selectable Baud Rate module plugged into the TSR-500D, this 110 Baud ASCII switch position enables the SBR-100 and the signalling rate of the terminal unit becomes that baud rate that has been programmed into the SBR-100.

Programming of the SBR-100 is accomplished via an 8-pole DIP switch mounted on the SBR-100 board.

This switch has its pole numbers molded into the top of the switch and the BCD (binary coded decimal) weighting of each pole etched on the PC board in front of the switch.

The four left-most poles are the MSD (most significant digit) and the four right-most poles are the LSD (least significant digit) of the BCD number.

As an example, to program the SBR-100 for 65 baud (88 WPM) operation, using the formula:

 $\frac{60,000}{16 \text{ X Baud Rate}} = \text{BCD NUMBER},$

the BCD number 58

will be used.

This means the MSD poles will be programmed for BCD 5 and the LSD poles will be programmed for the BCD 8.

To aid in the familiarization of this method of programming, the tops of switch poles 1, 3 and 8 have been marked with a red dot. When these three poles are ON, the BCD number 58 has been programmed, and the signalling baud rate will be 65 baud (Baudot 88 WPM).

To install the SBR-100, unplug the Signal Speed switch cable from the TSR-500D board and install the SBR-100 in its place, by inserting the header (H1) of the SBR-100 into the S1 socket of the TSR-500D.

The switch cable is then plugged into the high profile 16 pin socket (J1) on the SBR-100 board.

A ground wire must be connected between the SBR-100 and the TSR-500D.

The empty E-Points around the edge of the SBR-100 are ground. A convenient ground point on the TSR-500D is the front hole of the X6 INH location in the right front center of the TSR-500D board.

The SBR-100 will not function properly if this ground is omitted and the four standard Baudot signalling rates will be incorrect.

The SBR-100 may also be used with the TSR-200D Regeneration assembly and with the TBA-1000 Baudot-ASCII Code Translator. In these units it may be necessary to shorten the mounting bolts to provide clearance.

SSD-100 SOLID STATE CROSS DISPLAY

OPERATING INSTRUCTIONS

CALIBRATION

Calibration of the SSD-100 Display is accomplished by setting the two gain pots at the top edge of the SSD-100 board (R17 and R18).

The Mark Gain pot (R17) is near the front panel MARK VFO and the Space Gain pot (R18) is near the front panel SPACE VFO.

The Intensity Threshold pot (R11) is mounted halfway down the left side of the SSD-100 board.

Turn ON the MPC Series terminal unit, set the Mode switch to MS-REV and set the LEVEL control to 12 o'clock.

Tune in the Mark and Space tones from the AFSK tone keyer, using both the SSD-100 display and the individual Mark and Space LEDs mounted directly above the VFOs.

With both channels peaked for maximum amplitude, set the Mark and Space Gain pots so that four (4) LEDs on each side of the center pair (apex) are fully lit.

After a five minute warm-up, check the gain pots again. The display driver circuitry has a high degree of hysterisis and the gain in each channel may be set so that the fourth LED is "hard-on" and the fifth LED is fully off.

Set the Intensity Threshold potentiometer (R11) at mid-scale.

Block the ambient light flow to the photocell in the lower left quadrant of the display. (Use your thumb.) The light output of the display should drop to about half of the normal intensity. If not, adjust Rll so that this action occurs smoothly.

In some factory-installations, the front panel photocell replaces the board mounted photocell.

OPERATION AND INTERPRETATION

The incoming Mark signal is displayed on the horizontal line of LEDs and the space channel is displayed vertically.

The two LEDs (DS1 and DS2) at the apex of the cross are connected to the terminal unit's Signal Loss circuit.

When the two incoming tones are tuned-in properly, these two center LEDs will light, forming a complete cross.

If the terminal unit is incorrectly tuned, such as both channels tuned to the same tone, a cross will be displayed, but the center LEDs will not light, and a separate LED in the lower right-hand quadrant (DS5) will light, indicating that the terminal unit has automatically gone into Markhold.

This separate LED also lights when the terminal unit is switched to Standby (MPC-1000C) or Send (MPC-1000CR and MPC-1000R).

If the terminal unit is tuned to a steady Marking signal, the LEDs at the center of the cross will not light if the "sense" of the terminal unit is upside down. Reversing the NORMAL-REVERSE switch will cause the LEDs to light; filling in the line of lit LEDs.

A second separate LED (DS4) in the upper right quadrant monitors the high level loop supply and duplicates the indication from the front panel LOOP LED. This LED has been included in the SSD-100 display for operator convenience.

The SSD-100 also includes a unique Multipath Distortion Indicator (MDI) in the upper left quadrant. This LED (DS3) flashes in the presence of time or frequency dispersive multipath distortion. Its operation can be checked by tuning both channels of the terminal unit to the same incoming tone. The intersymbol interference generated by the RY Generator (MS-REV) will also flash this MDI LED.

The Multipath Distortion Indicator circuit consists of U3, Q2, DS3 and their associated components. To understand the validity of the MDI, it must be explained that terminal units generally use non-identical channel filters in the Mark and Space channels. For this reason, both filters exhibit their own characteristic groupresponse, time-delay, overshoot, ringing, etc. These non-identical filters have a tendency to distort the mark and Space channel signals unequally. The channel filters in the MPC Series terminal units are identical Bessel Function filters. Their Bessel characteristic makes them very "tame" in the presence of pulse signals (RTTY pulses in particular) and prevents ringing and overshooting.

Since they are identical, any distortion added to one channel is also added to the other channel.

The MDI monitors the output of the two channel filters. One channel is inputted to pin 8 of U3. The other channel is inputted to pin 9 of U3. This integrated circuit is a two-input NAND gate. If both channels contain amplitude energy simultaneously, the output of U3 (pin 10) goes LOW, i.e., zero. This is the normal function of a two-input NAND gate. This LOW is applied to three more NAND gates that are connected as inverters, whose outputs immediately go HIGH and drive Q2 into conduction. When Q2 conducts, the MDI (DS3) is turned on.

In this way, whenever the Mark and Space channels simultaneously

contain a significant amount of amplitude energy, the MDI will flash. By definition, time and frequency dispersive multipath distortion will flash the MDI.

The voltage dividers (R23/R25 and R24/R26) have been selected to "Flash" the MDI whenever pulse overlap at 45 to 75 bauds exceeds ten percent.

Since 10% bias distortion does not generally increase the error rate, it is best to operate the MPC Series terminal unit with the Multipath Corrector turned off. If the MDI starts to flash, turn the MPC on.

VARIATIONS AND OPTIONS

Provisions have been made for attaching an external intensity control to the SSD-100 at E-Point E2. Resistors R3 and R8 have not been installed, but locations have been provided that would provide part of an external intensity control circuit.

E-Point El has been provided to permit a front panel-mounted photocell at the INT location to be used instead of the board-mounted photocell.

E-Point E3 is the output of a four diode bridge (CR1-CR4). This bridge is driven by the original filament supply of the CRT (6.3 VAC at 600 mils). Since LEDs work equally well on pulsating DC, the output of this bridge supply is not filtered or regulated, and provides about 4.5 PVDC.

E3 may be bypassed with a 1000 Mfd capacitor to provide a 6.5 VDC source, capable of providing a 5.1 VDC regulated supply for possible future applications. Filtering this supply will increase the light output and power consumption of the SSD-100 display, so diode isolation is recommended. An increase in light output is not required, and increased power consumption by the bargraph display driver chips and the LEDs will only decrease their MTBF.

ADDENDUM

Two resistor locations have been provided at R21 and R22. Dovetron installs jumpers at these locations, but low impedance resistors (15-33 ohm) may be installed to limit current flow thru DS1, DS2, DS4 and DS5 in other applications.

SSD-100 SOLID STATE CROSS DISPLAY

INSTALLATION INSTRUCTIONS

FACTORY INSTALLATION OF SSD-100

When an SSD-100 Solid State Cross Display is to be installed in a Dovetron MPC Series Terminal Unit, the following components are not installed on the MPC Main Board A75100-E:

F3, F3 Fuse Clips, C53, C63, C64, C65, C66, C67, CR44(4), CR45, CR46, R173, R174, R175, R176, R177, R178, R179A, R179B, R180, R181, R182, R183, R184, R185, R186A, R186B, R187, R188, R190, R191, R192, R193, R194 and R195.

The photocell socket/leads assembly is not installed.

The CRT socket and cable assembly are not installed.

Rll4 (originally 1K) is changed to 68 ohms, 1/4 watt, 5%. Rl70 (originally 33 ohms) is changed to 120 ohms, 1/4 watt, 5%. R222 (originally 62K) is changed to 120 ohms, 1/4 watt, 5%.

The yellow wire connected to the cathode of the LOOP LED is moved from E34 to E47.

A jumper wire is installed between CRT-10 feed-thru and ground.

Z37 (originally μ 741CP) op-amp is changed to TI TL081CP.

The 8 pin plug-in cable assembly that connects the SSD-100 to the MPC main board is connected to various E-Points and feed-thru holes on the main board per the Installation Chart on SSD-100 Assembly/Schematic Print 75189.

FIELD RETROFIT INSTALLATION OF THE SSD-100K

The SSD-100K retrofit kit consists of an SSD-100 Display Assembly, an SSD Bezel with optical filter, an 8 pin interconnecting cable, 3 replacement resistors, an op-amp (TL081CP), and the necessary hardware to mount the SSD-100 in place of the original CRT assembly.

Since simple modifications are normally more successful than complex ones, only those components that would interfere with the operation of the SSD-100 are removed. Excess components may be removed.

 Remove and discard the CRT bezel, the mounting screws, the CRT shield, the CRT tube and the CRT socket assembly. When removing the CRT socket assembly, clean out the holes at points 1, 10 & 11.

-4s-

- Remove and discard the high voltage diodes at CR45 and CR46. This effectively removes high voltage from the CRT's original high voltage power supply.
- 3) Remove the F3 fuse located on the bottom side of the MPC main board.
- 4) The high voltage filter capacitors C66 and C67 may be removed. Save C66 (40 Mfd, 350 VDC) as a spare for loop supply filter capacitor C60.
- 5) Remove 1K (R114) to the right of Z37 and replace with 68 ohms.
- 6) Remove 33 ohms (R170) near pin 8 of Z43 (XR2206C) tone keyer and replace with 120 ohms.
- 7) Remove 62K (R222) in left front corner of main board and replace with 120 ohms.
- 8) Remove photocell socket/leads assembly by disconnecting the two leads from E47 and E48. Clean out E47.
- 9) Move the yellow wire from LOOP LED from E34 to E47.
- 10) Connect jumper wire from CRT E10 to ground feed-thru marked (-). This ground is also at the anode end of CR53.
- 11) Remove (μ 741CP) and replace with Texas Instruments TL081CP (Z37).
- 12) The 2N3439 transistors (Q10, Q11 & Q12) may be left in their sockets. They will spare the Q7 loop keyer, Q5 and Q6 on the main board and Q1 and Q2 on the SSD-100 Display assembly.
- 13) Remove the disc capacitors (.01) at C63 and C64.
- 14) Install the 8 wire interconnecting cable per Cable Installation chart on SSD-100 Assembly/Schematic print 75189.

The 8 wire cable has standard EIA color coding: Pin 1 = brown, pin 2 = red, pin 3 = orange, pin 4 = yellow, pin 5 = green, pin 6 = blue, pin 7 = violet and pin 8 = gray.

Secure the cable (2 inches from connector end) with the cable clamp supplied at the main board mounting screw at the front edge. Dress the cable to run directly down the center line of the terminal unit.

- 1) MPC +V at TP9, which is located between TP10 and CR60.
- 2) MPC jumper location C, just to the rear of CR60, and to the left of locations A and B.
- 3) Junction of R214 and R215. R214 is not normally installed. Connect wire to the front-most feed-thru of R214. This

location is the left of Q13 and about 1 inch from the front edge of the main board.

- 4) MPC Ground at TP8, which is just to the left of the large white capacitor (1.0J100) C55.
- 5) CRT Filament Line 1, located behind the FOCUS potentiometer, R193.
- 6) CRT Filament Line 11, located behind the ASTIG potentiometer, R194.
- 7) Space Channel. Locate the old C64 location. Follow the trace from C64 to the left and locate feed-thru on this trace at the center-line of the terminal unit.
- 8) Mark Channel. Locate the old C63 location. The proper location for wire 8 is the feed-thru directly behind the feed-thru used in the previous step.

MECHANICAL INSTALLATION OF SSD-100 DISPLAY AND BEZEL ASSEMBLIES

Install the SSD-100 display and SSD bezel per the mechanical drawing on SSD Assembly/Schematic print 75189. The bezel and the four bolts are installed from the front of the terminal unit, and immediately secured with four 6/32-3/16 inch nuts.

The SSD-100 display card is slipped onto these four mounting bolts, with the LED cross display side to the front of the terminal unit and with the Mark and Space Gain pots at the top of the board. Be careful not to pinch any local wires between the bolts and the SSD-100 board.

Secure the SSD-100 board in place with the second set of four 6/32-3/16 inch nuts.

ELECTRICAL INSTALLATION OF THE SSD-100 DISPLAY

The connector on the end of the 8 wire cable plugs into the SSD-J1 connector, which is located at the bottom left (viewed from the front of the SSD-100 board.

The notched corner on the top of the connector shell indicates Pin 1.

The cable is installed properly when this notched corner (Pin 1) is closest to the center of the SSD-100 board. Installing the cable backwards will damage the SSD-100 display.

If a plastic cable clamp has been supplied with the SSD-100K kit, it may be secured under the number 4 bolt at the front, center edge of the main board and used to tie down the 8-wire cable.

This completes the modification of the terminal unit, and the electrical and mechanical installation of the SSD-100 Solid State Display.

If the original CRT adjustment potentiometers have been left on the main board, set them for Mid-scale and forget. Refer to the SSD-100 Operating Instructions for the proper calibration procedure for the Mark Gain, Space Gain and Intensity Threshold pots.

REMOTE CRT DISPLAY

The MPC-1000C and MPC-1000CR have both Remote Scope Display and Dual-Diversity connectors on the rear panel.

The MPC-1000CR/DK and MPC-1000R (above Serial R050) have only Dual-Diversity connectors at the rear panel. These Diversity connectors are connected Mark J3 to E54 and Space J2 to E53. For remote oscilloscope operation, move the orange wire from E53 to E51. Move the yellow wire at E54 to E52. These E-Points are located at the left rear corner of the MPC main board.

SSD-100 LOOP LED INTENSITY

Light Emitting Diodes (LEDs) act somewhat like zener diodes, but their zener voltages are not precise.

The LOOP LED (SSD-DS4) is paralleled across the front panel LOOP LED (MPC-DS1).

If one of the LEDs has a significantly lower zenering point than the other, the second LED will not light, or at best, will operate with a very low light level output.

In the case that the SSD-DS4 LED does not light, but the front panel LED does light, put a 120 ohm, 1/4 watt resistor in series with the front panel LED (MPC-DS1).

At Dovetron, this resistor is added by moving the yellow wire on the anode of MPC-DS1 from E-Point 34 to E-Point 47 and installing the 120 ohm resistor in location R222. (If this location contains a 62K resistor, which was part of the CRT photocell circuit, remove it and discard it). Locate CRT Pin 10 on the mainboard. This location is directly in front of diode CR47. Connect a wire between CRT Pin 10 and Ground. A convenient ground location is the mounting feedthru for the anode end of zener diode CR53, which is directly to the right of C65 and in front of CRT INTENSITY pot R195.

If the front panel MPC-DS1 LED does not light, and the SSD-DS4 does light, add the 120 ohm resistor in series with the SSD-DS4 LED. This is easily accomplished by removing the SSD-100 display assembly and installing the 120 ohm resistor at location SSD-R21, which is just above the LM3914 at location UL, replacing the jumper wire.

When re-installing the SSD-100, be sure that pin 1 of the 8 wire connecting cable is toward the center of the SSD-100 board. Pin 1 is identified with a "notched" corner on the top of the cable connector.

ASCII OPERATION WITH MPC-SERIES

A high performance terminal unit has its bandwidth tailored for the baud rate at which it is going to operate. Standard Dovetron terminal units are tailored for optimum performance over the range of 45 to 75 baud. This is accomplished in the design of both the channel filters and the low pass filters.

ASCII at 110 baud can be processed thru the Dove with excellent results. The slight distortion caused by the tight bandwidth of the low pass filters is cleaned up with the Multipath Corrector. The Bessel function channel filters restrict some signal power (sideband energy), but if the signal is good, copy will be good.

The biggest problem with 110 (and faster) ASCII is that the Mark and Space pulses are only 9 milliseconds long (compared to 13.5 ms at 75 baud and 22 ms at 45 baud) and multipath propagation tears them apart before the terminal unit has a chance to process them.

If the terminal unit is to be dedicated to ASCII operation, the <u>low pass</u> <u>filters</u> can be opened up by changing the eight 510K resistors at locations R45 thru R48 and R70 thru R73 to:

<u>110 Baud - 330K.</u> <u>150 Baud - 240K.</u> <u>300 Baud - 120K.</u> <u>600 Baud - 62K.</u>

A set of precision resistors are available from Dovetron at \$20.00 per set to open up the <u>channel filters</u> for 150, 300 or 600 Baud, but remember that the performance of these channel filters at 45 and 75 baud is very poor. You are better off to maintain the original channel filters and manipulate the bandwidth (Signal to Noise Ratio) at the low pass filters.

The Mark II versions of the Dove contain a BBP-100 Binary Bit Processor, which permits front panel selection of three different bandwidths. Normally, the bandwidth modules supplied are 50, 75 and 110 Baud. Two spare bandwidth modules are stored on the BBP assembly and they are easily changed to any bandwidth (baud rate) required.

Above 150 Baud, the spike suppression cap (C52) in the high level loop circuit should be changed to a 0.05 mfd cap. If the high level neutral loop is not going to be used, C52 can be removed entirely, but Q7 will be damaged by inductive spikes if a mechanical teleprinter is plugged into the loop connectors.

Baud rates above 600 baud are not very practical. At 850 Hertz shift at 1200 baud, assuming Mark-Space Reversals, 65% of the incoming signal power falls at the center frequency, that is, halfway between the Mark and Space tone frequencies, and only 16% of the signal power is processed thru either channel filter.

The TSR Regeneration Assemblies can be used at 110 Baud without modification. The UART Program switch will have to be set for either 7 or 8 level operation, and the Word Correction circuit on the 500D will have to be disabled by inserting a jumper at X6.

Since most high speed peripherals have signal regeneration, it is probably not practical to modify the TSR for higher baud rates, but a 153.6 KHz crystal and a pair of 8PST DIP switches are available from Dovetron for \$20.00 to accomplish such a modification.

Due to the spectral dispersion of the Mark and Space tone carriers at the higher baud rates and the flat fades that plague HF signals with less than 400 Hz shift, an 850 Hz shift is recommended for all ASCII Baud rates.



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	ARB		R3.9,3 R20 R8.16.1 R4-6.1 R7.22.2	7.23.26 0-15/18/1			4	אד. 2 אר. 2 אר. 4 אר.					
c	AEB	Fil.M	R3.9,3 R20 R8.16/1 R4-6,10 R7.22.2 R27	7.23.26 0-15/18/1			4	7K 0K 0K 4.7K					
		FILM	R3.9,3 R20 R8.16.1 R4-6.10 R7.22.2 R27 R25	7,23,26 0-15/18,1 (4,29,30		RESI		ΟK ΔK 4.7K 1.5K 1.2K		1,5%	70	R-0	
			R3.9,3 R20 R8.16.1 R4-6.1 R7.22.2 R27 R25 R25 R2	7.23.26 0-15/18/1 (4.23,30				20K ΔK 4.7K 1.5K 1.2K 1K 470±				R-0	HIM OROLA
 	2B.	FILM .	R3.9,3 R20 R8.16.1 R4-6.11 R7.22.2 R27 R27 R25 R2 R21,3	7.23.26 0-15/18/1 (4.23,30		TRAN	4 2 1 57025 57025 57025	-7K -0K -0K -0K 	/ 511 /, 511	نے د رور د	<i>N</i>	R-0 MOT	0801A
	128.	FILM IBA	R3.9.3 R20 R8.16.1 R4-6.1 R7.22.2 R27 R25 R2 R21.3 Q2.4.	7.23.26 0-15/18/1 (4.23,30		TRAN	4 2 1 1 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 5 7 5 7 5 7 5 7 5 7 5 7 5 7 5 7 5	-7K -0K -0K -0K 	/ 511 /, 511	نے د رور د	<i>N</i>	R-0 MOT	ORDLA
21	1221 128. 1221 154	511.M 511.M 19A 116 139	R3.9.3 R20 R8.16.1 R4-6.1 R7.22.2 R27 R25 R2 R21, 3 Q2.4, Q3 Q1	7,23,26 0-15/18/1 (4,29,30 5		TRAN TRAN TRA	4 2 1 5 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 5 7 5 7 5 7 5 7 5 7 5 7 5 7 5 7 5	-7K -0K -0K -0K -0K -0K -0K -0K -0K -0K -0	/ 511 /, 511 , 511	3C0 3C0 3C0 3C0 3C0	<i>N</i>	R-0 MOT MOT	OROLA OROLA
	28. 128. 1400	FILM FILM 19A 166 339	R3.9.3 R20 R3.46.1 R4.6.1 R7.222 R27 R25 R2 R21,7 R25 R2 R21,7 R25 R2 R21,7 R2 R21,7 R2 R21,7 R2 R2 R21,7 R2 R2 R2,7 R2 R2 R2,7 R2 R2,7 R2,7 R2	7,23.26 3-15,18,1 (4,29,30 51		TRAN TRAN TRA	4 . 2 . 1 . 1 	7K 0K 0K 0K 1.7K 1.5K 1.2K 1.2K 1K 4701 NPN 2. NPN 2. NPN VER, S	, 511 , 511 , 511	3CU 3CD 1CDN 1CDN	<i>N</i>	R-O MOT NOT	OROLA OROLA OROLA
	1221 128. 1221 154	FILM FILM 19A 166 339	R3.9.3 R20 R8.16.1 R4-6.1 R7.22.2 R27 R25 R2 R21, 3 Q2.4, Q3 Q1	7,23.26 3-15,18,1 (4,29,30 51		TRAN TRAN TRA	4 2 1 5 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 2 5 7 0 5 7 5 7 5 7 5 7 5 7 5 7 5 7 5 7 5	7K 0K 0K 0K 1.7K 1.5K 1.2K 1.2K 1K 4701 NPN 2. NPN 2. NPN VER, S	, 511 , 511 , 511	3CU 3CD 1CDN 1CDN	<i>N</i>	R-O MOT NOT	OROLA OROLA
	128. 128. 154 1914	FILM FILM 19A 166 339	R3.9.3 R20 R3.46.1 R4.6.1 R7.222 R27 R25 R2 R21,7 R25 R2 R21,7 R25 R2 R21,7 R2 R21,7 R2 R21,7 R2 R2 R21,7 R2 R2 R2,7 R2 R2 R2,7 R2 R2,7 R2,7 R2	7,23,24 2-15,18,1 24,29,30 51 5 5		TRAN TRAN TRA DICE DICE	4 . 2 . 1 . 1 		/ 511 /, 511 , 511	160N 160N	<i>N</i>		OROLA OROLA OROLA
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	128. 128. 1400 1914	FILM FILM HG HG H39 D7 -E ALUM	R3.9.3 R20 R8.16.1 24-6.11 R7.222 R2- R27 R25 R2 R27 R25 R2 R27 R25 R2 R21, 2 R25 R2 R21, 2 R25 R2 R25 R2 R25 R2 R25 R2 R25 R2 R25 R2 R25 R25	7,23,24 2-15,18,1 24,29,30 51 5 5		TRAN TRAN TRAN DIGE DIGE CAPP	4 2 3 5 5 5 7 5 7 5 7 5 7 5 7 5 7 5 7 5 7 5		, 511 , 511 , 511 , 511 , 511 , 511 , 21 , 21	160N 160N	<i>N</i>	К-0 Мат Мат Мат Ург Эле	OROLA OZOLA AROLA E. DEOLA LAGUE
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