CHAPTER 4

PRINCIPLES OF OPERATION

CONTENTS

ILLUSTRATIONS

Fig. No.

CHAPTER 4

PRINCIPLES OF OPERATION

INTRODUCTION

1 This chapter describes the principles of operation for the RA1792 HF Communications Receiver. Figure 4-1 is an overall functional block diagram for the receiver which may be divided into four major sections. The RF/IF/AF section, the frequency synthesizer, the display and front panel section, and the power supply. The chapter has been arranged to cover these sections in that order.

RF/IF/AF SECTION

2 The RF/IF/AF section comprises the rf amplifier/low pass filter A1, the first mixer A2, the second mixer A3, and the second IF/AF assembly A4. The input to the RF/IF/AF section is received at the RF IN connector A1J1.

RF Amplifier/Low Pass Filter, A1

3 The incoming RF signal is passed from the antenna connector A1J1 through a protection circuit, an optionally connected RF amplifier and then through a 4-section elliptical low pass filter which has a cut-off frequency of 35 MHz. The RF amplifier may be connected or by-passed by linking. The filter provides the necessary protection to the receiver, from image signals at frequencies between 81.4 and 111.4 MHz; and from signals at the first intermediate frequency of 40.455 kHz. The filter also prevents first local oscillator reradiation from the antenna connection. The circuit diagram is shown in Figure 8-1.

4 The RF amplifier consists of transistor stage Q2-Q3. Linking E7 to E10 by-passes the amplifier. Linking E7 to E8 and E9 to E10 connects the amplifier between the input and the low pass filter.

5 Q1 is normally conductive, holding relay K1A closed. A MUTE input to A1J1 pin C will turn off Q1 opening the relay to disconnect the antenna input from the following stages of the receiver. A signal of greater than 5V rms approximately will also turn off Q1 and open the relay, thus protecting the receiver from large input signals.

First Mixer, A2

6 Figure 4-2 is a simplified block diagram of the first mixer module A-2. It consists of a signal low pass filter, first mixer, roofing filter, first IF amplifier and drive amplifier with its associated filters. The function of this module is to convert the incoming RF signal to the first intermediate frequency of 40.455 MHz, by mixing with the local oscillator frequency 40.605 to 70.455 MHz derived from the synthesizer. The circuit diagram from the first mixer is shown in Figure 8-2.

Signal Low Pass Filter and Mixer

7 The output of the A1 module is connected to the first mixer through a 2 section elliptical low pass filter which has a cut-off frequency of 35 MHz. The mixer consists of T1, Q2, Q3, Q4, Q5 and T3. The mixer output (from T3) is connected directly to the roofing filter FL1 which selects the 40.455 MHz mixing product. The 3 dB bandwidth of this filter is 16 kHz, and defines the widest bandwidth available in the receiver.

Drive Amplifier

8 The mixer drive amplifier comprises transistors Q1, Q6 and Q7. The local oscillator signal from the filter, which may be monitored at TP2, is coupled to the base of amplifier Q1. The output of Q1, which may be monitored at TP3, drives the differential amplifier stage Q6 and Q7. The output of this stage, through transformer T2, is the LO input to the mixer.

Output Amplifier

9 The mixer output, through filter FL1 and impedance matching transformer T4, drives the high linearity amplifier stage Q8. The output to the following second mixer stage (through A2J3) is taken from a tap on transformer T5, which is in the load circuit of Q8.

First IF AGC

10 The AGC input, through A2J2 pin 6, controls the current through the gain control diode CR1. Thus, the AGC input controls the load impedance and consequently the gain of Q8. The bias signal, through A2J2 pin 5, controls the bias on Q8. This varies the bias as the gain is varied (by the AGC input) so that sufficient current flows through Q8 to assure high amplifier linearity.

Second Mixer, A3

11 The second Mixer, A3, contains three amplification stages, filtering and a mixer. The circuit is shown in Figure 8-3.

12 Figure 4-3 is a simplified block diagram of the second mixer. The 40.455 MHz first IF output from the first mixer is amplified and applied through a 40.455 MHz bandpass filter to a balanced mixer where it is mixed with the 40 MHz output from the LO/BFO synthesizer board. The second IF is produced by selecting the 455 kHz difference frequency at the output of the mixer.

13 The output signal level from the first stage of IF amplification is controlled by the AGC input from the main IF/AF board. The output from the second stage of IF amplification is applied to the balanced mixer through a 40.455 MHz band pass filter. The 455 kHz difference frequency at the mixer output is filtered and amplified before being applied to the MAIN IF/AF module A4.

Amplifier Stage

14 The 40.455 MHz first IF output from the first mixer is applied to an amplifier stage, Q1 via board pin E1 and C3. The amplified output from the Q1 load transformer T1 is applied via C9 to a second amplifier stage, Q2.

Second IF AGC

15 The AGC voltage input, coming in through A3J1 pins 2 and 4, is applied to a circuit consisting of U2A, U1A, B, C which converts a linear voltage charge to a logarithmic current charge to drive pin diode CR1. The diode controls the gain of amplifier Q1. This circuitry is similar to that described in paragraph 10.

16 The AGC current drive for the first mixer is derived from stage U1D and comes out of A3J1 pin 6, while the bias signal for the first mixer is derived from stages U2B and U2C and comes out of A3J1 pin 3.

Mixer

17 The first IF signal from Q2 is applied to the signal port of the mixer U3 via a four section band pass filter tuned to 40.455 MHz. The 40 MHz second LO signal from A8 is applied via J2 to the mixer oscillator port. The difference signal at 455 kHz is selected at the mixer output by the tuned transformer T2 and the ceramic bandpass filter FL1. The output amplifier U4 provides a low impedance signal feed to the MAIN IF/AF module A4.

Main IF/AF Module A4

18 The Main IF/AF module A4 contains the 455 kHz filters used to determine the reception bandwidths, the second IF amplifier, the AM, FM, and Product detectors with associated AF power amplifiers, together with the IF output and AGC circuits.

19 Solid state switching circuits are also included for filter selection, detector selection, AGC time constants, remote gain control and signal level monitoring.

20 Provision is also made for the necessary signal and control inputs to the optional ISB IF/AF module A5 when this faciltiy is required.

21 Figure 4-4 is a simplified diagram of A4 and figure 8-4 is the circuit diagram.

IF Filters

22 The main IF/AF module will accommodate up to seven filters, five of these are normally symmetrical filters and two are sideband filters. When the 16 kHz bandwidth is selected these filters are bypassed and an attenuator is switched in to compensate for gain changes. When the 3 kHz bandwidth is selected the USB filter FL2, is switched in and the 1st LO synthesizer and bfo are offset by 1.7 kHz to make the USB filter appear symmetrical about the receiver frequency (unless optional 3 kHz symmetrical filter is fitted).

23 Filters are selected by the binary coded logic inputs to A4J2 pin 35 (DB0), pin 31 (DB1), pin 33 (DB2) and pin 37 (DB3). These logic inputs are applied through voltage level shifter, U3, to a latch, U2, and then to the one of eight decoder, U1. The latch is set or clocked by the input to A4J2 pin 29 (OP3C) through the level shifter, U16. The outputs from U1 and the output from pin 1 of the latch, U2, selects the appropriate filter by applying a +15 volt bias to the diode switch to select a filter and 0V to switch off the other filters.

24 The output of filter FL1, when selected, may be sent to the main IF/AF signal path or the ISB IF (through J3 out) path (in the optional A5 card) by connection of link LK1 for the SSB or ISB mode.

Input Amplifier

25 The source impedance of the signal from the selected filter is transformed from 5K ohms to about 200 ohms by Q1 and the signal is then applied to an integrated circuit gain-controlled amplifier, U8. This device contains two amplifier sections which are connected in cascade to provide high gain and AGC range. The input signal is applied via C33 to pin 1, and the output from the first section, at pin 12, is applied via R39 and C40 to the input of the second section at pin 10. The output taken from pin 7 is applied via a bandpass filter to an emitter follower, Q6 and also to the IF output amplifier composed of Q7, Q8, Q9, and from there to the back panel IF OUT jack, J4 at a level of 100 mV.

26 AGC is applied to both sections of U8 via pins 3 and 4, thus providing a control range of approximately 60 dB. The three terminal regulator U6 serves to stabilize the supply of U8 at 12 volts.

SSB Detector

27 The IF output from U8 and the bandpass filter is fed via emitter follower stage Q6 to the IC product detector U20. The BFO (455 + 8 kHz) signal from A8 is also fed to U20 via A4J5, the RF switch (CR22-CR25), when selected in other than the AM or FM modes, and U18. J6 out supplies a similar BFO signal to the optional A5 ISB module. The resulting beat difference output frequency at AF from U20 pin 6 is fed to the FET switch, U19A. The BFO output, through the RF switch, is selected by the binary coded logic input to A4J2 pin 39 (DB6).

AM Detector

28 In the AM, FM mode, the binary coded logic input to A4J2 pin 40 (DB7) allows the RF switch to pass the IF signal from Q6, through CR25 into limiter amplifier U18. The output from pin 10 of U18 feeds the carrier input, pin 8, of AM detector module U20. The IF input, from Q6 is also fed into the signal input, pin 1 of U20. The detected AF output from pin 6 is fed to the FET switch U19A.

FM Detector

29 In the AM, FM mode U18 also performs FM detection on the IF input (through the RF switch) yielding the AF output from pin 1 which is fed to the second input of the analogue switch, 19A.

Detector Selection

30 The required signal detector is selected by the application of a binary coded logic input to A4J2 pin 33 (DB2), through U3 and U23 (providing voltage level shifting and latching) which drives the analogue switch U19A. The latching of U23 is clocked by the OP3F input to A4J2 pin 25.

Audio Frequency Stages

31 An audio cross point switch, U25, is used to switch the detected audio from the main IF/AF and ISB IF/AF boards to the appropriate audio outputs (the Loudspeaker and monitor line outputs on the main IF/AF board and the LINE 1 and LINE 2 outputs on the ISB IF/AF board). In a receiver without the ISB option only one line output is provided (the monitor line) and the line level is adjusted using R129. In an ISB receiver there are three line outputs, all of which carry the same signal except when an ISB mode is selected. In this case the upper sideband is fed to the LINE 1 output and the lower sideband to the LINE 2 output. The signal at the monitor line output depends on the sideband selected for monitoring on the front panel. R129 adjusts the level on LINE 1 and R132 adjusts the level on LINE 2. The output on the monitor line is equal to that on the line being monitored. Switching of the cross point switch is controlled by the microprocessor data bus.

32 A dual audio amplifier, U26 provides the loudspeaker and monitor line outputs. The input to the loudspeaker amplifier is set by the VOLUME control mounted on the front panel.

AGC Detector and Amplifier Stages

33 The IF signal from the emitter follower Q6 feeds the U10 transistor array connected as a detector. U10B compensates the bias of U10C for temperature changes. The output from U10C feeds the AGC integrator U14A through one of two paths (Q4 controlled on or off by Q5 or U7C in series with switch U11B), dependant on whether carrier or peak signal AGC is selected. Q5 is controlled by the binary coded logic

input into A4J2 pin 39 (DB6) through U5 and U15. U11B switch is controlled by binary coded logic input into A4J2 pin 38 (DB5) through U5 and U15. Latch U15 is clocked by the OP3D input to A4J2 pin 27. The output from the integrator U14A goes through the AGC filter, which is set for carrier or peak signal AGC through U12C. The filtered output goes through stage U17B and on to control the gain of the IF AGC amplifier, U8. This output also goes on to stage U17D, where it is combined with the ISB AGC input (from A4J8 pin 1 through stage U17C). The output of this stage goes out of A4J2 pin 34 to the second mixer module, A3.

34 Three alternate AGC time constants are provided together with AGC 'hang' and 'dump' capabilities. These time constants are selected by the appropriate parallel combination of R52. R53 and R55, R53 and R55 are switched in or out by FET switches U11A and U12A. The switches are controlled by the binary coded logic inputs (through latch U13) on A4J2 pins 31 (DB1) and 35 (DB0). U12A ON selects short, U11A ON selects medium and both OFF select the long time constant. Latch U13 is clocked by the OP3D input to A4J2 pin 27.

35 When selected, the AGC 'hang' circuit disconnects R52, R53 and R55 from the decay circuit by cut-off of transistor U10D. This transistor is driven by 'hang' circuit stages U7A and U7B. Capacitor C42, through U7A, charges when a large enough signal is received from the AGC detector. The voltage on C42, through U7B, cuts off U10D when the signal is removed. This causes the AGC to 'hang' until C42 discharges. Transistor Q2, connected across C42, disables the 'hang' circuit when switched into the conducting state by the binary coded logic signal from A4J2 pin 38 (DB5) through U4 and U5. Latch U4 is clocked by the OP3C input to A4J2 pin 29.

36 When a 'dump' command is received at U4 pin 1 the Q output of U9A is clocked to a '1' turning on U10c and U12d. This causes the agc voltage to decay rapidly until comparator U7a detects a signal at the IF output. This resets U9A and turns off U10e and U12d.

Manual/Remote IF Control

37 When Manual gain selected, FET switches U12B and U11C are turned ON by the binary coded logic inputs to A4J2 pins 36 (DB4) and 37 (DB3) through latches U15 and U13. This allows the IF gain control voltage from the front panel (through A4J2 pin 22) to set the gain through stages U14C and U14A. Latches U13 and U15 are clocked by the OP3D input at A4J2 pin 27.

38 The output of the DAC, U21, is used to control the receiver gain when the receiver is under remote control by switching on U11d. The DAC voltage is stored by the sample and hold circuit consisting of U14C, U11d, R71 and C54 while the DAC is performing the receiver metering functions. When the receiver is under agc control the DAC is used to hold the output of U14C at 0V and also to set the agc voltage on TP9 to 10V when no signal is present.

Meter Circuits

39 The main IF agc, ISB IF agc and detected AF level are compared with the DAC output voltage in comparators U24c, U24b, U24a respectively. The outputs of the comparators are fed to the microprocessor which changes the DAC input data to adjust the DAC voltage until it is approximately equal to the voltage being compared. Thus the processor is able to measure the RF and AF levels and display the result on the front panel meter.

FREQUENCY SYNTHESIZER SECTION

40 The frequency synthesizer section consists of the first LO synthesizer module (A7) and the second LO/BFO synthesizer module (A8). Paragraph 41 describes the first LO synthesizer module, and paragraph 47 describes the second LO synthesizer module.

First LO Synthesizer Module

41 First LO Synthesizer is a VCO single loop synthesizer with an output frequency of 40.605 to 70.455 MHz in 10 Hz increments. The basic synthesizer circuits are shown in simplified block diagram Figure 4-5.

Simplified Block Diagram Description

42 The Voltage Controlled Oscillator generates the basic frequency which is applied to the first mixer module (A2) and to the divide by N circuit. The value of N is determined by the digital control logic, which in turn is controlled by the frequency selection inputs. The output of the divide by N circuit is applied to a phase comparator, which generates an output based on the phase difference between the divide by N signal and the reference signal. The phase comparator output is combined with additional frequency selection information from the digital control logic filtered and applied as a control voltage to the VCO.

43 A change in the value of N will change the value of the output frequency F_o by an amount equal to the reference F_r. For example, if F_r is 100 kHz and N is 10, then the output frequency F_o will be 1 MHz. If N is changed to 11, then, in order to maintain F_d at 100 kHz, the value of the control voltage will have to change in a direction and by an amount such as to adjust the frequency F_o of the VCO to 1.1 MHz.

44 For output frequency changes in less than 100 kHz increments (the value of F_r), the value of N is changed for brief periods of time. In order to more clearly understand the circuit operation, it may be helpful to assume that the control line to the VCO is disconnected, that F_o is 10.1 MHz, and N has a value of 10. Under these conditions, F_d is 101 kHz, and therefore not equal to F_r (which is 100 kHz). Therefore, a phase error will be detected by the phase comparator. For each period of F_r, F_o will produce 10.1 pulses (instead of 10) and will therefore advance in phase by 0.1 of a cycle. Thus, after 10 periods of F_r, F_o will have produced 101 pulses and will have advanced in phase by one complete cycle. Throughout this time, F_d will be advancing on F_r and the control voltage of the phase

comparator will continue to increase. If the control line were reconnected to the control input of the VCO this signal would of course tend to adjust F_o until it was exactly at 10 MHz.

45 The digital control unit is used to operate when F_o has advanced by one complete cycle to remove or absorb one complete cycle of F_o. This simultaneously adjusts the phase of F_d and brings F_d into phase with F_r. The output of the phase detector thus falls to zero.

46 Since frequency F_o is still at 10.1 MHz, the phase error between F_d and F_r will start again to build up and the value of the VCO control signal will increase once more, until, after a further 101 cycles of F_o (ten cycles of F_d), the digital control unit will once again absorb once complete cycle of F_o, eliminating the phase difference, and dropping the VCO control voltage to zero. The net effect of this circuitry is that a sawtooth waveform is produced as the control voltage to the VCO.

Second LO/BFO Synthesizer

47 This board contains the 5 MHz internal reference oscillator, the 40 MHz second LO and the 455 kHz BFO synthesizer circuits, together with the links and switching circuits necessary to enable the operation from, or the provision of, an external reference frequency of 1, 5 or 10 MHz. A 1 MHz reference output is also provided to the first LO synthesizer module A7. The block diagram is shown in Figure 4-6 and the circuit diagram in Figure 8-8.

Reference Oscillator (TCXO Optional)

48 Y1 is a temperature compensated crystal oscillator (TCXO) operating at 5 MHz. The power supply to Y1 is regulated by U1 and can be switched off via transistor Q1, when operation from an external reference signal is required, by ungrounding the /INT input (switch S2 set to EXT position).

49 With Y1 active, the 5 MHz reference signal is applied to the digital phase comparator U3 via the transistor switch Q5 and TTL shaper Q6. At this time, Q4 is made inoperative by the ground on the /INT line, and diode CR2. When operating from an external source Y1 and Q5 are turned off; Q4 is turned on.

40 MHz Crystal Oscillator/Phase Locked Loop

50 U22D operates as a crystal controlled oscillator in conjunction with crystal Y2. The oscillator frequency can be varied over narrow limits by the application of a d.c. control voltage to varactor diode, CR4. The oscillator is phase locked to either a 1 MHz, 5 MHz or 10 MHz reference signal as described in the following two paragraphs.

51 The 20 MHz oscillator output is fed to buffer U22A and isolation amplifier Q10, to divider chain U7, which is capable of dividing by either 20, 4 or 2. The division ratios are selected for the phase comparator reference and external reference output frequencies by using IC switches U4 and U5 and suitably linking LK1 and LK2. (For 1 MHz connect LK1 and LK2, for 5 MHz connect LK2 only, for 10 MHz connect LK1 only).

52 The divided output is applied to the digital phase comparator U3 together with the internal (or external) reference frequency. The phase comparator outputs are fed to a digital to analogue converter circuit Q7, Q8 and Q9 which provides a smooth d.c. control voltage to the oscillator varactor diode CR4 so as to phase lock the 20 MHz oscillator to the reference signal.

53 The 40 MHz output is provided by the frequency doubler stage, consisting of Q11, L9 and L10, through J3 to the second mixer on A3.

Reference Input/Output

54 The reference frequency output is amplified and buffered by Q3, Q2 when the internal reference oscillator is in use. When an external reference is employed the output impedance of this buffer serves to provide a 50 ohm termination for the external source.

Beat Frequency Oscillator

55 The required 455 ±8 kHz BFO frequency is derived from a single PLL synthesizer tunable in 10 Hz increments and locked to the reference frequency.

56 Q18, Q19 and associated components form a voltage controlled oscillator operating at 50 times the required BFO frequency in the range 22.350 MHz to 23.150 MHz.

57 The output of Q19 is buffered by Q20 and fed to an integrated circuit U20, fixed divide by 50, and is also fed to a programmable divider chain U14 to U19.

58 The fixed divider, U20 provides the required output frequency in the range 455 ±8 kHz to A4 while the output from the variable divider serves as one input to the phase comparator U10. The second (reference) input to the phase comparator is derived from the fixed divide by 2000 U8, and U9, operating with a 1 MHz input and an output of 500 Hz.

59 The phase comparison frequency is 500 Hz, thus enabling the VCO to be phase locked in discrete 500 Hz increments over the operating range, depending on the selected division ratio of the variable divider.

60 The particular division ratio required in the range 44,700 to 46,300 Hz is selected by BCD inputs from the control module, A9.

61 The phase comparator outputs are fed to digital to analogue converter circuit Q15, Q16, and Q17, which functions to provide a smooth d.c. control voltage to the oscillator varactor diode CR7 in such a manner as to phase lock the oscillator to the chosen multiple of the reference frequency.

62 The subsequent division by 50 in U20 provides the required BFO output signal, variable in 10 Hz increments over the range 447 - 463 kHz.

CONTROL SECTION

63 The control section comprises the microcomputer module A6A2, the receiver control module A9, and the optional rear panel interface module A6A1. Figure 4-7 is a simplified block diagram of the control section.

64 The overall operation of the RA1792 is controlled by the Central Processing Unit (CPU), an 8-bit integrated circuit computer. The microprocessor operates according to the Control Program, permanently stored in a Read Only Memory (ROM), and uses Random Access Memory (RAM) for temporary data storage (scratch pad). The CPU addresses the memory via the Memory Interface, a special large-scale integrated circuit, in order to fetch instructions and data.

65 Under the direction of the Control Program, the microcomputer controls specific functions within the RA1792, including:

(a) Display of information on the front panel.
(b) All data supplied to the receiver circuits.
(c) Memory retention of the receiver settings during power failure.
(d) Initialization of circuits following application of power.
(e) Interface with remote controller.
(f) Interface with local controls on front panel.
(g) Monitoring and display of receiver status.

66 A continuous sampling/enabling process sequentially presents data inputs and outputs for receiver control. This sampling/enabling process, encompassing control and monitor functions, is accomplished either on demand or at regular intervals as specified by the CPU. When there is a change in some front panel or remote control setting, the CPU detects this change and presents instructional data to the control circuitry of the synthesizer and RF paths, as well as presenting data to change the front panel display settings.

Detailed Circuit Description, Microcomputer, A6A2

67 The Microcomputer Module, A6A2, contains the CPU, the memory, input/output (I/O) expansion circuitry and the power on/power fail master reset system. The 3850 CPU manipulates data, provides both arithmetic and Boolean logic operations, performs data routing and memory address and I/O operations, under real time control. The memories are addressed by the CPU through the 3853 Static Memory Interface (SMI). The ROMC code from the CPU specifies the operation to be performed by the SMI. The Control Program for the CPU is stored in the erasable/programmable read-only memory (EPROM), and a 'scratch pad storage' is provided to the CPU through 256 bytes of random access memory (RAM). The method of communication between the CPU and all other components of the control section is through the bi-directional, 8-bit Processor Bus. The I/O expansion circuitry uses the Processor Bus and the ROMC codes to obtain a Control Bus (IOC) which provides both I/O strobes, the direction data is to go, and which address Processor Bus data is to go to or be obtained from. A Data Bus (IOD) is provided, isolated from the Processor Bus except during I/O operation. The power on/power fail master reset system is used to initialize the microprocessors, and to provide orderly cessation of microprocessor operations in event of Power Failure. Figure 8-6 in the circuit diagram of the Microcomputer Circuit Card Module.

Central Processor Unit, U1

68 Figure 4-8 presents a logical organization diagram of the 3850 CPU, U1. The timing for the entire microcomputer, the 2 MHz Φ output, is generated by Y1, C1 and C2. There are 4 or 6 Φ periods in an instruction cycle; the choice between short or long cycle is made by the CPU and is dependant on the instruction (ROMC) being executed. The instruction cycle control signal, WRITE, defines each machine cycle. The 16 bits of latched I/O data from the CPU, I/O ports 00 to 07 and I/O ports 10 to 17, and the interrupt logic are directly linked to the rear panel interface A6A1 only. The /RESET line is used to disable the CPU to end processing at the completion of a machine cycle. The /RESET is also used to initialize CPU operation. When /RESET is asserted, pulled low, the CPU will execute the program originated at address 0. The data buffers, DB0 to DB7, are the bi-directional Processor Bus. The serial stream of digital operations created by the real time processing of the microcomputer are passed along this 8-bit bus. The five control signals ROMC0 to ROMC5 identify the operations which other components of the microcomputer must perform. The 5-bit ROMC control signals are made available directly to the SMI, rear panel interface, and the I/O expansion circuitry.

System Memory

69 System Memory consists of the 3853 SMI, U2, the EPROMs U5, 6 and 7, the 'scratch pad' RAMs, U8 and 9 and the read/write and memory page control circuitry, U3A, U3B and U13. The SMI generates the 16-bit addresses for the microcomputer in accordance with the ROMC control signal output from the CPU. The top 4 bits of address are ignored. The /MEMW line, when low, specifies that data from the Processor Bus will be read into the RAM at the specified address. The READ line enables decoders U3A and U3B Address bits A11 and A12 specifying the memory device which is to read out to the Processor Bus the contents of a specific address. U13 maintains the correct logic for this address read to Processor Bus operation. Interrupt Request (/INT REQ) are made available to the CPU on the basis of interrupt priority (/PRI IN) at the SMI. This allows for orderly consideration of rear panel interface interrupt requests. Figure 4-10 provides a logic organization diagram of the SMI.

I/O Expansion

70 The I/O data on the Processor Bus is presented in a serial fashion consisting of an I/O address followed on the next execution cycle by the I/O data. The I/O system to the Processor Bus must be capable of holding on to the I/O address so the address and data can be used at the same time. Otherwise the address is a WRITE cycle ahead and gone from the Processor Bus by the time you have the data. The I/O system also instructs in which direction data is to be moved, input to, or output from the Processor Bus. U4, U11A, B, C, U12A, B and D, U13 and U14 provide for simultaneously available address/data and directions. They allow for the rest of the control section to be made up of decoders which address data to a specific Data Bus I/O Port and input or output strobe that I/O Port.

71 On the positive transistion of the clock, CLK (U14-11), the 'Q' outputs of U14 are set to the logic states of the Processor Bus, the I/O port addresses. U11A, U12A, and U11B are used to detect the specific ROMC state for I/O. When an I/O cycle is detected, CLK is then asserted, and the output control (Q5) of U14 and the enable (/G) of U4 are also set high. This isolates the Processor Bus (PB) from the Data Bus (IOD) and prevents U14 from transferring data to the Control Bus (IOC). The next WRITE cycle ROMC code brings low CLK, OC and /G. This causes the inputs of U14 (D0 to D7) to present a high impedance to the Processor Bus and enables U14 to output the address data to the Control Bus. The low on the /G line enables buffer U4 to transfer data bi-directionally between the Data Bus and the Processor Bus. This achieves coincidence of I/O data and address.

72 The direction of data transferred between the Data Bus and the Processor Bus is in accordance with the ROMC code detection. This code is provided by U11B, U11C and U12D. A low on the DIR line of U4 moves the data from the Data Bus to the Processor Bus and asserts the I/O READ strobe. When the ROMC code specifies a Processor Bus to Data Bus transfer, DIR is asserted so that NAND, U11B, /WSTB

strobes serve to enable I/O decoders in unison with the Control Bus addresses. The Control Bus (IOC), /WSTB, and /IO READ are available to both the rear panel interface, A6A1 and the front panel memory board A9A2 modules. The Data Bus (IOD) is available only to the front panel memory board A9A2.

Master Reset System

73 The master reset system is composed of the schmitt trigger, Q1 and Q2, the RAM shutdown timing system, Q4, Q5, R14, C15, Q6, the 2.0 volt RAM power source, BT1, R9, CR3, C16, the battery charging circuit and the switching transistor Q3.

Power Fail/Memory Retention

74 The schmitt trigger, Q1 and Q2, detects voltage variations of the +5 volt unregulated line. The collector of Q2 will go to ground when the power supply +5 volt unregulated line wanders past the trigger thresholds set by CR1 and R5. This asserts the /RESET line of the CPU and instructs the CPU to come to a stop at the end of the next execution cycle, no matter what that cycle is. Because the CPU may still require some memory access from or to the RAMs for that last execution cycle, there is a delay in the switch of the RAMs power source, determined by R14 and C15. When /RESET line is asserted, it proceeds to turn off the drive to Q4 turning off Q5 which lets R15 discharge C15. Once C15 brings the gate of Q6 within 2 volts of ground, the chip enable 2 line (CE_2) is brought low, allowing the V_{DD} to drop to 2 volts. The CE_2 line must be a solid low before the voltage on V_{DD} drops below 4.7 volts. The RAMs receive their 5 volt supply through Q3. When Q3 back biases it leaves an open circuit through C16, causing it to slowly discharge its +5 volts. As C16 discharges CR3 is brought into conduction providing 2.4 volts from BT1 to the RAMs. The battery leakage is greater than the current drawn by the RAMs therefore several months of memory retention is available

Power ON/System Initialization

75 At Power On, the +5 volt unregulated line comes up first which switches Q1 and Q2, bringing the /RESET line high. The CPU now starts the initialization process and executes the instructions located at address zero. /RESET going high turns Q4 and Q5 on. C15 is charged, the gate of Q6 goes negative and CE_2 is asserted, enabling both +5 volt V_{DD} and memory I/O. During the turn on cycle, Q3 will quickly become a saturated transistor and quickly charges C16. R11 protects Q3 from damage during turn on. Once C16 reaches a 4.7 volt charge, CE_2 at the RAMs has gone negative and a +5 volt operation begun. At the same time CR3 is back biased and CR6 and R9 charge the Ni-Cad battery, BT1. If the serial remote control option is installed, the /RESET line is also provided to the UART, A6A1U10, for start-up initialization of the microprocessor.

Front Panel, A9

76 The front panel assembly contains the front panel, the switch and display circuit card assembly A9A1 and memory board A9A2.

Switch and Display Circuit Card Assembly, A9A1

77 The Switch and Display Circuit Card assembly contains the liquid crystal displays (LCD's), their drivers and the switch matrix. Figure 8-9 is the circuit diagram of this assembly. This assembly connects to the memory board through connector W1P1.

78 U1 and U2 are liquid crystal displays. Access to the data bus, DB0 to DB7 (from the memory card), is provided to the LCD meter and mode display by the BCD to 4- or 7-segment decoder/driver circuits U3-U26 and U28. Strobing from the data bus into the latches of the decoder/drivers is provided by U27 (4 bit latch /4- to 16-bit decoder) driven by inputs N0, N1, N2 and N3 and the number display strobe, and display strobes OP32-OP37 (from the memory board). The display oscillator U29 supplies the required difference frequency signal to all decoder/ drivers.

79 The switch matrix SA0-SC7 and SD0 (columns A, B, C and D and rows 0-7) connects directly to the memory board through connector W1P1. The function of each switch is shown in the switch function table. The L/S Phone assembly, Volume Control, IF Gain control and Meter switch are mounted on the front panel and connect to the switch and display circuit card assembly through terminals E1-E10 and then on to the memory board through connector W1P1.

Memory Board, A9A2

80 The memory board interfaces microprocessor A6 to the front panel switch and display circuit card and to circuit cards A1-A4, A7, A8 and A10. It serves to connect the circuitry in these cards to the microprocessor data bus and control lines, under control of the microprocessor. In this manner, functions requested by the front panel controls or the remote controller can be performed by the microprocessor programs. Figure 8-11 is the circuit diagram of the memory board. The microprocessor connects to the memory board through connector W1P1 while the switch and display circuit card connects through connector J2.

Switch Matrix

81 The status of the switch matrix is continually read by the microprocessor, Columns A, B, C and D of the switch matrix are activated, in turn, by microprocessor signals IOC0-IOC2, IOC5 and $\overline{\text{IO READ}}$, through multiplexer U10. The 7 rows of the switch matrix are strobed onto the microprocessor bus (IOD0-IOD7) through buffers U16b and U17a, to be read by the microprocessor.

Display Data and Strobes

82 The display data is transferred from the microprocessor bus to the receiver data bus (DB0-DB7) through latches U19 and U20 by microprocessor signals IOC5 and $\overline{WSTB}$. The strobes for the transfer of data from the receiver data bus to the appropriate display latches are generated by the 4 to 16 line decoder U8, driven by IOC0-IOC5, $\overline{WSTB}$ and timing stages U9a and U9b, and counter U12.

1st LO Synthesizer

83 Connections to the 1st LO synthesizer are provided through connector W5P1*. The serial strobe, serial clock and serial data signals out are generated by flip-flop U4 and gates U5C and U3C. They are then entered on the data bus and strobed by OP31 and OP39, via multiplexer U8.

2nd LO Synthesizer

84 Connections to the 2nd LO synthesizer are provided through connector W2P1. The BFO enable and frequency setting are output through flip-flops U24-U27, entered on the data bus and strobed by OP38, via multiplexer U8.

Main IF/AF

85 Connection to the main IF/AF card are provided through connector W6P1. The data bus and strobe signals OP3A-OP3F from multiplexer U8 are sent to the main IF/AF control circuitry. The IF gain, volume and L/S connections from the front panel are also fed to the main IF/AF through this connector. The scan inhibit, AF comparator, main RF comparator, and ISB RF comparator, from the main IF/AF board together with the meter switch input (from the switch and display circuit card) are strobed to the microprocessor bus for readout, through buffer U15 via output 5 from multiplexer U10. This same strobe, through U17b, strobes the tuning encoder outputs onto the microprocessor bus for readout.

Tuning Encoder Circuitry

86 The tuning knob is coupled to an optical encoder. An enscribed coding disc is attached to the encoder spindle, and rotates over two sets of LED/photo-transistor detectors U29 and U30. As the disc rotates, the detectors generate pulse waveforms that are input for pins 12 and 14 of buffer U17b. Access to the data bus is as described in paragraph 85. Detectors U29 and U30 are physically displaced so that the two outputs are 90° out of phase. Clockwise rotation of the tuning shaft (from the front) causes the output of U28 pin 14 to lead as shown in Fig. 4-11. Counterclockwise rotation causes the output of U28 pin 1 to lead. Resistors R12 and R13 and capacitors C14 and C15 provide a small amount of a.c. and d.c. hysteresis.

* W4P1 on early versions of receiver.

Memory

87 U13 and U14 are two 1024 x 4 bit EAROMs. These provide the channel memory. Data terminals D0-D7 connect to the microprocessor data bus while the address terminals A0-A9 connect to the receiver data bus and the outputs of Counter U12. Reading and writing into and from the EAROM is controlled by microprocessor signals IOC0, IOC1 and $\overline{\text{WSTB}}$, and output 1 of multiplexer U10.

POWER SUPPLY, A10

88 The power supply module includes a power line filter assembly, a power transformer, three rectifiers, and four integrated circuit regulators with associated smoothing and decoupling capacitors. The module can be set to operate with line input voltage of 100, 120, 220, or 240 Volts + 10% - 15% and line frequencies from 45 to 65 Hz. Power is controlled by an ON/OFF switch mounted on the receiver front panel. Figure 8-12 is the circuit diagram.

Power Input Circuit

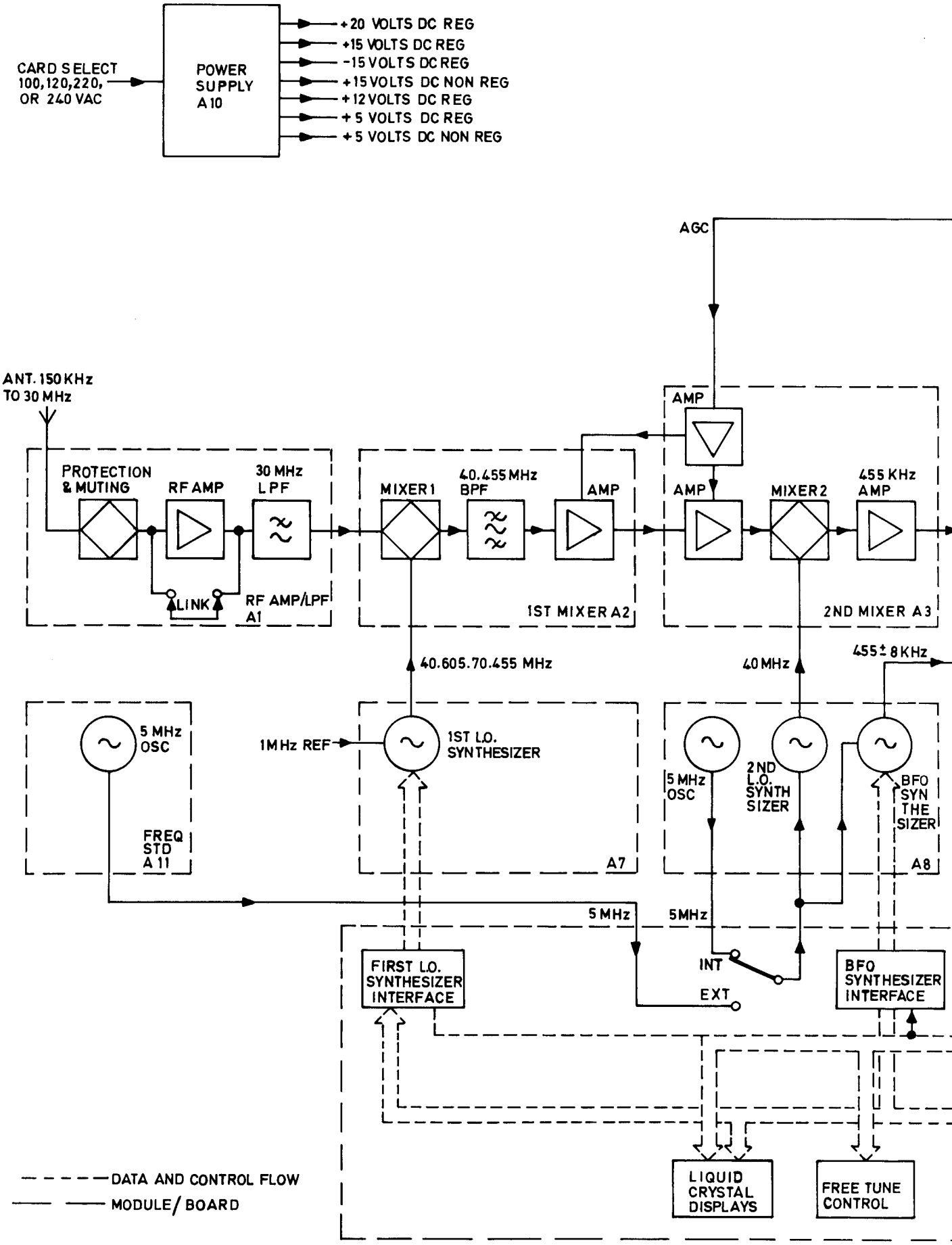
89 Power is applied to the power line filter assembly which includes the connector A10J1, the fuse F1, a line filter and a printed circuit card switch for transformer primary tap selection. The tap selection allows operation from nominal 100, 120, 220 or 240 volt power sources.

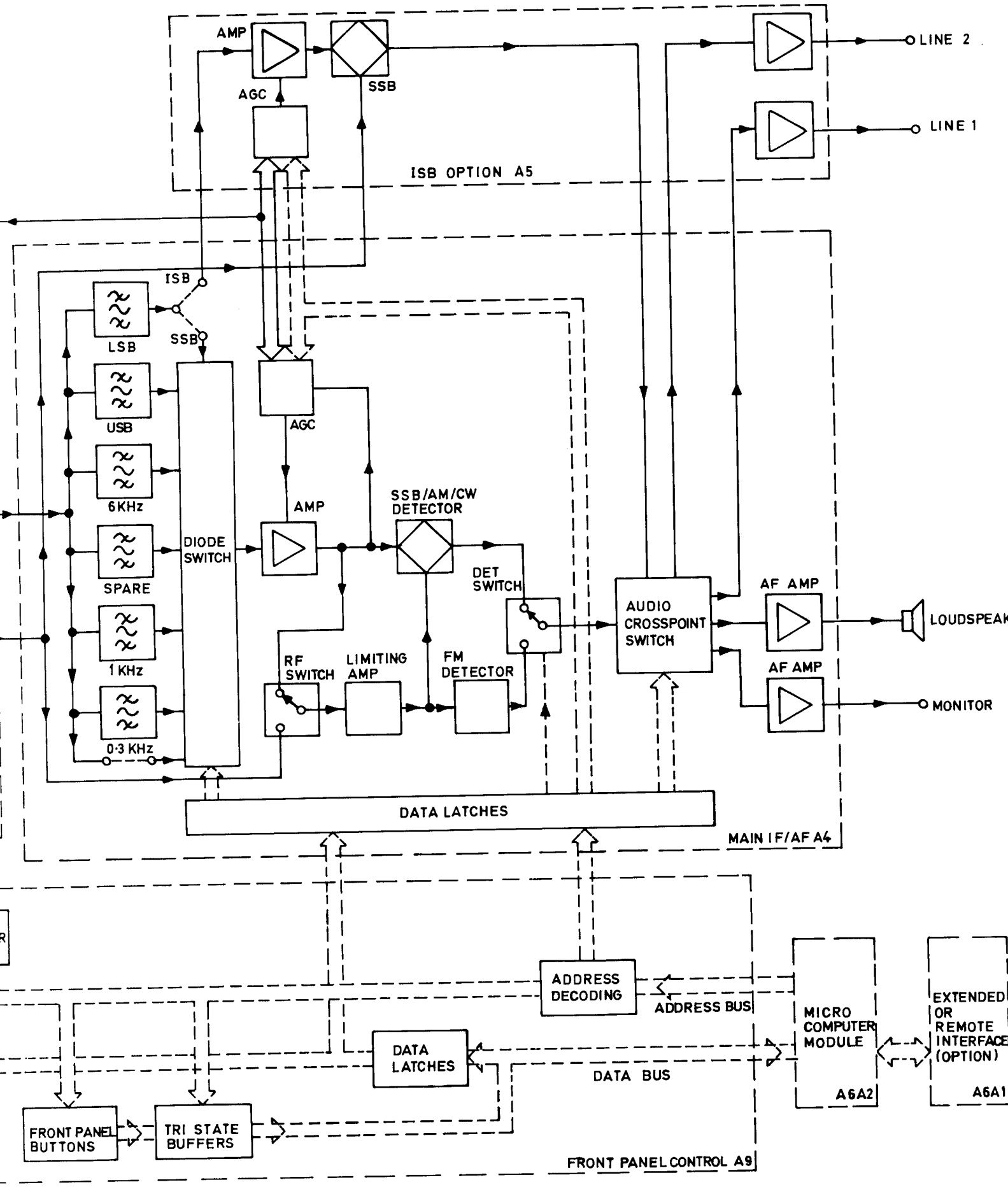
90 Power is provided via A10J2 pins 3, 4, to the front panel double pole ON/OFF switch and returns via A10J2 pins 8-9 to the selected taps on the power transformer A10T1.

DC Outputs

91 Full-wave rectifiers, smoothing capacitors and integrated circuit voltage regulators are employed to provide the required d.c. output voltages of +20, +15, +12, +5 and -15 regulated, and +15 and +5 unregulated for the various receiver modules. The d.c. voltages are supplied through connector A10A1J1.

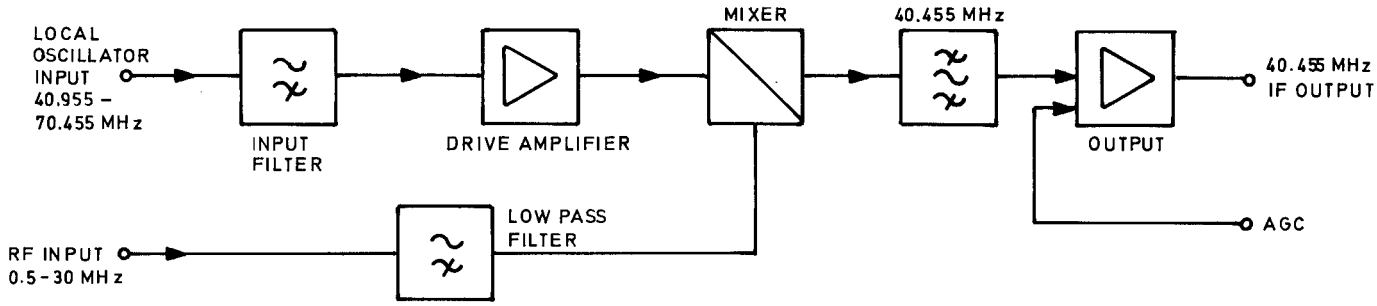
92 Zener diode VR1 provides over-voltage protection for the +5V bus. Capacitors C2, C3, C5, C6, C8, C9, C11, C12, C13 and C14 are fitted adjacent to the repective regulators to suppress possible oscillation. Bridge rectifiers CR1, CR2 and CR3 rectify the a.c. voltage from the secondary taps of T1 while capacitors C1, C4 C7 and C10 provide filtering for the a.c. ripple voltage.


CARD SELECT
100,120,220,
OR 240 VAC
POWER
SUPPLY
A10
+20 VOLTS DC REG
+15 VOLTS DC REG
-15 VOLTS DC REG
+15 VOLTS DC NON REG
+12 VOLTS DC REG
+5 VOLTS DC REG
+5 VOLTS DC NON REG
AGC
ANT. 150 KHz
TO 30 MHz
PROTECTION
& MUTING
RF AMP
30 MHz
LPF
LINK
RF AMP/LPF
A1
MIXER 1
40.455 MHz
BPF
AMP
1ST MIXER A2
AMP
AMP
MIXER 2
455 KHz
AMP
2ND MIXER A3
40.605.70.455 MHz
40 MHz
455 ± 8 KHz
5 MHz
OSC
FREQ
STD
A11
1MHz REF
1ST L.O.
SYNTHESIZER
A7
5 MHz
OSC
2ND
L.O.
SYNTH
SIZER
BFO
SYN
THE
SIZER
A8
5 MHz
5MHz
FIRST L.O.
SYNTHESIZER
INTERFACE
INT
EXT
BFO
SYNTHESIZER
INTERFACE
LIQUID
CRYSTAL
DISPLAYS
FREE TUNE
CONTROL
DATA AND CONTROL FLOW
MODULE/BOARD

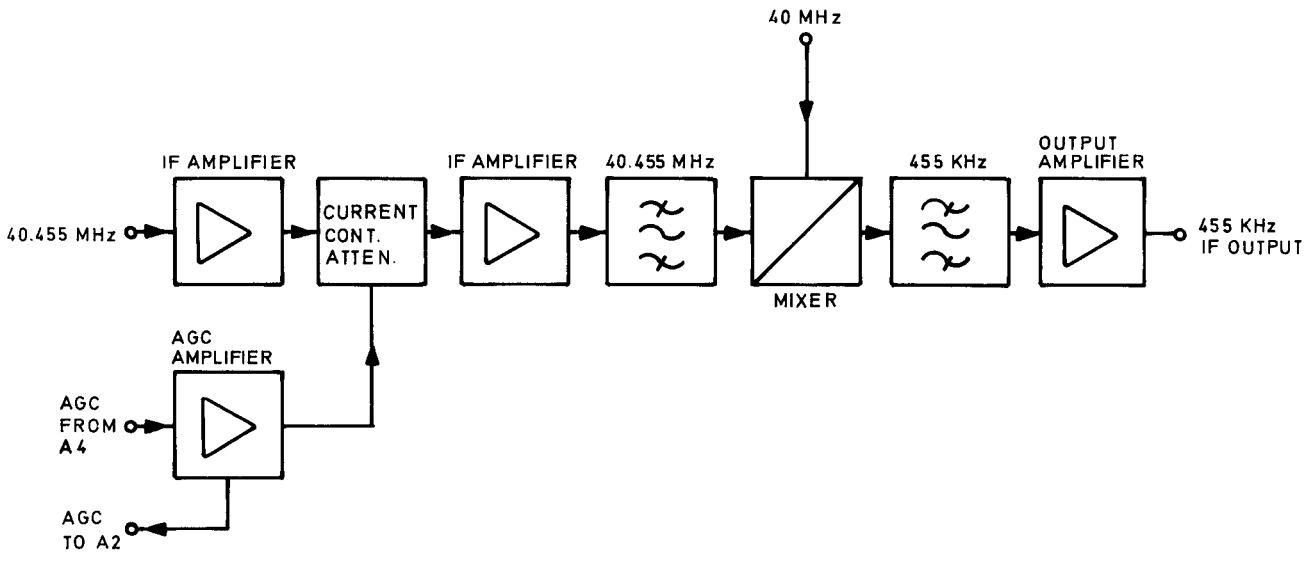


Overall Functional Diagram: RA 1792

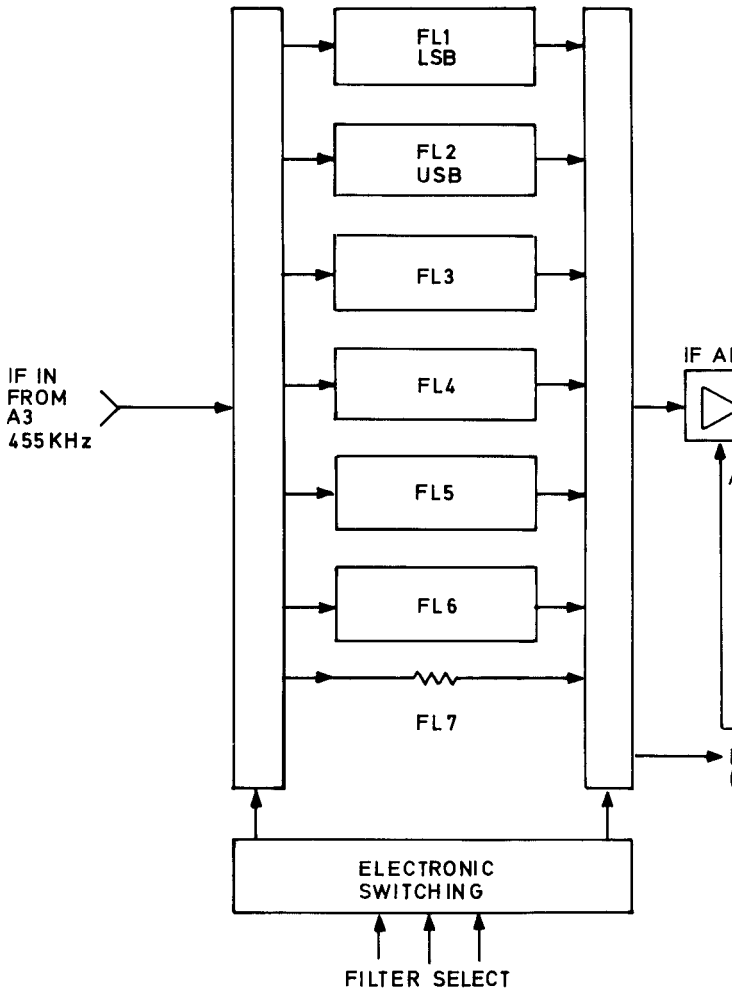
Fig. 4.1

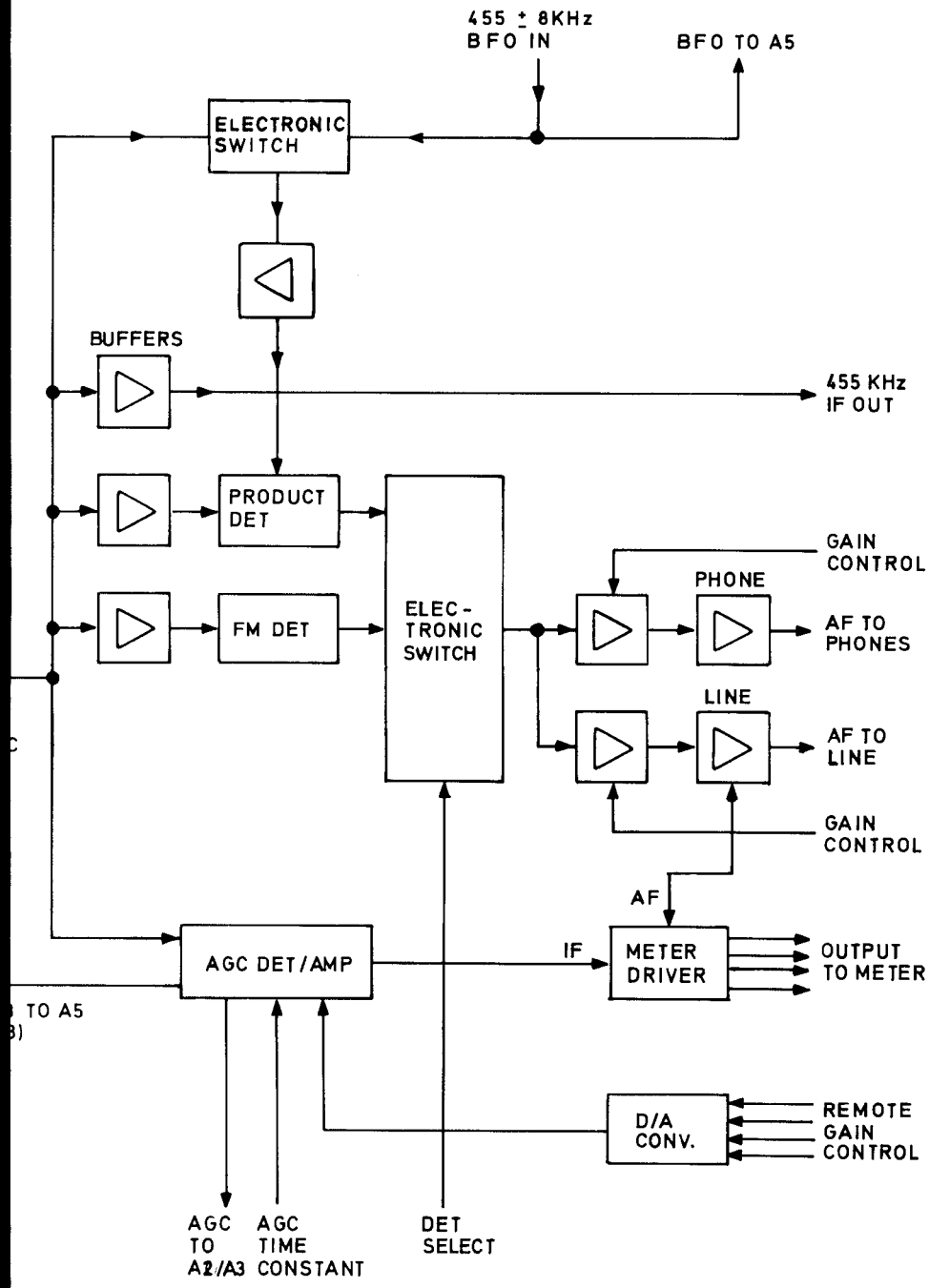


Simplified Block Diagram, First Mixer, A2 Fig.4-2



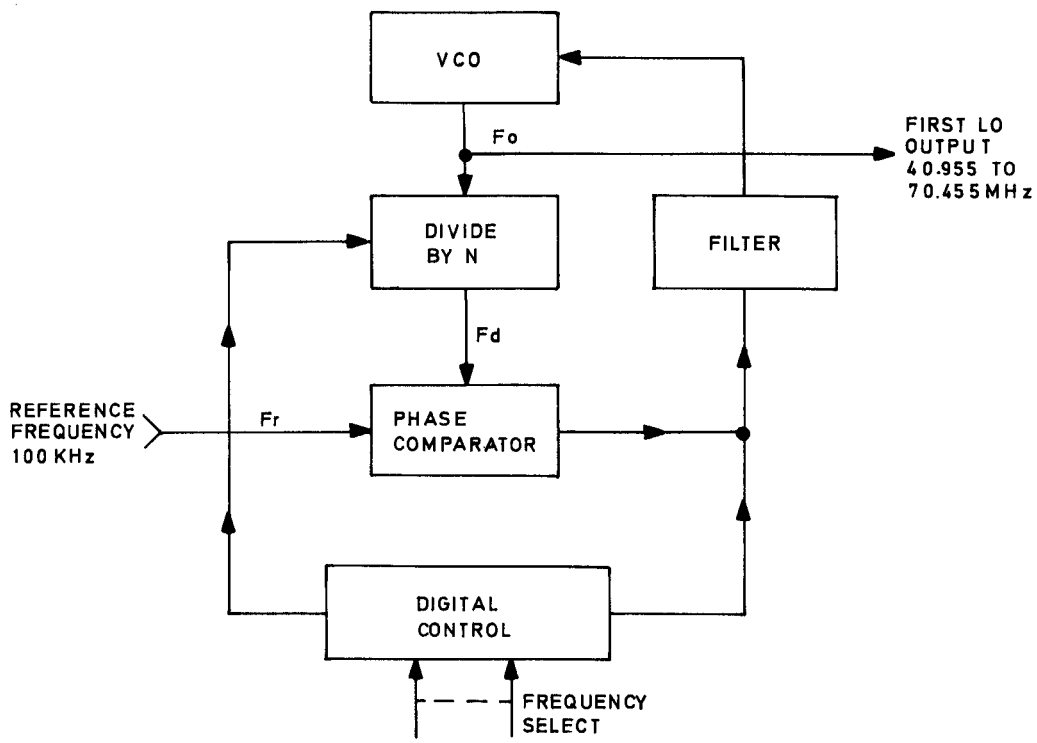
Simplified Block Diagram, Second Mixer, A3 Fig.4-3


FL1
LSB
FL2
USB
FL3
FL4
FL5
FL6
FL7
IF IN
FROM
A3
455KHz
ELECTRONIC
SWITCHING
FILTER SELECT



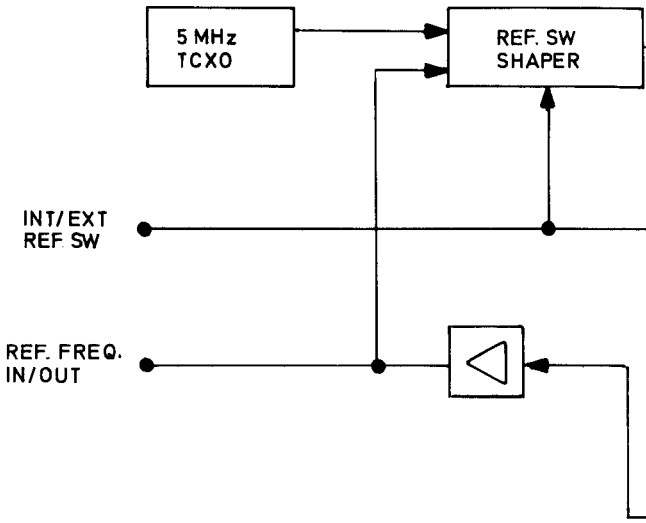
Simplified Block Diagram
Main IF/AF A4

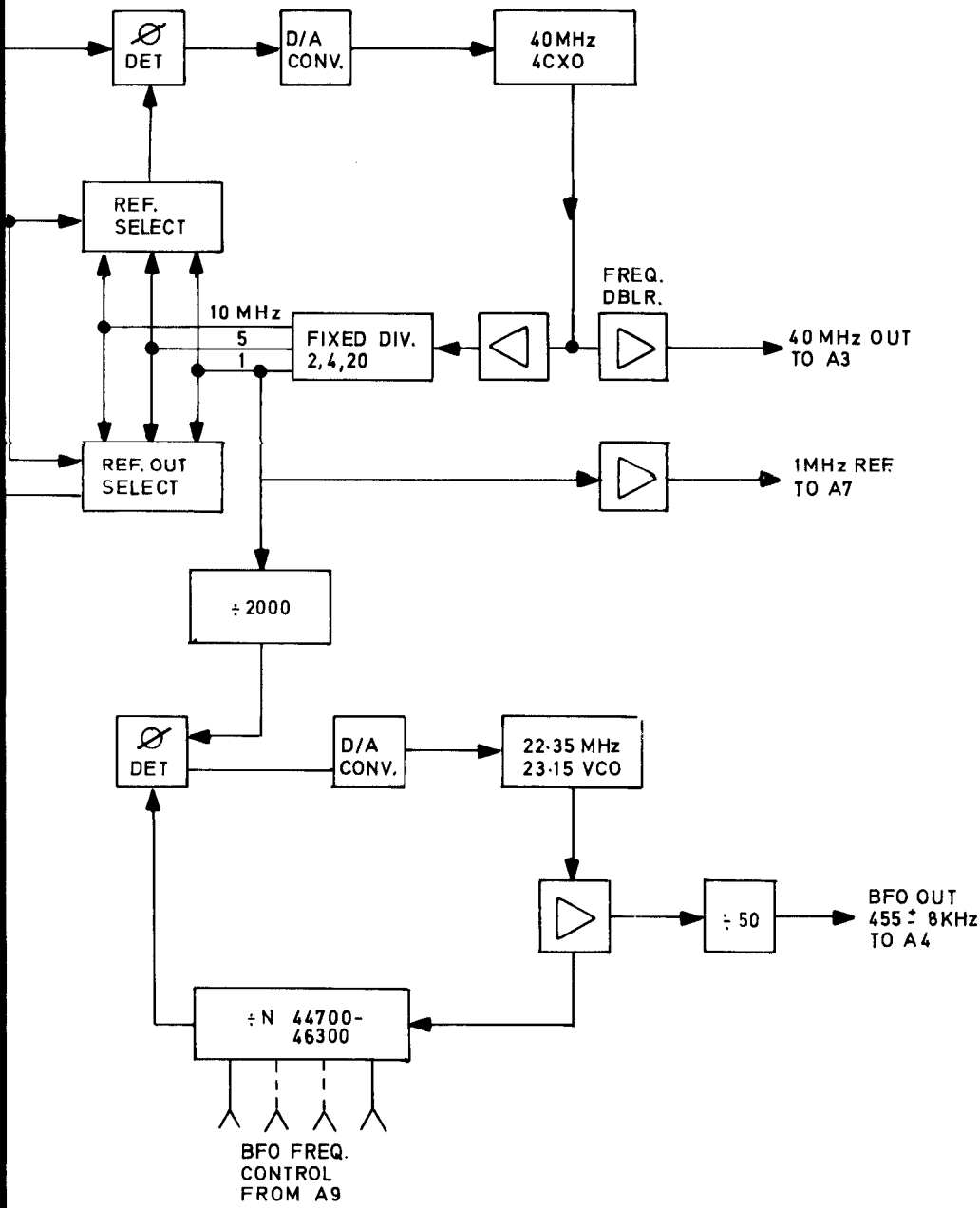
Fig. 4.4



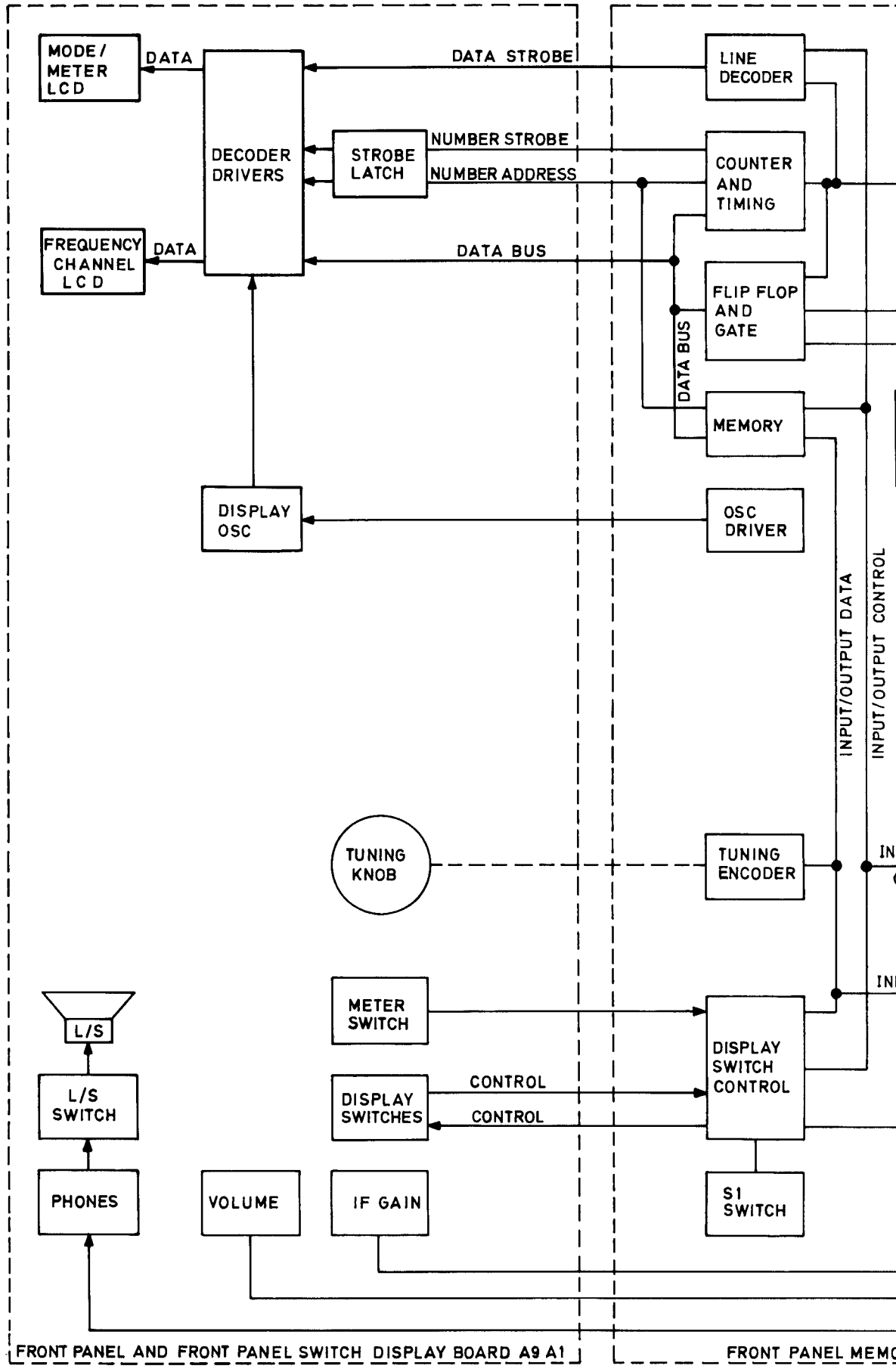
RACAL
TH1496

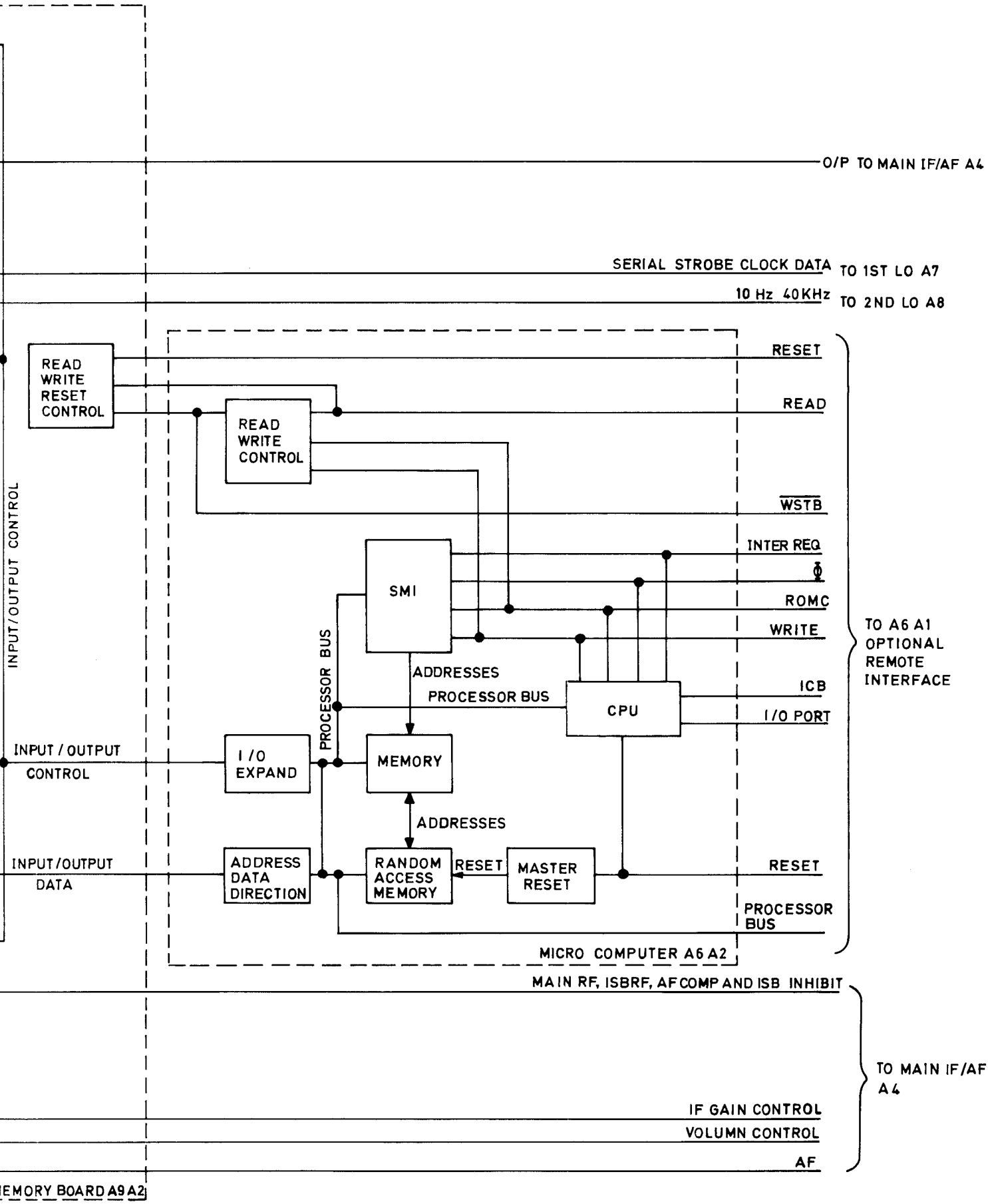
Simplified Block Diagram, First LO Synthesizer Fig.4-5


5 MHz
TCXO
REF. SW
SHAPER
INT/EXT
REF SW
REF. FREQ.
IN/OUT

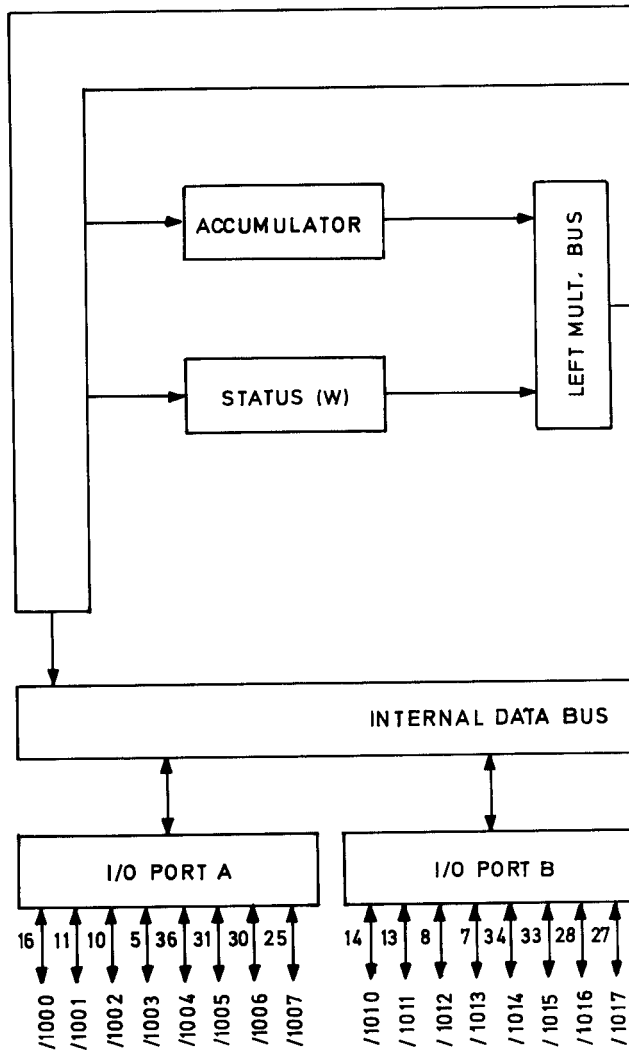


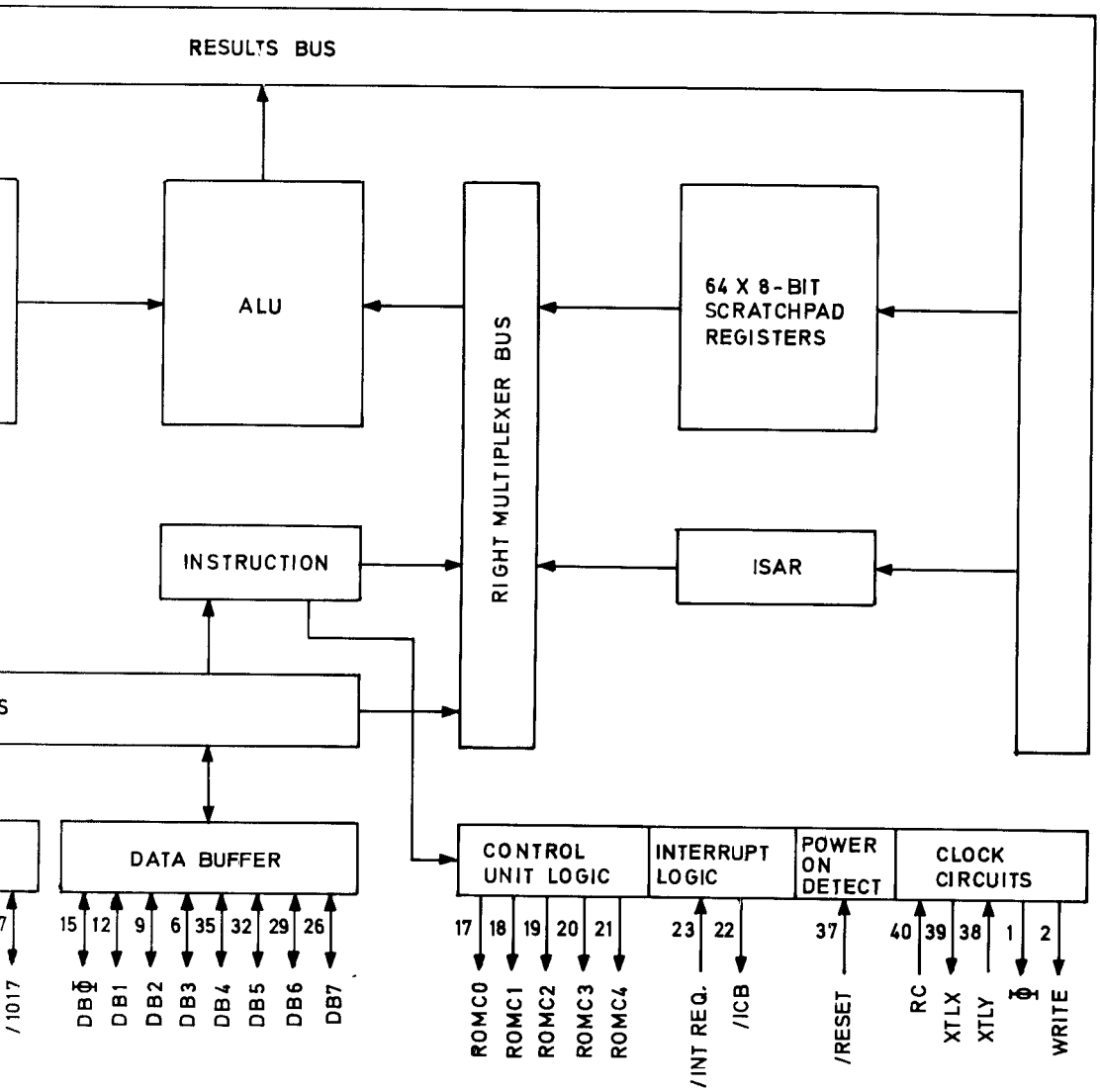
Simplified Block Diagram, Second LO/BFO Synthesizer, A8 Fig 4-6


MODE / METER LCD
DATA
DECODER DRIVERS
DATA STROBE
LINE DECODER
STROBE LATCH
NUMBER STROBE
NUMBER ADDRESS
COUNTER AND TIMING
FREQUENCY CHANNEL LCD
DATA
DATA BUS
FLIP FLOP AND GATE
DATA BUS
MEMORY
DISPLAY OSC
OSC DRIVER
INPUT/OUTPUT DATA
INPUT/OUTPUT CONTROL
TUNING KNOB
TUNING ENCODER
METER SWITCH
L/S
L/S SWITCH
DISPLAY SWITCHES
CONTROL
CONTROL
DISPLAY SWITCH CONTROL
PHONES
VOLUME
IF GAIN
S1 SWITCH
FRONT PANEL AND FRONT PANEL SWITCH DISPLAY BOARD A9 A1
FRONT PANEL MEM



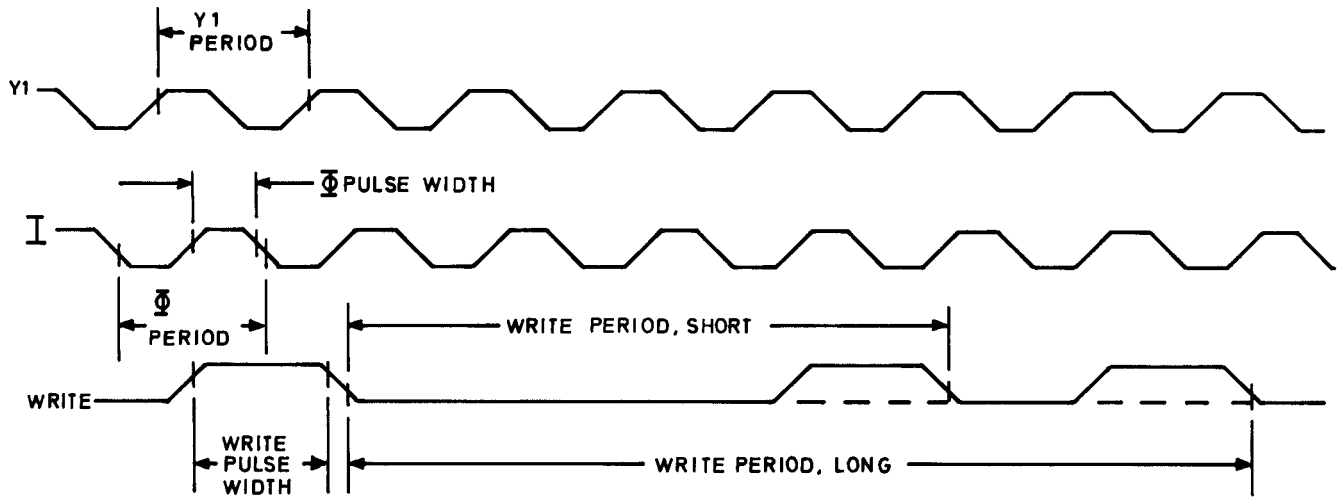
Functional Diagram : Control Section Fig. 4.7


ACCUMULATOR
STATUS (W)
LEFT MULT. BUS
INTERNAL DATA BUS
I/O PORT A
I/O PORT B
16 11 10 5 36 31 30 25
/1000 /1001 /1002 /1003 /1004 /1005 /1006 /1007
14 13 8 7 34 33 28 27
/1010 /1011 /1012 /1013 /1014 /1015 /1016 /1017



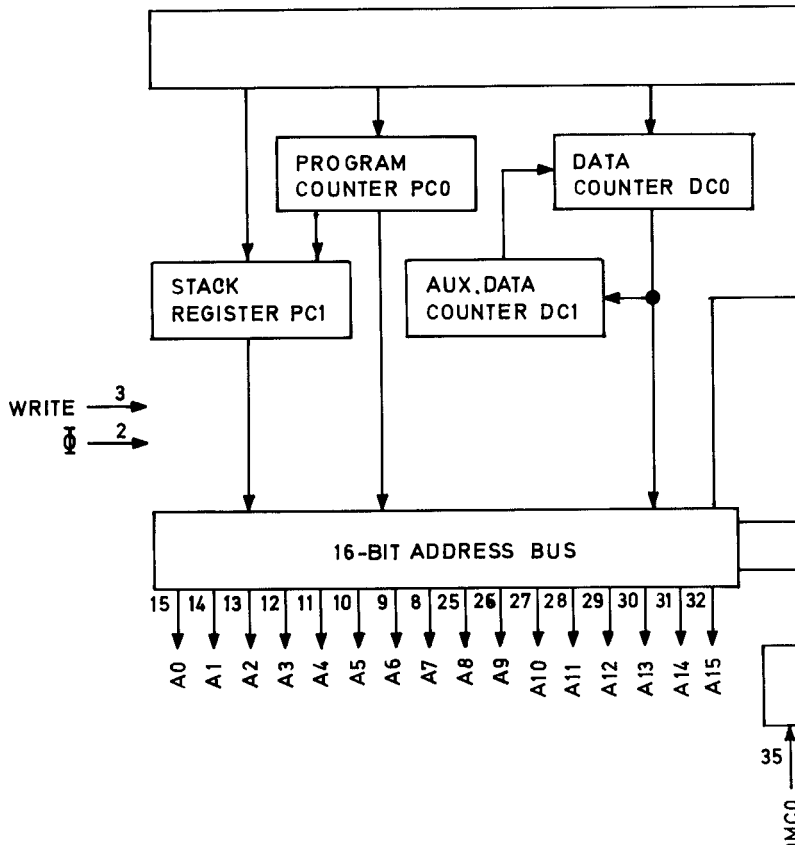
Logic Organisation and Pins for the 3850CPU

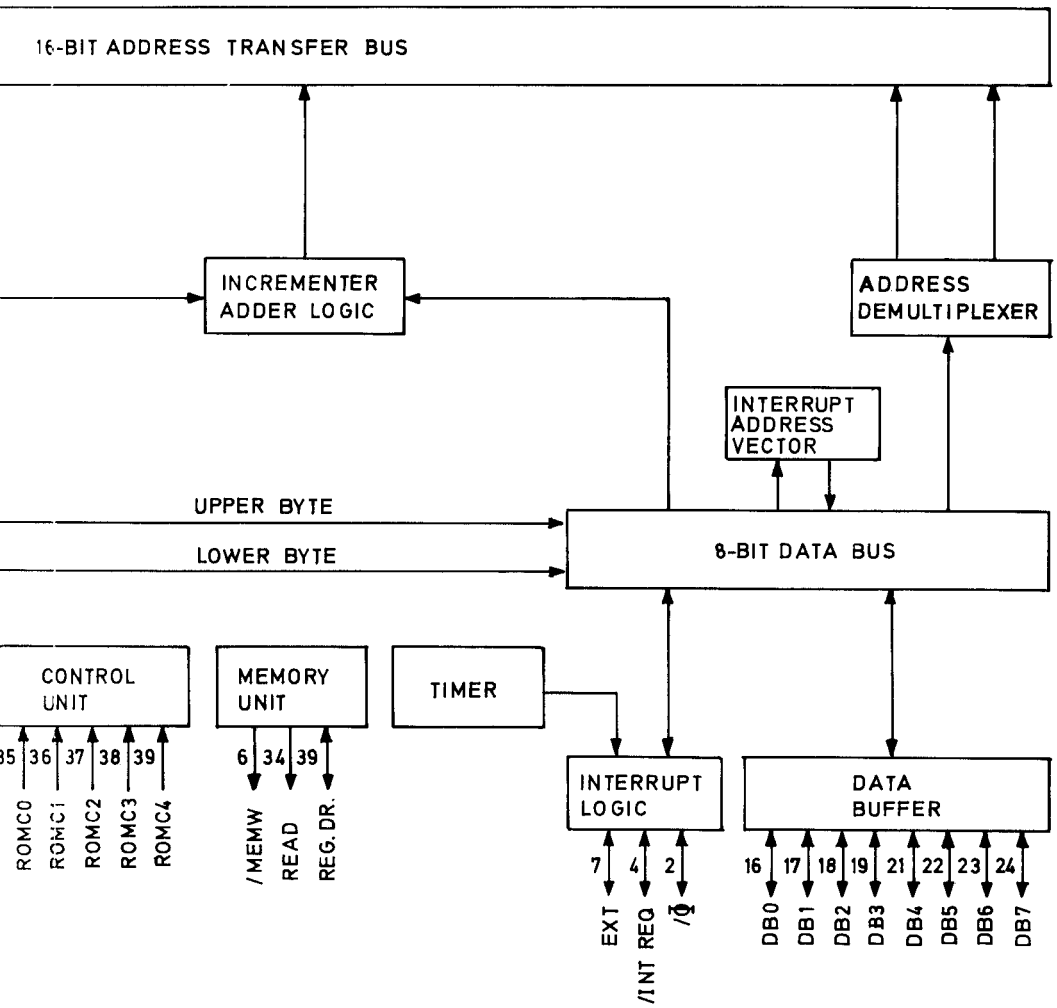
Fig. 4-8



Timing Signal Specifications

Fig.4-9

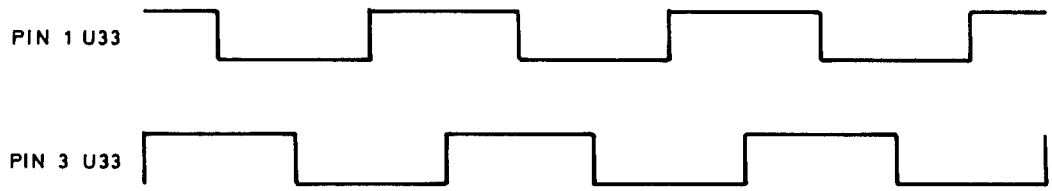

PROGRAM COUNTER PC0
DATA COUNTER DC0
STACK REGISTER PC1
AUX. DATA COUNTER DC1
WRITE
3
Φ
2
16-BIT ADDRESS BUS
15 14 13 12 11 10 9 8 25 26 27 28 29 30 31 32
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15
35



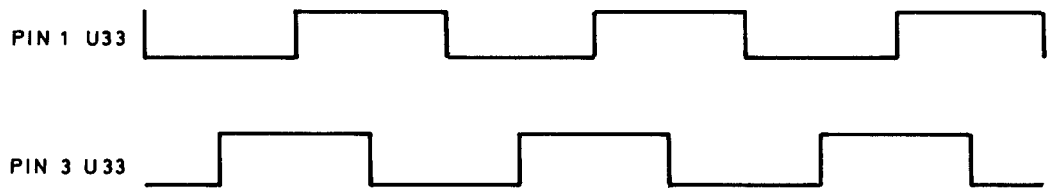
Logic Organisation and Pins for the 3853SMI

Fig. 4.10

CLOCKWISE:



COUNTER-CLOCKWISE:



Encoder Outputs

Fig. 4·11