RA3700 Series
Modular HF Receivers

MAINTENANCE MANUAL

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RA3700 SERIES
MODULAR HF RECEIVERS
MAINTENANCE MANUAL

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PREFACE

SCOPE OF MANUAL

This manual is for use with all receivers and receiver control units in the RA3700 Series.

PRESENTATION OF MANUAL

Information is separated into chapters as follows:

(1) Chapters 1 to 4 contain general descriptive and maintenance information.

(2) Chapter 5 covers both the serial ASCII and IEEE-488 remote interface protocols and includes the complete instruction set of commands required by the receiver for operation in a computer controlled system.

(3) Chapters 6 to 14 are self-contained module chapters for the modules provided with a basic receiver, and include functional descriptions, block and circuit diagrams, parts lists, fault finding and alignment information as appropriate to each module.

(4) Chapters 15 onwards are as above but for optional modules which may be fitted to a receiver.

ASSOCIATED DOCUMENTS

RA3700 Series Modular HF Receivers Operators Manual (Ref. TH 9041).

CHAPTER 1

GENERAL DESCRIPTION

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CHAPTER 1

GENERAL DESCRIPTION

INTRODUCTION

1 The RA3700 Series of receivers is a family of fully synthesised programmable receivers covering the frequency range 15 kHz to 30 MHz in 1 Hz or 10 Hz steps. Reception facilities for CW, MCW, AM, USB/LSB and FM signals are provided as standard with ISB and FSK modes available as options.

2 A conventional tuning knob with selectable tuning rates enables continuous tuning over the frequency range without any need for band changing. Alternatively, instant frequency selection is available using a numeric keypad. A 100-channel, non-volatile memory is provided for storing 100 frequencies and their associated operating settings for instant recall. Facilities for automatic scanning of these preset channels and sweeping of a pre-defined frequency range are also provided.

3 All receivers can be controlled remotely and contain comprehensive built-in test equipment (BITE) facilities, which may be accessed either locally or remotely to enable fault location and subsequent repair to be rapidly carried out.

4 The RA3700 Series includes the following equipments:

(1) RA3701 HF receiver with front panel controls plus local and remote control facilities.

(2) RA3702 dual HF receiver which is effectively two RA3701 receivers in one chassis sharing a common front panel which may be switched to control one receiver at a time.

(3) RA3703 HF receiver which is a remote control version of the RA3701 and intended for operation as a slave receiver.

(4) RA3704 dual HF receiver which is a remote control version of the RA3702 and intended for operation as two independent slave receivers.

(5) RA3705 dual HF receiver which has common frequency synthesisers shared by the two receivers. It is intended for use as a slave receiver in DF systems where a two channel receiver is required.

(6) MA3700 receiver control unit with a receiver front panel for use as a controller for receivers in the RA3700 Series.

5 The receiver is of modular construction with space provided for additional optional modules; details of these are contained in the appropriate module chapter. All external connections except headphones are made at the rear panel, while the front panel provides all the local controls. Front and rear panel views for the various versions are shown in Fig. 1.1 to Fig 1.4.

RA3701 BLOCK DIAGRAM DESCRIPTION

6 The following brief technical description of the basic RA3701 receiver should be read in conjunction with the block diagram in Fig. 1.5. A more detailed description of each module is given in the appropriate module chapter.

RF Input

7 The incoming RF signal is routed via a PROTECTION AND MUTING circuit through a 30 MHz low pass filter (LPF) either side of a wideband RF AMP, which may be bypassed by means of relays controlled by the PROCESSOR via the MODULE BUS INTERFACE.

8 The protection circuit contains a relay which automatically open- circuits the RF path for signals at the antenna greater than approximately +18 dBm, or when a mute signal is applied to the receiver via a rear panel connection or via the remote control interface.

9 The low pass filters protect the receiver from image frequency signals and also attenuate first local oscillator re-radiation from the antenna connection.

First Mixer and IF Amplifier

10 After amplification in the DRIVE AMP, the 41.4 MHz to 71.4 MHz output of the 1st LO Synthesiser is mixed with the received signal in the 1st MIXER stage. The resulting difference frequency of 41.4 MHz is fed as the 1st IF to the AGC controlled 1st IF AMP, via a CRYSTAL FILTER centred on 41.4 MHz. This acts as a 'roofing' filter to establish the maximum bandwidth of 12 kHz for the receiver.

First Local Oscillator

11 The first local oscillator signal is produced by a single-loop synthesiser and is phase locked to a 20 MHz reference signal derived from the Reference/BFO Module. In the synthesiser a voltage controlled oscillator (VCO) generates the basic 1st LO frequency of between 41.4 MHz to 71.4 MHz. The frequency is controlled by a phase locked loop in which the VCO frequency is divided by the PROGRAMMABLE DIVIDER and compared with a 1 MHz reference frequency in the PHASE COMPARATOR. The output of the PHASE COMPARATOR is filtered by the LOOP FILTER and fed back to the VCO to lock the loop.

12 The division ratio of the signal fed back to the PHASE COMPARATOR is determined by the PROGRAMMABLE DIVIDER. This is controlled by a SYNTHESISER CONTROL (LSI) device which is loaded with frequency setting data from the PROCESSOR, via the MODULE BUS INTERFACE, and processes this information in such a way as to obtain a frequency resolution down to 1 Hz.

Second Mixer and IF Amplifier

13 The 2nd MIXER mixes the 1st IF of 41.4 MHz with a 40 MHz signal derived from the 2nd LO output of the Reference/BFO Module. The resulting 2nd IF output of 1.4 MHz is passed through a 1.4 MHz LPF and then amplified in a fixed gain 1.4 MHz 2nd IF AMP prior to being routed to the IF/AF Module. A wideband IF output via a BUFFER AMP is also made available at the rear panel.

Second Local Oscillator

14 The 2nd LO output is produced by a FREQUENCY DOUBLER from the output of a reference generator. This employs a 20 MHz voltage controlled crystal oscillator (VCXO) phase locked to a 1 MHz reference signal which may be derived from either an internal or external source.

15 The user may select the reference source by means of switch No. 1 on top of the Reference/BFO Module, setting it to either INT or EXT. With INT selected and an internal 5 MHz Frequency Standard Module fitted, the frequency standard output is divided to produce a 1 MHz reference for the PHASE COMPARATOR. In this mode a reference output is made available at the rear panel for connection to external equipment. By setting additional switches No. 3 and No. 4 (switch No. 2 not used) according to the positions marked on the switch label, an external reference output frequency of either 1 MHz, 5 MHz or 10 MHz is derived from the LOOP DIVIDER.

16 With EXT selected, an external frequency standard of either 1 MHz, 5 MHz or 10 MHz may be used by setting the switches accordingly. A 5 MHz output is also made available at the rear panel to allow, for example, a dual receiver to operate from a single reference standard.

BFO Synthesiser

17 To enable demodulation of SSB and CW signals, the BFO synthesiser provides an output centred on 1.4 MHz and tunable in 10 Hz steps over the range plus or minus 9.99 kHz. It operates in a similar manner to the 1st LO synthesiser in that it also employs a single phase locked loop controlled by a SYNTHESISER CONTROL (LSI) device. In this loop a 2.5 MHz signal from the reference synthesiser is used to phase lock the 5.6 MHz VCO which is divided by 4 to produce the BFO signal.

IF Filters

18 A FILTER SWITCHING circuit using diodes switched via the MODULE BUS INTERFACE enables the selection of either a filter bypass path or any one output of up to five 1.4 MHz CRYSTAL FILTERS. When the bypass is selected the receiver bandwidth is determined by the crystal filter in the Front End Module as previously mentioned. A typical receiver may contain symmetrical filters with nominal bandwidths of 6 kHz, 1 kHz and 300 Hz,plus two sideband filters of 2.7 kHz each.

AGC Controlled Second IF Amplifiers

19 The selected filter output signal is applied to an automatic gain controlled IF amplifier. The AGC circuits keep the output level constant by controlling the IF gain distribution throughout the receiver. The circuits consist of AGC detectors whose decay times are dependent on the AGC time constant selected by the operator.

Demodulators

20 CW and SSB demodulation is performed by a product detector which mixes the IF signal with the BFO signal. Demodulation of FM signals is performed by a limiter and FM discriminator employing a quadrature tuned circuit. The limiter also provides a carrier signal to the product detector to enable it to demodulate AM signals.

Audio Switching Circuits

21 Depending on the receiver mode selection, the appropriate detected audio output is routed from the DEMODULATORS to the audio output stages via the AUDIO SWITCHING circuits. These circuits switch the audio to a line amplifier to provide a 600 ohm output at the rear panel, and to the AUDIO AMPLIFIERS in the Front Panel Assembly for driving the loudspeaker and phones outlet.

Control Circuits

22 The Front Panel Assembly provides the controls and displays necessary to operate the receiver. These are interfaced via the PROCESSOR which processes front panel commands as well as those received via the remote control ports. Hence control of all modules in the receiver is completely digital.

23 Single function push buttons control the most commonly used operations and four softkeys control the receiver's many special facilities by means of a menu system.

24 Three liquid crystal displays (LCDs) indicate the current selections and operating settings of the receiver. Backlighting is provided, the intensity being controlled by the PROCESSOR.

25 Frequency setting information from the SHAFT ENCODER is sampled by the PROCESSOR, which also decodes any key selection made on the KEYBOARD.

26 The PROCESSOR comprises a type 68000 microprocessor supported by 256 kbytes of EPROM for program storage. There is also 64 kbytes of RAM for use as a working memory and 8 kbytes of EEPROM. The latter is used for channel storage and configuring the receiver.

27 The REMOTE INTERFACE allows connection to remote control equipment using serial ASCII to exchange data and complying to RS423 standard. It consists of Master and Tributary ports to allow different system configurations in which the receiver may act,depending on the version,as either a controller with a built-in,multi-addressing capability of up to 99 receivers or as a slave. An IEEE-488 remote control interface version is also available as an alternative.

28 Slave receivers may be controlled in a number of ways: by computer (Chapter 5 provides remote interface details); by using the MA3700 receiver control unit; or by using the RA3701 and RA3702 receivers, which have built-in controller facilities. All front panel controls except on/off switching can be controlled remotely.

Power Supply Indicators

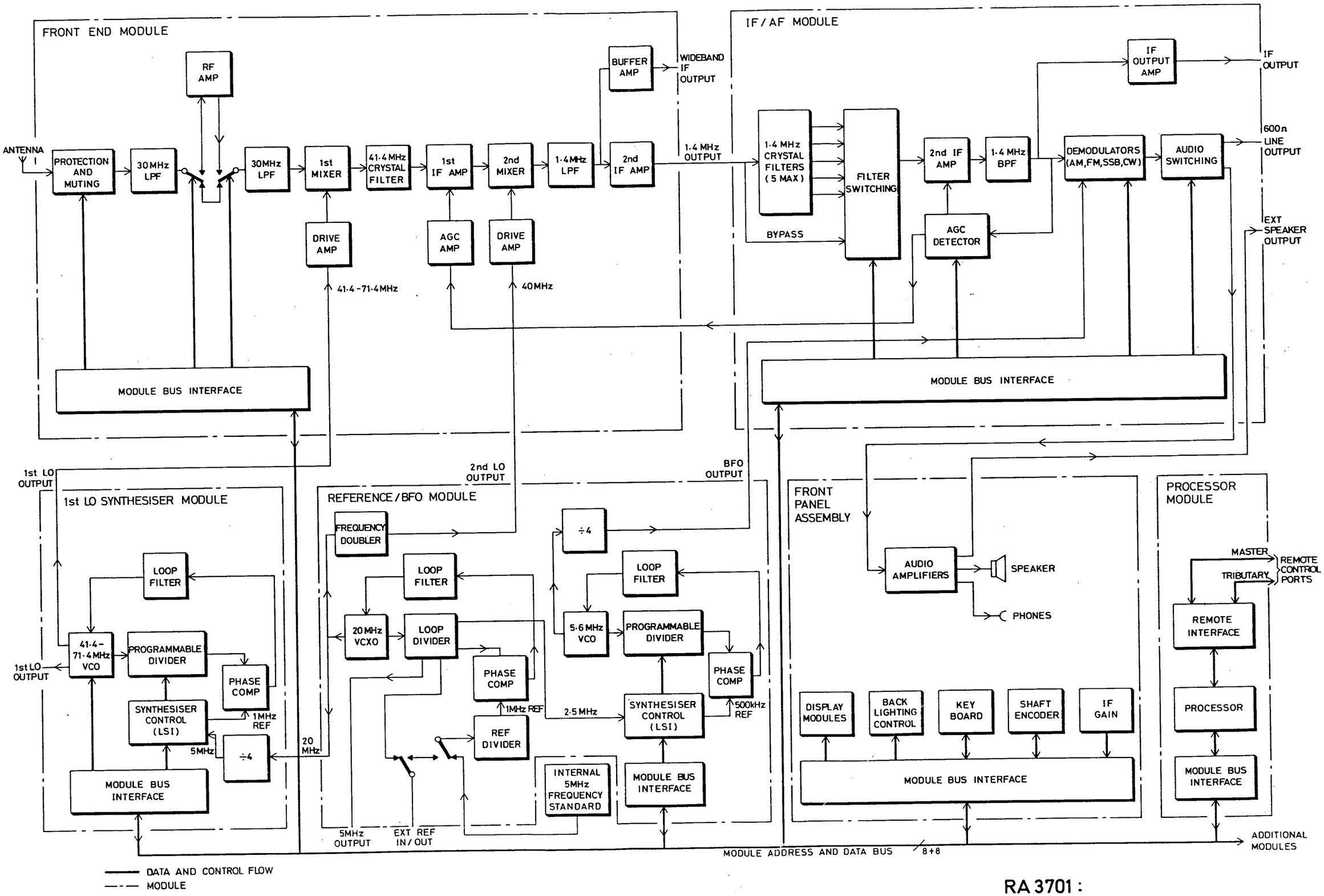
29 When lit, four red LEDs on top of the Power Supply Regulator Module indicate the presence of the stabilized +24 V, +15 V, +5 V and -15 V power supplies which are distributed throughout the equipment.

BITE

30 A comprehensive BITE facility automatically monitors the receiver operation to identify faults to module level. The BITE facilities may be controlled locally through a menu system or remotely via the REMOTE INTERFACE. Details of all these facilities are contained in Chapter 3.

PLUG/SOCKET INTERCONNECTIONS

31 The intermodule plug/socket interconnections for the various equipments in the RA3700 Series are shown in Figs. 1.6 to 1.8. Details of signals carried by the connections are given in the appropriate module chapters.



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RA 3701 : Block Diagram

Fig. 1.5

CHAPTER 2

RECEIVER SERVICING

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CHAPTER 2

RECEIVER SERVICING

INTRODUCTION

1 This chapter introduces the methods to be used in fault diagnosis and provides information to assist in any subsequent repairs to the equipment.

FAULT FINDING TECHNIQUES

2 The presence of a fault condition may be indicated by the FAULT indicator being lit or by a failure occurring when the unit confidence test is run. Alternatively, during normal operation the equipment may be observed as functioning incorrectly.

3 The user may wish to identify and replace a faulty module in order to return the equipment to service as quickly as possible. Alternatively, the user may wish to identify and replace the faulty component. This manual contains information to assist with fault diagnosis to module and component level.

4 The built-in test equipment (BITE) identifies many faults to module level using the continuous monitoring or unit confidence test facilities. Instructions on the use of these BITE facilities are given in Chapter 3. The preliminary functional checks and overall receiver performance tests detailed in Chapter 4 of this manual may also be used to indicate the presence of a fault condition and to assist in fault diagnosis. The faulty module can easily be replaced with no re-alignment being necessary.

5 In addition to identifying a faulty module, the BITE also provides more information to assist in isolating the fault to an area within the suspect module. A fault finding BITE facility (select test) is provided to allow individual BITE tests to be selected manually and run repeatedly as an aid to fault finding to component level.

6 Signature analysis facilities are also included as a means of locating faulty components in the digital circuits throughout the receiver.

7 Full details explaining the use of the fault finding BITE facility including signature analysis are also provided in Chapter 3. The actual BITE tests are detailed in the appropriate module chapter, which also includes a fault directory listing faults against possible causes with suggested actions which in some cases refer to a separate check procedure. The fault directory may be used when a fault is detected by the BITE or by other means. Where applicable, signature analysis tables are included at the back of the module chapter.

8 Refer to the appropriate module chapter for a functional description of the module under test. A circuit diagram is supplied with each module chapter and includes notes to assist with fault finding. These notes also include alignment information where applicable.

9 To assist with fault finding in the signal path through the Front End and IF/AF Modules, level charts are provided with these chapters. These charts may be used to determine the correct signal level at each stage for any input level. They also indicate the correct nominal gain of each stage.

10 Fault finding to component level may be carried out with the modules plugged in using the receiver as a test bed. Internal access to the suspect module is gained using an extender assembly provided with the BITE Kit (Table 2.1). Only standard proprietary workshop test equipment is required. A list of recommended test equipment and tools required for servicing is given later in this chapter.

11 The modules employ components which are surface mounted to the printed circuit board (PCB) instead of using plated through holes in the PCB. The recommended methods of repair of these surface mount devices (SMDs) are detailed in the module repair instructions given later in this chapter.

SAFETY PRECAUTIONS

12 Observe all safety regulations. Do not replace modules or make adjustments (except when aligning trimmers or other adjustable components) with power applied to the receiver.

WARNING:

Voltages within this equipment are sufficiently high to endanger life. Use caution when servicing power supplies or their load components.

TEST EQUIPMENT AND TOOLS

13 Table 2.1 lists the test equipment recommended for conducting performance checks, fault finding and maintenance procedures. Alternative test equipment of similar specification may be used. No special tools other than normal hand tools are required for the replacement of any module in the RA3700 Series. However, the replacement of surface mount components is simplified by the use of more specialised supplementary tools, as listed in Table 2.1.

TABLE 2.1

Test Equipment and Tools

Item	Description	Example
1	Signal Generator (quantity 2) Frequency Range : 450kHz to 50 MHz. Modulation : CW, AM and FM Output Impedance : 50 ohms.	Racal-Dana Instruments 9087
2	RF Millivoltmeter Input Impedance : 1 Mohm with 50 ohm adaptor	Racal-Dana Instruments 9302 or 9303
3	Digital Frequency Meter Frequency Range : 0 to 120 MHz	Racal-Dana Instruments 1992
4	Oscilloscope, dual trace Sensitivity : 5mV/div Bandwidth : 100 MHz	Tektronix 2235
5	Digital Multimeter	Racal-Dana Instruments 4008
6	Audio Power Meter Input Impedance : 15ohms and 600 ohms	Marconi TF893B
7	AC Voltmeter	Racal-Dana 9300B or 5002
8	Spectrum Analyser with Tracking Generator Frequency Range : 100 Hz to 100 MHz	Marconi 2382 with 2380 display
9	Signal Combiner	Racal CA612
10	Signature Analyser	Hewlett Packard 5006A
11	BITE Kit (see Chap.8, RA3700 Series Operators Manual for details of contents)	Racal supplied to order (ST88233)
12	Desolder Station	Weller DS801 or Adcola 555 with SM desoldering attachments
13	SMD Desoldering/ Reflow tips for Soldering Iron	Adcola
14	Tweezers, non-magnetic, fine point	
15	Solder Pump or Braid	

DISMANTLING THE RECEIVER

14 The modular design of the equipment keeps to a minimum the amount of dismantling necessary to gain access for maintenance purposes. The modules can be quickly removed and replaced without the use of a soldering iron. Following repair, ensure that all dismantled assemblies are correctly re-assembled and that all covers are replaced.

Fuse Replacement

15 The receiver is fitted with three supply fuses: a 2A power fuse in the voltage selector unit on the Chassis Assembly to protect the mains input, with two additional fuses (5A) mounted on the printed circuit board within the Power Supply Regulator Module. These fuses protect the +5V and +15V supplies. A spare 2A mains fuse is also provided in the voltage selector unit.

16 To change the mains fuse proceed as follows:

(1) Remove the mains lead.

(2) Open the cover of the voltage selector unit.

(3) Withdraw the right hand fuse holder and replace the 2A slow-blow fuse. (Racal Part No. 922457H). A spare fuse is normally contained in the adjacent spare fuse holder.

(4) Insert the fuse holder with the arrow pointing in the direction shown on the inside of the cover.

(5) Close the cover of the voltage selector unit.

(6) Refit the mains lead.

17 To change either the +5 V or +15 V fuses proceed as follows:

(1) Remove the mains lead.

(2) Detach the Power Supply Regulator Module from the chassis by unscrewing the four securing bolts.

(3) Identify the appropriate 5A fuse on the board (FS1: +5 V; FS2: +15 V) and replace. (Racal Part No. 922453L).

(4) Refit the Power Supply Regulator Module to the chassis.

(5) Refit the mains lead.

Module Replacement (Fig. 2.1)

18 A plug-in module is easily removed by first disconnecting any connections at the rear of the module and then unscrewing the two captive bolts securing the module to the chassis cross-rails. The module can then be unplugged. Reverse the above procedure to refit the module. No re-alignment is necessary for a new module. Internal access to a plug-in module is gained by removing the screws securing the top and bottom covers to the module.

19 The Power Supply Regulator Module can be removed by releasing the four securing bolts and withdrawing the module until the two connectors can be unplugged, allowing complete removal.

20 The Front Panel Assembly is held in place by four bolts securing it to the side cheeks of the Chassis Assembly. After unscrewing these bolts, carefully remove the module until the two ribbon connectors and power cable are accessible. Unplug these connections to allow complete removal of the Front Panel Assembly. To re-assemble, reverse the above procedure.

21 The printed circuit board attached to the rear of the Front Panel Assembly may be released by undoing the securing screws, after first unplugging the loudspeaker (if fitted) and removing the front panel knobs.

22 The Frequency Standard Module (if fitted) is accessible when the Front Panel Assembly is first removed following the procedure described previously. After unplugging PL1, the module can be released by undoing four securing screw

Module Repair

General

23 Module repair consists mainly of component replacement. It is assumed at this stage that with the aid of the circuit diagram and component layouts the faulty component has been identified.

24 Generally, normal established workshop practices are applicable. However, because the modules use SMDs it is recommended that tools designed for the removal of SMDs are employed. Removed components should be discarded.

SMD identification and handling

25 The higher density of SMDs prevents these components being labelled on the PCB. Each SMD is identified by a grid reference given in the appropriate parts list in the module chapters, which refers to the layout drawing for the surface mount side of the PCB. The code number inscribed on surface mount resistors is also given for further identification. Other types of SMDs are either unmarked or have an ID code that may vary according to the manufacturer and are therefore not provided.

26 All components are allocated a Racal part number which is specified in the parts lists and this number is clearly marked on packages containing spares supplied by Racal.

27 Because of the small size and lack of marking on some components, it is important that when individual components are removed from their package and issued for repair, they are kept in containers marked with their part number until they are actually fitted to the board. Static sensitive device handling precautions for SMDs are identical to those for conventional leaded components.

SMD removal

28 Although repair of boards is possible using conventional tools and techniques there is a wide range of specially designed tools available which makes the task easier and reduces the chances of damaging the printed circuit board.

29 The simplest tools are SMD desoldering/reflow tips designed to fit conventional soldering irons and desoldering tools. Some incorporate a vacuum pump to melt the solder and a "sucker" to lift the component off the printed circuit board. Examples of these are listed in Table 2.1.

30 Also available are more sophisticated Rework Stations which include a positioning system, hot air gun for melting the solder, vacuum pump to remove molten solder and built-in microscope for inspection and alignment.

31 It is recommended that the repair workshop is equipped with some SMD repair facility of the type described above. Information on the removal of SM components using these tools will be found in the manufacturer's instructions.

SMD replacement

32 Surface mounted components may be replaced using a conventional miniature soldering iron and low melting point solder or using a Rework Station with a hot air gun. Before fitting the new component, any excess solder should be removed from the printed circuit board to allow the component to lie flat on the board. To avoid thermal shock to the new component, particularly capacitors, heat should be applied directly to the pads, not the component.

33 Clean the area worked upon, then inspect it to ensure the following:

(1) No damage to or displacement of adjacent components.

(2) No damage to tracks or pads.

(3) No solder bridges, solder spikes or solder splashes.

(4) No flux on the board.

34 The board is now ready for electrical test.

CHAPTER 3

USE OF BUILT IN TEST EQUIPMENT

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CHAPTER 3

USE OF BUILT IN TEST EQUIPMENT

INTRODUCTION

1 The power-up and continuous monitoring BITE tests are automatically executed without operator intervention. Access to the more in-depth BITE facilities is obtained either via the front panel menu system or the remote control port, or using the switches on the Processor Module. A summary of the BITE tests is given at the end of this chapter.

INTERPRETATION OF THE FAULT LEGEND

2 During the power-up BITE routine an automatic validity test of data stored when power was switched off is performed. If uncorrupted this data is used to set up all the receiver operational settings. If an error is found the FAULT indicator is illuminated.

3 The continuous monitoring BITE checks for correct operation of the receiver while it is switched on. A detected failure causes the FAULT legend to be lit.

4 In the above cases, more information on the nature of the fault can be obtained using the SHOW FAULT facility accessed via the menu system as described in Chapter 7 of the RA 3700 Series Operators Manual.

UNIT CONFIDENCE TEST

5 This BITE facility performs a more comprehensive test of the receiver's operation and includes a performance check of the signal path using a noise source as a test signal. In this mode the reception of normal signals is interrupted.

6 Upon detection of a fault condition the test is halted and the name of the suspect module or section is displayed. Further information can then be obtained as to the nature of the fault using the BITE operating instructions in the Operators Manual as before.

7 It is good practice to take a note of all failed tests so that a more accurate diagnosis can be made.

8 Some faults may prevent the unit confidence test being initiated from the front panel. For this reason the test can be enabled by means of a switch on the Processor Module. This is achieved by powering up the receiver with switch No. 6 set to OFF.

SELECT TEST

9 This BITE facility is intended as an aid to tracing a fault to component level. It includes all the tests performed by the unit confidence test but allows individual tests to be selected and run repeatedly. It also includes other tests which are not included in the unit confidence test.

10 To access the select test BITE facility, proceed as follows:

(1) Press the MENU key repeatedly until the following BITE test (level 3) options are displayed:

UNIT	SEL	FACT	SHOW
TEST	TEST	TEST	FAULT

(2) Press the M2 soft key to select the required test option.

(3) Check that a module or section name is displayed on the top line with INC, SLCT and EXIT displayed on the bottom line. The Processor tests are presented first.

(4) If another module or section is required to be tested, select INC by pressing the M1 soft key repeatedly until the desired module or section name is displayed.

(5) To select the BITE tests for the displayed module or section, select SLCT by pressing the M3 soft key. The first test for the chosen module or section is then displayed.

(6) If the displayed test is required to be carried out, press the M3 soft key again to select SLCT. The selected test is then performed repeatedly with the result indicated alongside the test title.

(7) If another test is required, select INC by pressing the M1 soft key until the desired test is displayed and then select SLCT by pressing the M3 soft key.

(8) To exit to the level 3 options, select EXIT by pressing the M4 soft key.

(9) Press the RCL key to exit the menu system and return the receiver to normal operation.

INTERPRETATION OF THE PROCESSOR MODULE INDICATORS

11 Some faults may prevent the menu system from displaying information on the front panel. Likewise, a fault in the remote interface of a receiver intended for remote operation would prevent the controller from examining the fault condition.

12 In both these cases, three status indicators on top of the Processor Module may be used. These 7-segment alphanumeric displays flash a 3- digit BITE test number for the failed test as listed in the Summary of BITE Tests. The BITE test numbers are not displayed on select test. If a fault exists in receiver 2 of a dual receiver, the indicators also display '.' (decimal point) in front of the test number.

13 When conducting the continuous monitoring test or select test, the letter P is displayed on one of these displays on successful completion of a test. When the unit confidence test is completed the number 999 is displayed.

SIGNATURE ANALYSIS

Introduction

14 When the receiver is operating normally, the program instructions cause continuously changing data patterns to be present within the logic circuitry. Because these data patterns are changing, data checking using conventional techniques (e.g. logic probes and oscilloscopes) becomes difficult and time-consuming.

15 These problems are avoided by the use of signature analysis techniques. The Processor is instructed to execute a series of test programs which produce distinctive and repetitive data streams (signatures) at selected points throughout the logic circuitry in the receiver. These software test programs reside in the EPROM on the Processor Module and are executed by means of test switches on the module.

16 A further test facility is provided in which the normal data bus activity of fetching data from the EPROM on power-up is isolated from the microprocessor and is replaced with a forced instruction that will allow it to free-run. This hardware signature analysis routine cycles through the entire address range to develop signatures on the address bus and address decode lines, allowing these and fundamental operation of the microprocessor, including the control lines, to be checked.

17 A common signature analysis routine is used for all plug-in modules except the Processor, Front End and Front Panel modules. The module under test is mounted on the BITE extender assembly (part of BITE kit) which is plugged into socket SK10 when testing the Processor Module and SK9 when testing any other modules. DIL switches on the Processor Module are then used to select the signature analysis routine. Detail of the DIL switch settings is given in the relevant module chapter.

Use of Signature Tables

18 Each relevant module chapter is provided with tables listing unique 4-digit alphanumeric signatures obtained from a known serviceable unit for various nodes throughout the logic circuitry. Therefore, these signatures are the references for comparison with signatures obtained when the same test is repeated during fault location procedures using a signature analyser.

19 To enter the signature analysis mode and set up the signature analyser, proceed as follows:

(1) Ensure that the receiver is powered-down.

(2) Set switches 5 to 8 on top of the Processor Module to the appropriate positions given at the beginning of each signature analysis table.

(3) Connect the signature analyser gating inputs to the test nodes given at the beginning of each signature analysis table and set the polarity as indicated. Use the test points provided on the BITE extender assembly (part of BITE kit) to gain access to the module bus plug connections.

(4) If necessary, consult the operating manual for the signature analyser for more detailed instructions on usage.

(5) Switch on the receiver. Examine the test nodes using the logic probe and check the signatures given in the table against the faulty module, working from left to right and top to bottom.

(6) Matching signatures (test and reference) imply correct functioning, incorrect signatures imply the existence of a fault condition.

(7) If an incorrect signature is found, consult the relevant circuit diagram to establish which is the driving logic and thus interpret the fault condition.

(8) The first signature given in the tables is the +5 V rail. In addition to checking the IC supplies, it also verifies that the test equipment is correctly set up.

SUMMARY OF BITE TESTS

20 Table 3.1 lists the BITE tests provided for each module and indicates if they are performed during the automatic BITE tests, or presented for selection during the manual select BITE tests. A more detailed description of each test is given in the appropriate module chapter.

TABLE 3.1

BITE Tests

Test No.	Displayed Message	Power-up	Continuous Monitoring	Unit Confidence	Select Test
	Processor				
001	Checksum PD1	YES	NO	NO	NO
002	Checksum PD2	YES	NO	NO	NO
003	RAM test ML17	YES	NO	NO	NO
004	RAM test ML15	YES	NO	NO	NO
005	EEROM test	YES	NO	NO	NO
006	+5V rail	YES	NO	YES	YES
007	+15V rail	YES	NO	YES	YES
008	-15V rail	YES	NO	YES	YES
009	+24V rail	YES	NO	YES	YES
010	-5V rail (serial only)	YES	NO	YES	YES
011	DAC test	YES	NO	YES	YES
012	Processor I/O	NO	NO	NO	YES
013	Parallel I/O 1	NO	NO	NO	YES
014	Parallel I/O 2	NO	NO	NO	YES
	RX Config.				
051	Master port INT (serial only)	NO	NO	NO	YES
052	Master port EXT (serial only)	NO	NO	NO	YES
053	Trib. port INT (serial only)	NO	NO	NO	YES
054	Trib. port EXT (serial only)	NO	NO	NO	YES
055	IEEE 488 Interface (IEEE only)	NO	NO	NO	YES
	RX bus				
101	RX data bus	YES	NO	YES	YES
102	RX address data	YES	NO	YES	YES
103	RX bus control	YES	NO	YES	YES
104	RX BITE bus	YES	NO	YES	YES
	Front Panel				
151	BITE hardware	NO	YES	YES	YES
152	+5V rail	NO	YES	YES	YES
153	+15V audio rail	NO	NO	YES	YES
154	-15V rail	NO	NO	NO	YES
155	+15V rail	NO	NO	NO	YES
156	Displays Test	NO	NO	YES	YES
157	Keyboard Test	NO	NO	NO	YES

TABLE 3.1

BITE Tests (continued)

Test No.	Displayed Message	Power-up	Continuous Monitoring	Unit Confidence	Select Test
	Reference/BFO				
201	BITE hardware	NO	YES	YES	YES
202	+5V rail	NO	YES	YES	YES
203	+15V rail	NO	YES	YES	YES
204	BFO Ref level	NO	YES	YES	YES
205	BFO Ref lock	NO	YES	YES	YES
206	Ref Osc. varac V	NO	YES	YES	YES
207	40 MHz o/p level	NO	YES	YES	YES
208	BFO lock	NO	YES	YES	YES
209	BFO Osc.varac V	NO	YES	YES	YES
210	BFO sweep	NO	NO	YES	YES
211	BFO o/p level	NO	YES	YES	YES
	1st LO Synth.				
251	BITE hardware	NO	YES	YES	YES
252	+5.2V rail	NO	YES	YES	YES
253	+15V rail	NO	YES	YES	YES
254	+24V rail	NO	YES	YES	YES
255	+9V rail	NO	YES	YES	YES
256	-15V rail	NO	YES	YES	YES
257	Synth. varactor	NO	YES	NO	NO
258	Synth. range	NO	NO	YES	YES
259	Synth. sweep	NO	NO	YES	YES
260	Synth. o/p level	NO	NO	YES	YES
	IF/AF				
301	BITE hardware	NO	YES	YES	YES
302	+5V rail	NO	YES	YES	YES
303	+15V rail	NO	YES	YES	YES
304	+10V rail	NO	YES	YES	YES
305	-15V rail	NO	YES	YES	YES
306	IF amplifier	NO	NO	YES	YES
307	IF filter	NO	NO	YES	YES
308	2nd IF AGC	NO	NO	YES	YES
309	AGC detector	NO	NO	YES	YES
310	AGC distribution	NO	NO	YES	YES
311	AGC decay	NO	NO	YES	YES
312	AGC hang	NO	NO	YES	YES
313	AGC dump	NO	NO	YES	YES
314	Product detector	NO	NO	YES	YES
315	AM detector	NO	NO	YES	YES
316	FM detector	NO	NO	YES	YES
	Front End				
351	BITE hardware	NO	YES	YES	YES
352	+5V rail	NO	YES	YES	YES
353	+15V rail	NO	YES	YES	YES
354	+24V rail	NO	YES	YES	YES
355	+12V rail	NO	YES	YES	YES
356	-15V rail	NO	YES	YES	YES
357	1st mix drive lvl	NO	YES	YES	YES
358	1st mix drive swp	NO	YES	YES	YES
359	2nd mix drive lvl	NO	NO	YES	YES
360	RX gain	NO	NO	YES	YES
361	1st IF gain	NO	NO	YES	YES

TABLE 3.1

BITE Tests (continued)

Test No.	Displayed Message	Power-up	Continuous Monitoring	Unit Confidence	Select Test
	100 kHz Module				
401	BITE hardware	NO	YES	YES	YES
402	+5 V rail	NO	YES	YES	YES
403	+15V rail	NO	YES	YES	YES
404	1.4 MHz A	NO	NO	YES	YES
405	1.4 MHz B	NO	NO	YES	YES
406	100 kHz A	NO	NO	YES	YES
407	100 kHz B	NO	NO	YES	YES
408	5 MHz level	NO	YES	YES	YES
	FSK Module				
451	BITE hardware	NO	YES	YES	YES
452	+5V rail	NO	YES	YES	YES
453	+15V rail	NO	YES	YES	YES
454	-15V rail	NO	YES	YES	YES
455	FSK disc. sweep	NO	NO	YES	YES
456	FSK meter sweep	NO	NO	YES	YES
457	FSK slicer sweep	NO	NO	YES	YES
	ISB Module				
501	BITE hardware	NO	YES	YES	YES
502	+5V rail	NO	YES	YES	YES
503	+15V rail	NO	YES	YES	YES
504	+10V rail	NO	YES	YES	YES
505	-15V rail	NO	YES	YES	YES
506	IF amplifier	NO	NO	YES	YES
507	AGC detector	NO	NO	YES	YES
508	AGC distribution	NO	NO	YES	YES
509	AGC decay	NO	NO	YES	YES
510	AGC hang	NO	NO	YES	YES
511	AGC dump	NO	NO	YES	YES
512	Product detector	NO	NO	YES	YES
	IF Filter				
551	BITE hardware	NO	YES	YES	YES
552	+5V rail	NO	YES	YES	YES
553	+15V rail	NO	YES	YES	YES
554	-15V rail	NO	YES	YES	YES

Note that the tests are not all performed in the order shown in the table.

CHAPTER 4

RECEIVER PERFORMANCE TESTING

CONTENTS

TABLE

CHAPTER 4

RECEIVER PERFORMANCE TESTING

INTRODUCTION

1 This chapter contains detailed test procedures to enable the performance of the complete receiver to be checked out. The tests may be carried out as part of a routine maintenance schedule or as an aid to fault location to a module. Refer to the appropriate module chapter for fault location information and alignment procedures.

2 It is assumed that the receiver is fitted with an internal frequency standard. If this is not the case, then a suitable external frequency standard must be connected to the rear panel REF IN/OUT.

PRELIMINARY FUNCTIONAL TEST (No test equipment required)

3 Carry out the following procedure to check that the receiver is functioning and that no major faults exist. The tests are written for receivers with full front panel controls but can be adapted for slave receivers by using a controller to operate the receiver via its remote interface.

Procedure

4 Inspect the equipment for signs of physical damage.

5 Check all controls for correct mechanical action, i.e. freedom from binding,scraping or general interference of parts.

6 Set the REF INT/EXT switch (S1) on the Reference/BFO Module to INT unless an internal frequency standard is not fitted. Set the other selector switches (S3, S4) for a 10MHz reference frequency output.

7 Ensure that the rear panel voltage selector is correctly set to suit the source of supply.

8 Connect the receiver to the local source of supply.

9 Connect a pair of headphones to the front panel PHONES socket.

10 Set the POWER switch on the receiver to ON.

11 Check that all Power Supply Regulator Module LEDs are lit.

12 Ensure that the front panel displays are activated after a delay of approximately two seconds.

13 Ensure that the FAULT legend is not visible on the left-hand display. If a fault condition is indicated, use the SHOW FAULT option accessed via the menu system to reveal the nature of the failure, refer to the RA3700 Series Operators Manual for instructions on usage.

14 Using the menu system, run the unit confidence test as detailed in the Operators Manual.

15 In the event of a failure occurring during either of the above tests, refer to the receiver servicing chapter in this manual for fault finding information.

16 Select each control function in turn by pressing the appropriate buttons (refer to the RA3700 Series Operators Manual for operating procedures) and observe that the front panel displays indicate that the correct function has been selected and that the tuned and BFO frequencies are correctly displayed.

17 Set the receiver to 0MHz. Press the TUNE-button repeatedly until SLOW is indicated on the centre display. Slowly rotate the tuning control clockwise and ensure that the receiver tunes up in 1Hz steps. Repeat in the anti-clockwise direction. Ensure each tune rate is displayed on the centre display by pressing the TUNE + button repeatedly. Note: the tune rates are made available for selection by the tune rate list menu facility

18 Select widest bandwidth, AM detector, Manual IF gain and enter a frequency above 500 kHz. Ensure that the noise output from the receiver varies with the setting of the IF GAIN and VOLUME controls, becoming louder as the controls are advanced.

19 Select SHORT AGC. Select each bandwidth in turn and ensure that the receiver noise level falls as the bandwidth is reduced.

20 Select FM and CW and ensure that the character of the noise output changes for each demodulator.

21 Select CW, MEDIUM AGC, enter tuned frequency 0 MHz, select BFO tune and tune the BFO through the range -9 kHz to +9 kHz using the main tuning knob. Ensure that a beat note corresponding to the BFO offset is audible. Ensure that the front panel loudspeaker output can be switched off and on using the L/S button.

22 Tune the BFO to +1.00 kHz, and observe that RF and AF levels are indicated as appropriate on the LCD meter scales.

23 Select SHORT AGC and set the IF GAIN control fully clockwise. Press SQLCH and ensure that the tone disappears (after a delay) when the IF GAIN control is set fully anti-clockwise.

24 Connect an antenna to the rear panel antenna socket and tune to a known transmission. Refer to the Operators Manual and observe that all controls function normally.

25 Check the channel memory by storing operational settings and recalling them as instructed in the Operators Manual.

26 Switch the receiver off and on again to see if it returns to the previous operational settings.

PERFORMANCE TEST PROCEDURE

27 Details of test equipment called up in the following test procedure can be found in Table 2.1, Chapter 2.

Audio Output Power

28 Connect the signal generator output to the receiver antenna input. Connect the audio power meter to the receiver external loudspeaker output (pins 8 and 15, PL6 on the IF/AF Module). Set the power meter load to 8 ohms.

29 Set the receiver as follows:

Mode	:	USB
AGC	:	Short
Internal Loudspeaker	:	Off
Volume control	:	Fully clockwise
Frequency	:	1.02 MHz

30 Set the signal generator output to – 53 dBm, CW, and its frequency to 1.021 MHz.

31 Ensure that the audio output power is not less than 1 W.

32 Transfer the power meter to the PHONES output on the front panel. Set the power meter load to 600 ohms. With the volume control fully clockwise ensure that the power output is not less than 1 mW.

33 Connect the AC voltmeter with 600 ohm load to the receiver line output (pins 1 and 9, PL6 on the IF/AF Module). Ensure that the line level is 0dBm ± 3 dB. If necessary, adjust the line level control on top of the IF/AF Module to set the line output level.

Sensitivity

34 Connect the signal generator output to the receiver antenna input. Connect the AC voltmeter with 600 ohm load to the receiver line output.

35 Set the receiver as follows:

Mode	:	USB, 2.7 kHz bandwidth
AGC	:	Manual
IF Gain	:	Maximum
RF Amplifier	:	On

36 Set the signal generator output to –113 dBm, CW.

37 Set the receiver frequency to 0.52 MHz and the signal generator frequency to 0.5215 MHz. Note the reading on the AC voltmeter. Switch off the signal generator output and ensure that the reading on the AC voltmeter drops by not less than 16 dB. This is the S + N/N ratio.

38 Repeat para 37 with the receiver frequency set to 10.52 MHz and the signal generator frequency set to 10.5215 MHz.

39 Repeat para 37 with the receiver frequency set to 20.52 MHz and signal generator frequency set to 20.5215 MHz.

40 Repeat para 37 with the receiver frequency set to 29.52 MHz and the signal generator frequency set to 29.5215 MHz.

41 On the receiver, switch off the RF amplifier. Repeat para 37 to para 40 ensuring that the S + N/N ratio is not less than 10 dB.

42 Set the receiver as follows:

Mode	:	AM
Bandwidth	:	6 kHz
AGC	:	Short
RF Amplifier	:	On

43 Set the signal generator output to –103 dBm, 70% AM modulated at 1 kHz.

44 Set the receiver frequency and signal generator frequency to 0.52 MHz. Note the reading on the AC voltmeter. Switch off the signal generator modulation and ensure that the reading drops to not less than 16 dB.

45 Repeat para 44 to measure the AM sensitivity at 29.52 MHz.

Selectivity

46 Connect the signal generator to the receiver antenna input. Connect the RF millivoltmeter (50 ohm input impedance) to the IF output socket (SK1 on the IF/AF Module).

47 Set the receiver as follows:

Frequency	:	5.5 MHz
Mode	:	USB
AGC	:	Manual
IF Gain	:	Maximum

48 Set the signal generator to 5.501 MHz, CW and its level to –53 dBm.

49 Adjust the IF Gain control for a reading of –10 dBm on the RF millivoltmeter.

50 Select the appropriate mode and bandwidth and carry out the following procedure to check the passband selectivity. The specifications for the standard filters are listed in Table 4.1.

51 Tune the signal generator frequency across the passband of the selected filter and record the maximum output level indicated on the RF millivoltmeter. This peak response is the reference level.

52 Measure the offset frequencies at which the response of the filter is 6 dB down on the reference level noted in para 51. Table 4.1 lists the correct limits for the standard filters.

TABLE 4.1

Passband Selectivity Characteristics

Filter Number	Filter Type	Nominal Bandwidth (kHz)	Offset Frequencies at -6 dB	
			Not Exceeding (kHz)	Not less than (kHz)
BD86658	USB	2.7	+0.3	+3.0
BD86659	LSB	2.7	-3.0	-0.3
BD86662	SYM	0.3	-0.15	+0.15
BD86661	SYM	1.0	-0.5	+0.5
BD86658*	SYM	2.7	-1.35	+1.35
BD86660	SYM	6.0	-3.0	+3.0
Bypass	SYM	12.0	-6.0	+6.0

Note: * indicates offset USB filter

AGC and Manual Gain Control

53 Connect the signal generator output to the receiver antenna input. Connect the AC voltmeter with 600 ohm load to the line output.

54 Set the receiver as follows:

Mode	:	USB
AGC	:	Short
RF Amplifier	:	On
Frequency	:	1.02 MHz
Meter	:	RF

55 Set the signal generator output to 1.021 MHz, CW, – 107 dBm (0 dB μV pd).

56 Note the indication on the AC voltmeter as a reference. Increase the output level of the signal generator in 10 dB steps up to a maximum of + 13 dBm. At each step monitor the RF meter on the front panel and ensure that it reads within ±20 dB of the signal generator level. Also observe the AC voltmeter and ensure that the reading remains within ±2 dB of the reference level.

57 Repeat para 56 for AGC medium, omitting the front panel meter tests.

58 Repeat para 56 for AGC long, omitting the front panel meter tests.

59 Set the AGC to manual and the IF Gain control fully clockwise.

60 Set the signal generator to the following output levels in turn and ensure that at each output level the IF Gain control can be used to restore the indication on the AC voltmeter to within ±2 dB of the reference noted at para 56.

– 107 dBm
– 87 dBm
– 67 dBm
– 47 dBm
– 27 dBm
– 7 dBm
+ 13 dBm

Out of Band IMPs

61 Connect the outputs of the two signal generators to the signal combiner inputs. Connect the AC voltmeter with 600 ohm load to the receiver line output (PL6, IF/AF Module).

62 Set the receiver as follows:

Mode	:	CW
Bandwidth	:	300 Hz
AGC	:	Manual
BFO	:	1 kHz
RF Amplifier	:	On

63 Set the equipment to the following frequencies:

Receiver	:	2.123 MHz
Signal generator 1	:	2.148 MHz
Signal generator 2	:	2.173 MHz

64 Connect the RF millivoltmeter (50 ohm input impedance) to the output of the combiner.

65 Switch off the output of signal generator 2 and set the output level of signal generator 1 for an indication of -13 dBm on the RF millvoltmeter.

66 Switch off the output of signal generator 1, switch on the output of signal generator 2 and set its output level for an indication of -13 dBm on the RF millivoltmeter.

67 Switch on the output of signal generator 1.

68 Disconnect the combiner output from the RF millivoltmeter and connect it to the receiver antenna input.

69 Adjust the IF Gain control for an indication of 0 dBm on the AC voltmeter. If 0 dBm cannot be achieved then set the IF Gain control fully clockwise. Note the AC voltmeter indication for use as the reference level.

70 Switch off the output of signal generator 2. Set signal generator 1 to the receiver frequency and reduce its output level until the indication on the AC voltmeter is restored to the reference level. Ensure that the reduction in signal generator level is not less than 70 dB.

71 Repeat para 64 to para 70 for the following frequencies:

Receiver	:	29.123 MHz
Signal generator 1	:	29.148 MHz
Signal generator 2	:	29.173 MHz

Cross Modulation

72 Connect the outputs of the two signal generators to the signal combiner inputs.
Connect the AC voltmeter with 600 ohm load to the receiver line output (PL6, IF/AF Module).

73 Set the receiver as follows:

Mode	:	AM
Bandwidth	:	2.7 kHz
AGC	:	Short
RF Amplifier	:	On

74 Set the equipment to the following frequencies:

Receiver	:	5.020 kHz
Signal generator 1	:	5.020 kHz (wanted signal)
Signal generator 2	:	5.040 kHz (unwanted signal)

75 Connect the RF millivoltmeter (50 ohm input impedance) to the output of the combiner.

76 Switch off the output of signal generator 2 and set the output level of signal generator 1 for an indication of -13 dBm on the RF millvoltmeter.

77 Switch off the output of signal generator 1, switch on the output of signal generator 2 and set its output level for an indication of -13 dBm on the RF millivoltmeter.

78 Switch on the output of signal generator 1.

79 Disconnect the combiner output from the RF millivoltmeter and connect it to the receiver antenna input.

80 Set each signal generator for 30% amplitude modulation at 400 Hz and reduce the output level by 40 dB (to produce a signal at -53 dBm).

81 Note the AC voltmeter indication for use as the reference level.

82 Switch off the modulation of signal generator 1.

83 Increase the output level of signal generator 2 until the AC voltmeter indicates 20 dB below the reference level. Ensure that the increase in signal generator level is not less than 54 dB.

Blocking

84 Connect the outputs of the two signal generators to the signal combiner inputs.
Connect the AC voltmeter with 600 ohm load to the receiver line output (PL6, IF/AF Module).

85 Set the receiver as follows:

Mode	:	CW
Bandwidth	:	2.7 kHz
AGC	:	Short
BFO	:	1 kHz
RF Amplifier	:	On

86 Set the equipment to the following frequencies:

Receiver	:	5.020 kHz
Signal generator 1	:	5.020 kHz (wanted signal)
Signal generator 2	:	5.040 kHz (unwanted signal)

87 Connect the RF millivoltmeter (50 ohm input impedance) to the output of the combiner.

88 Switch off the output of signal generator 2 and set the output level of signal generator 1 for an indication of -13 dBm on the RF millvoltmeter.

89 Switch off the output of signal generator 1, switch on the output of signal generator 2 and set its output level for an indication of -13 dBm on the RF millivoltmeter.

90 Switch on the output of signal generator 1.

91 Disconnect the combiner output from the RF millivoltmeter and connect it to the receiver antenna input. Decrease the output level of both signal generators by 40 dB (to produce a signal at -53 dBm).

92 Note the AC voltmeter indication for use as the reference level.

93 Increase the output level of signal generator 2 until the indication on the AC voltmeter drops by 3 dB.

94 Disconnect the combiner output from the antenna and connect it to the RF millivoltmeter.

95 Switch off the output of signal generator 1 to measure the output level of signal generator 2. Check that it is not less than +7 dBm.

In-Band IMPs

96 Connect the outputs of the two signal generators to the signal combiner inputs.
Connect the spectrum analyser input to the MAIN IF OUT socket (SK1) on the IF/AF Module.

97 Set the receiver as follows:

Mode	:	CW
Bandwidth	:	2.7 kHz
AGC	:	LONG
BFO	:	1 kHz
RF Amplifier	:	On

98 Set the equipment to the following frequencies:

Receiver	:	5020.00 kHz
Signal generator 1	:	5019.70 kHz
Signal generator 2	:	5020.30 kHz

99 Connect the RF millivoltmeter (50 ohm input impedance) to the output of the combiner.

100 Switch off the output of signal generator 2 and set the output level of signal generator 1 for an indication of –13 dBm on the RF millvoltmeter.

101 Switch off the output of signal generator 1, switch on the output of signal generator 2 and set its output level for an indication of –13 dBm on the RF millvoltmeter.

102 Switch on the output of signal generator 1.

103 Disconnect the combiner output from the RF millivoltmeter and connect it to the receiver antenna input.

104 Adjust the spectrum analyser to display the two wanted signals plus the third-order intermodulation products.

105 Check that the third-order intermodulation products are more than 50 dB down relative to the wanted signals.

CHAPTER 5

REMOTE CONTROL OF RECEIVERS

CONTENTS

TABLES

CONTENTS (continued)

ILLUSTRATIONS

Fig.

CHAPTER 5

REMOTE CONTROL OF RECEIVERS

INTRODUCTION

1 This chapter gives details of how RA3700 Series receivers may be controlled via the Serial ASCII or IEEE-488 interfaces. Basic instructions for setting up a remote control system in which a RA3700 Series equipment acts as the controller are given in the Operators Manual. The information in this chapter provides more details of how the system operates and will allow the user to set up a remote control system using a computer as the controller.

2 The chapter is divided into a number of sections as follows:

RA3700 SERIES EQUIPMENTS IN SYSTEMS	-	An introduction to typical applications for RA3700 Series receivers in systems.
SERIAL LINK PROTOCOL	-	Full details of the serial link protocol including electrical, packet format, timing and link control characteristics. This section is not applicable to equipments with the IEEE-488 interface.
IEEE-488 LINK PROTOCOL	-	Full details of the IEEE-488 link protocol including electrical, packet format, timing and link control characteristics. This section is not applicable to equipments with the serial interface.
INSTRUCTION SET	-	A complete description of all the remote control commands and their syntax.
SUMMARY TABLES	-	Tables summarising the commands and error messages applicable for equipments used in various roles (e.g. controller, slave etc.)

RA3700 SERIES EQUIPMENTS IN SYSTEMS

Remote Control Unit

3 A RA3700 Series receiver or MA3700 receiver control unit may control other receivers by sending remote control commands from its remote control port (master serial port or IEEE-488 port depending on the option). The controller is set to address one slave receiver at a time using the address facilities on the front panel.

4 A controller in control of a slave will send commands whenever the slave settings require updating. In addition, the controller will poll the addressed slave at a rate of approximately 3 times per second in order to obtain BITE and metering information.

5 The slave receiver will only send a data packet in response to a command from the controller. This is to avoid bus clashes in multi-address systems.

6 A computer may be used as the controller in a remote control system. It should be programmed so that the commands comply with the protocol specified in this chapter.

Operation as a Slave

7 A receiver may be operated as a slave by sending control commands to its remote control port (tributary serial port or IEEE-488 port depending on the option).

8 In response to a command, a slave receiver replies with an acknowledgement packet unless the received packet was found to contain errors, eg. incorrect CRC, and link control characters were not in use. This packet may contain data or, if there is no data to send, the packet may be empty. To avoid bus clashes in a multi-address system a slave receiver will not send any data packets from its remote control port except in response to a command from the controller.

9 The slave receiver can be returned to local front panel control using the front panel REMOTE button . However, the controller can set the slave to a "local lockout" mode in which the REMOTE button is inhibited.

Receiver Set to Local

10 A receiver operating as a local, manually operated receiver can still be interrogated, allowing a controller to obtain setting information from the receiver. However, the receivers settings cannot be changed by the controller unless it first sets the receiver to remote.

Diversity Master Operation

11 This mode of operation is only available on receivers fitted with the serial remote control interface.

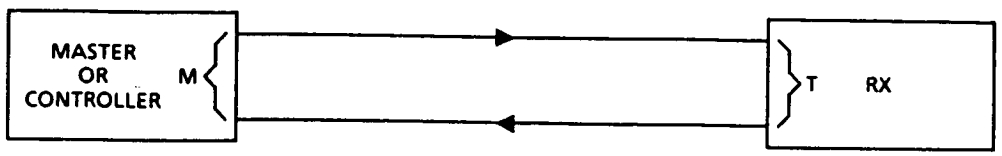
12 A receiver in "diversity master" mode sends control data from its master port to set the associated "diversity slave" to identical settings. The diversity master receiver may itself be set to local whereby it can control both receivers from its own front panel, or remote, in which case a remote controller controls both receivers as a pair. The remote controller may also address each receiver in the pair individually using a sub-addressing command. If no sub-addressing is used then the diversity master replies with its own data.

SERIAL LINK PROTOCOL

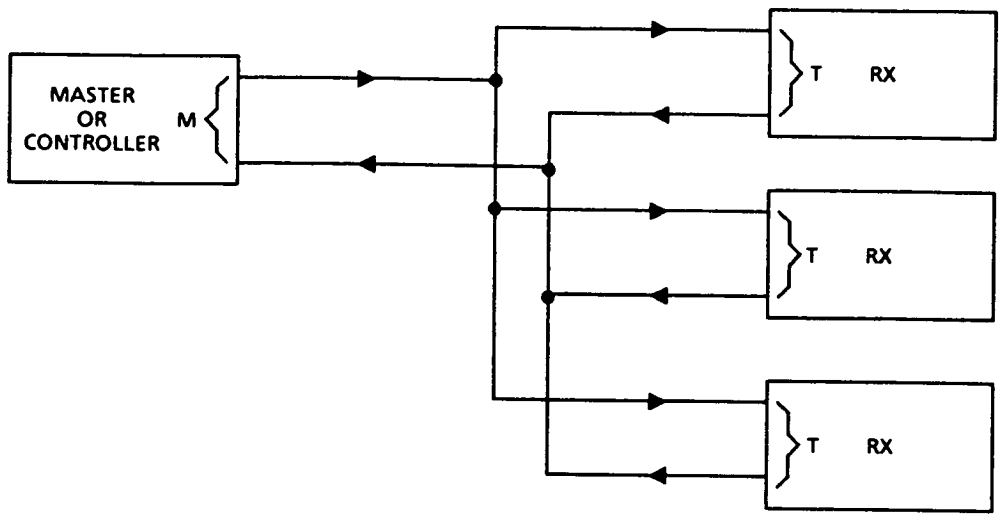
13 This section describes the link protocol used for transferring data expressed as ASCII characters over a serial link.

14 RA3700 Series equipments (serial ASCII versions) have two serial control ports. One, the "Master Port", is used on an equipment which is acting as the link controller (Master). The other, the "Tributary Port", is used when an equipment is acting as a slave (Tributary). Typical system configurations are shown in Fig. 5.1.

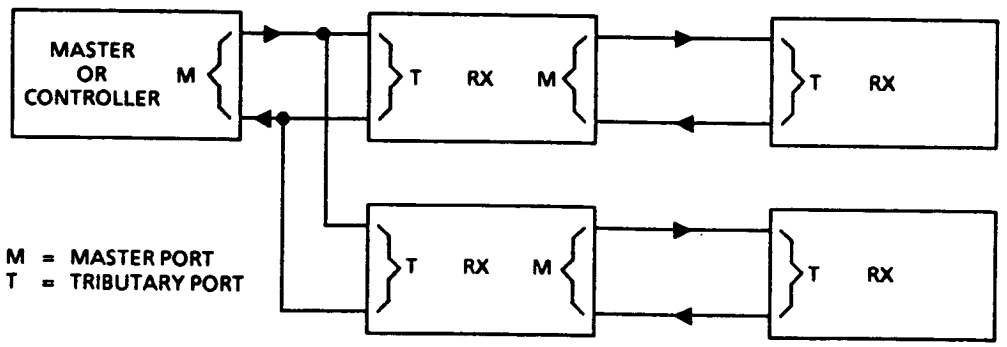
15 Before an equipment can be used in a remote control system, various parameters must be preset so that all the equipments in the system are compatible. For example, they must all be set to send and receive data at the same speed. Also, each equipment in the system must be allocated a unique address. These parameters may be set up locally as described in the Operators Manual. Alternatively they may be programmed remotely using an external control unit. This may be either a computer or another RA3700 Series equipment with full front panel controls; details of the latter are contained in the Operators Manual. Programming via a computer is covered later in this chapter.



(a) ONE – TO – ONE



(b) MULTI – DROP SYSTEM



(c) REMOTE CONTROLLED DIVERSITY PAIRS

TH 9359

Typical Serial Remote Control Configurations

Fig.5.1

Fig. 5.1 Typical Serial Remote Control Configurations

Electrical Characteristics

16 The electrical characteristics of the serial interface comply with CCITT recommendation V10 and EIA standard RS423-A.

17 Additionally, the data output may be set to a high impedance state. This allows multi-address systems to be configured with several slave equipments connected to the same control lines (i.e. multi-drop systems). The data outputs on all slave equipments not currently being addressed by the controller are set to the high impedance state.

18 The serial interface is also capable of interoperation with equipments complying with V28/RS232-C.

19 The serial interface is designed to operate with RS423-A remote control systems, but may also be operated with RS232-C systems simply by altering the signal return arrangements (see later). RS423-A is designed for longer lines with each of the two data lines for each port having their own return line, this being twisted together with the data line. RS232-C systems utilise a common return line.

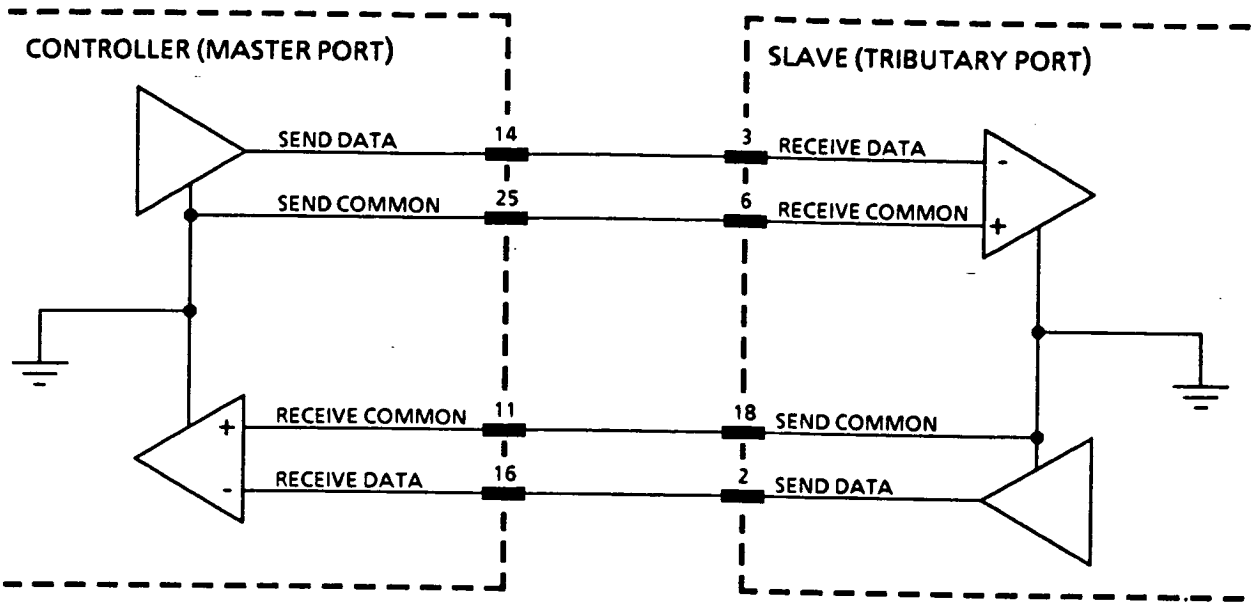
20 For an equipment fitted with a serial remote control interface, the Processor Module is provided with a 25-way D-type connector (PL2) with male pins for connecting to external equipment employing interfaces according to the above standards. The pin connections are listed in Table 5.1. Typical configurations using these connections are shown in Fig. 5.2.

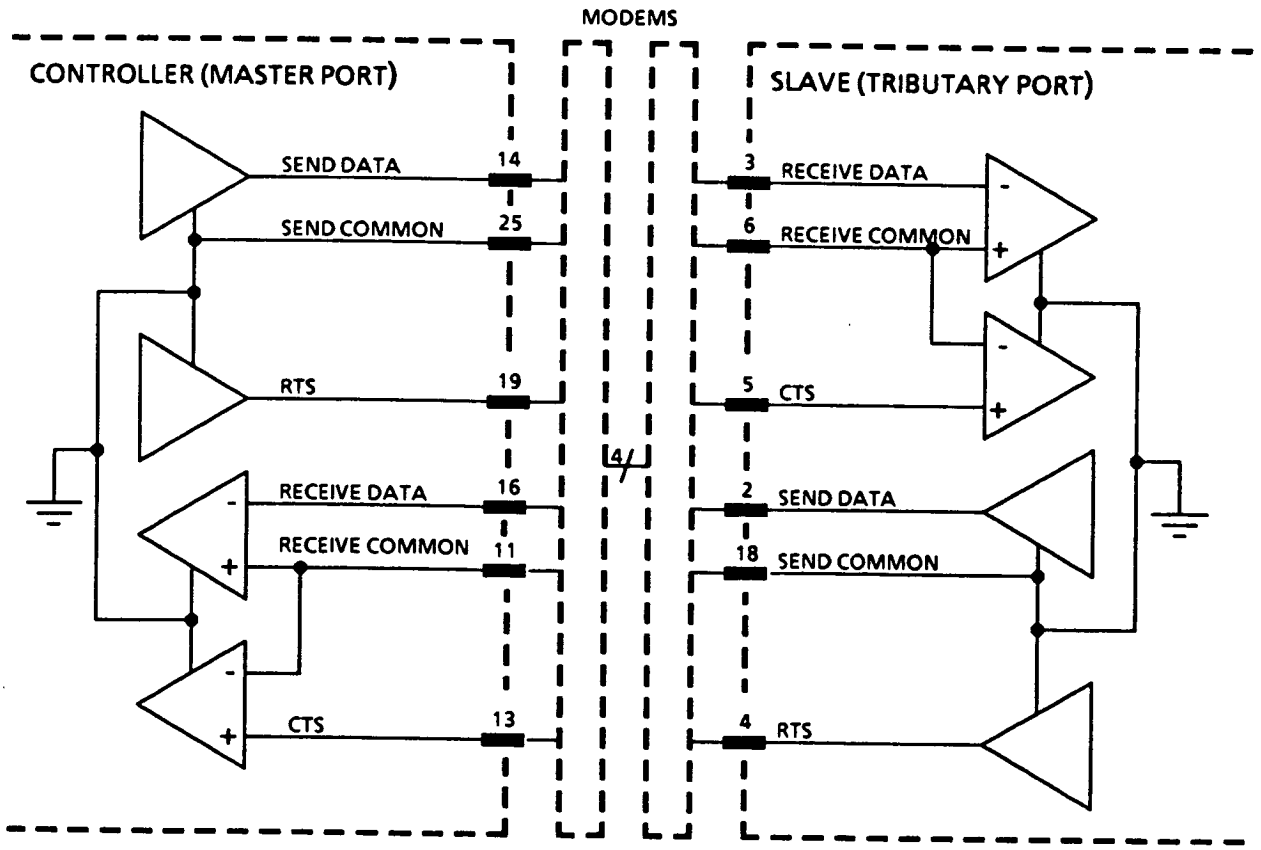
TABLE 5.1

Serial ASCII Interface Connections

Signal Description		Connector Pin No.
Send data	(M)	14
Send Common	(M)	25
Receive Data	(M)	16
Receive Common	(M)	11
Send Data	(T)	2
Send Common	(T)	18
Receive Data	(T)	3
Receive Common	(T)	6
Request to Send	(RTS) * (M)	19
Clear to Send	(CTS) (M)	13
Request to Send	(RTS) * (T)	4
Clear to Send	(CTS) (T)	5
Protective Ground		1
Signal Ground		7
Configure		12
Logic '1'		9

NOTE: M = Master Port
T = Tributary Port
* = Clear to Receive (CTR) when computer controlled.





Typical RS423 Interface Connections Fig.5.2

Fig. 5.2 Typical RS423 Interface Connections

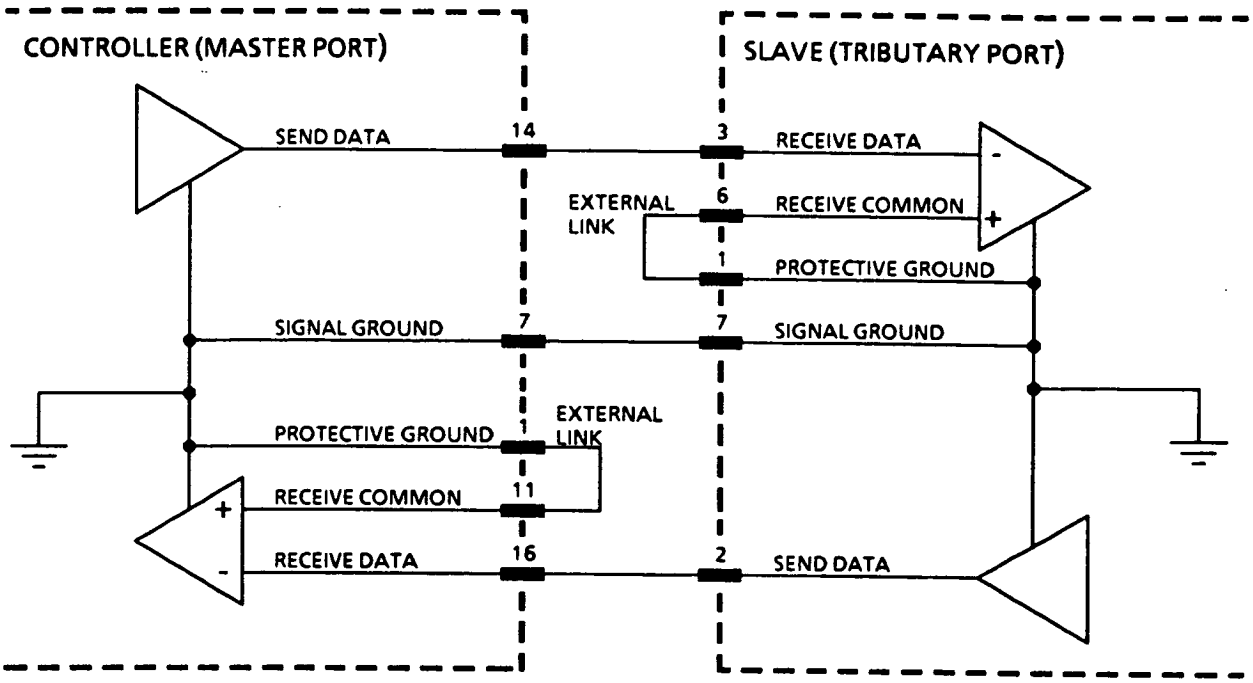


Fig. 5.3 RS232 Ground Connections

21 To accommodate either type of serial interface the signal return arrangements are connected as follows:

RS423: The 'send common' of the sending ends and 'receive common' of the receiving ends are connected together and earthed at the 'send common' ends only (see Fig. 5.2).

RS232: The signal grounds of both ends are connected together. Also the 'receive common' is linked to earth at the receiving ends by means of an external link (see Fig. 5.3).

Fig. 5.3 RS232 Ground Connections

Character Framing

22 Communication between the controller and the receiver is by means of strings of ASCII characters which are grouped together to form data packets.

23 Transmitted and received characters are asynchronous and are comprised as follows:

1 start bit	7 data bits	1 parity bit	1 stop bit

24 The data transmission speed is selectable from the following:

50, 75, 150, 300, 600, 1200, 2400, 4800, 9600 bps.

25 Character parity is selectable from "odd", "even" or "off". "Off" means that the parity bit is not sent.

26 The data bits are encoded in accordance with the CCITT ITA-5 (7 bit ISO/ASCII) alphabet (see Table 5.2 at the end of this chapter). Printing characters from columns 2 to 7 of Table 5.2 may occur as well as the following non-printing characters:

0/10	Line Feed	(LF)
0/13	Carriage Return	(CR)
1/1	DC1	(X-ON)
1/3	DC3	(X-OFF)

Packet Framing

27 The ASCII characters are assembled into packets of up to 255 characters as follows:

LF Character	0 or 1 Link Control Characters	0, 1 or 2 Address Characters	Up to 248 Printing Data Characters	0 or 3 Check Characters	CR Character

(a) The first character in the packet is a line feed.

(b) The equipment must be configured at the time of installation as to whether a Link Control Character (LCC) is included in transmitted or received messages. If not used, unacceptable packets are ignored. Configuration details are given in the Operators Manual. Details of the LCC are included later in this chapter.

(c) The equipment must be configured at the time of installation to set the number of address characters as follows:

0 - one to one operation
1 - up to 9 tributaries
2 - up to 99 tributaries

Configuration details are given in the Operators Manual.

(d) The data characters contain the actual command or data being sent over the link. Details of the command instruction set for the RA3700 Series are contained in this chapter.

(e) The equipment must be configured at the time of installation as to whether check characters are included in the transmitted and received messages. If selected, a 16 bit Cyclic Redundancy Code (CRC) is used. Details are contained in this chapter.

(f) The final character in the packet is a carriage return.

Packet Timing

28 The rules for packet timing are given in the following paragraphs. The values given are the longest total response time allowed for the system, including any transmission delays. The aim in general for good system operation would be to respond considerably faster than this, and the response times given should be treated as maximum values rather than design targets.

(a) A valid packet shall be a series of asynchronous characters beginning with (LF) and terminated by (CR). A packet shall also be terminated by the receipt of another (LF). Such a packet is not valid and shall not cause a response. The terminating (LF) may be the first character of another packet.

(b) At a Master port a received packet may be considered terminated if no character is received for 1 second. Such a packet is not valid.

(c) At a Master port, 1 second shall be allowed from the end of an output frame for the receipt of the (LF) of the reply packet before assuming a packet failure.

(d) At a Tributary port, gaps between characters shall be ignored and there shall be an indefinite wait for the next character.

(e) Between the transmitted characters in a packet, gaps should be no more than 100 ms. During any such gap the Data output shall be held at a MARK.

(f) After receipt of the last bit of a packet at a Tributary, the first bit of the reply packet (LF) should be placed on the Data Output within 100 ms.

(g) At a Tributary port there shall be an indefinite wait for a response from a Master port.

(h) No data (other than X-ON/X-OFF) shall be placed on the output of a port while a packet is being received at the input of that port.

(i) Whilst sending a packet from the output of a port, no input data (other than X-ON/ X-OFF) shall be valid.

(j) At a Master port, packets may be generated as required (except that paragraph (i) must be observed).

(k) At a Tributary port, packets shall never be generated except in response to a correctly addressed valid packet.

(l) At a Tributary port, packets shall always be generated in response to a correctly addressed valid packet.

Bus Driver Timing

29 The rules for bus driver timing are given below:

(a) Tributary port outputs are normally in the open circuit (O/C) condition and must default to this state at power-ON. If the unit has been configured for unaddressed operation then the output would normally remain active (not O/C) at all times.

(b) On receipt of its own address within a packet, a Tributary ports data output shall be placed in the MARK (Binary 1) state within 0.5 ms.

(c) If a Tributary port data output is held in the active state whilst receiving a packet which subsequently becomes invalid, then the data output shall be returned to the O/C state immediately.

(d) The Tributary data output must remain at MARK for at least one character length at the send data rate in use before starting to send (LF). Note that for any packet other than a minimum length packet with no CRC this condition is guaranteed by para (b).

(e) On receipt of a packet containing an address other than its own, a Tributary port shall be returned to the O/C condition within 0.5 ms after receipt of the last character of that address. For good system operation it is recommended that a delay of at least 0.2 ms occurs before the line is returned.

(f) The output of a Master port must be active at all times.

(g) If several Master ports are connected together only one may be the active link master. Arbitration for "mastership" will normally be manual.

Check Characters

30 The equipment may be configured to send check characters with the data packet so that integrity of the data can be checked at the receiving end of the link. This feature is useful on noisy links to prevent corrupted data from causing incorrect responses and so that a repeat of corrupted data can be requested. If the LCC is not in use, the equipment will not reply to a packet which has incorrect check characters.

31 The equipment may be configured so that check characters are not sent. This will give a slight improvement of data throughput on good quality links.

32 The 3 check characters are calculated as follows:

(a) A 16-bit Cyclic Redundancy Code (CRC) is calculated using the CRC-16 polynomial. The (LF), (CR) and check characters are excluded. Parity, if present, is masked to zero and the data treated as 8-bit characters.

(b) The 16-bit residue is transmitted in the 3 check characters as (MS 4 bits), (next 6 bits), (LS 6 bits). 32 decimal - (20 Hex) is added to each character to provide ASCII printing characters.

(c) If a packet is received with the terminating (CR) immediately following the (LF) or [Link Control Character] or [Address Characters] (total packet less than 7 characters), the CRC check is not performed.

Communication Protocol

33 Units transmit alternately over the link (half-duplex operation). Each responds to a packet from the other even if they have no data to send. A minimum length (link status) packet comprises the following:

(LF) [Link Control Character] [Address Characters] (CR).

Bus Driver Timing

29 The rules for bus driver timing are given below:

(a) Tributary port outputs are normally in the open circuit (O/C) condition and must default to this state at power-ON. If the unit has been configured for unaddressed operation then the output would normally remain active (not O/C) at all times.

(b) On receipt of its own address within a packet, a Tributary ports data output shall be placed in the MARK (Binary 1) state within 0.5 ms.

(c) If a Tributary port data output is held in the active state whilst receiving a packet which subsequently becomes invalid, then the data output shall be returned to the O/C state immediately.

(d) The Tributary data output must remain at MARK for at least one character length at the send data rate in use before starting to send (LF). Note that for any packet other than a minimum length packet with no CRC this condition is guaranteed by para (b).

(e) On receipt of a packet containing an address other than its own, a Tributary port shall be returned to the O/C condition within 0.5 ms after receipt of the last character of that address. For good system operation it is recommended that a delay of at least 0.2 ms occurs before the line is returned.

(f) The output of a Master port must be active at all times.

(g) If several Master ports are connected together only one may be the active link master. Arbitration for "mastership" will normally be manual.

Check Characters

30 The equipment may be configured to send check characters with the data packet so that integrity of the data can be checked at the receiving end of the link. This feature is useful on noisy links to prevent corrupted data from causing incorrect responses and so that a repeat of corrupted data can be requested. If the LCC is not in use, the equipment will not reply to a packet which has incorrect check characters.

31 The equipment may be configured so that check characters are not sent. This will give a slight improvement of data throughput on good quality links.

32 The 3 check characters are calculated as follows:

(a) A 16-bit Cyclic Redundancy Code (CRC) is calculated using the CRC-16 polynomial. The (LF), (CR) and check characters are excluded. Parity, if present, is masked to zero and the data treated as 8-bit characters.

(b) The 16-bit residue is transmitted in the 3 check characters as (MS 4 bits), (next 6 bits), (LS 6 bits). 32 decimal - (20 Hex) is added to each character to provide ASCII printing characters.

(c) If a packet is received with the terminating (CR) immediately following the (LF) or [Link Control Character] or [Address Characters] (total packet less than 7 characters), the CRC check is not performed.

Communication Protocol

33 Units transmit alternately over the link (half-duplex operation). Each responds to a packet from the other even if they have no data to send. A minimum length (link status) packet comprises the following:

(LF) [Link Control Character] [Address Characters] (CR).

34 The Link Control Characters and Address Characters are sent only if selected.

35 Link Masters may break the alternate transmission rule with one equipment by changing the Message Address. Since wrongly addressed messages are ignored by Tributaries, each Tributary is 'unaware' of this lack of continuity. Masters normally arrange status responses to each Tributary so as to prevent spurious error reports from the Tributary.

36 Tributaries wait indefinitely for a response from the Master. Masters wait for at least 1 second for a response before assuming loss of the packet. After such a timeout, the last packet may be re-transmitted.

37 Tributaries respond only to input packets containing their own address. Tributary responses include their address.

Flow Control

38 Link Control Characters and X-ON/X-OFF characters may be sent in order to control the flow of messages over the link. A CTR/RTS output and a CTS input are also provided.

Link control characters

39 Packet flow control is achieved using the link control character (LCC) which enables the sender to indicate its status with respect to input and output packets and consists of a bit significant printing character as follows:

bit 0 = OUTPUT-READY.

This bit indicates that the sender has data awaiting transmission over and above the packet containing the Link Control Character.

bit 1 = OUTPUT-PHASE.

This bit is a modulo 2 packet count. It shall alternate 0 to 1, 1 to 0 when a new packet is sent and remain unchanged when a packet is re-transmitted.

bit 2 = INPUT-ACCEPT.

This bit indicates that the sender has accepted the last packet received. A packet shall be accepted if received with appropriate address and without protocol, parity or CRC error. Note that acceptance at this level does not imply that the packet was entirely valid or has been actioned.

bit 3 = INPUT-PERMIT.

This bit indicates that the sender is prepared to receive an (other) input data packet. If this flow control facility is not used the bit shall be set always to 1. If input permit has not been set any received input may be ignored.

bit 4 = INPUT-PHASE.

This bit is a copy of the OUTPUT-PHASE bit of the last input packet to have been accepted by the sender.

bit 5 = 0
bit 6 = 1
bit 7 = Parity, if transmitted.

40 The rules for the use of link control characters are as follows:

(a) Following correct reception of a packet, a packet shall be returned including an LCC with INPUT-ACCEPT set to 1. INPUT-PHASE shall be a copy of the OUTPUT-PHASE bit in the LCC of the correctly received message. INPUT-PERMIT shall be set to 1 if the sender is prepared to receive a further data packet.

(b) If the packet is not received correctly, the return packet shall have INPUT-ACCEPT set to 0, and INPUT-PHASE shall be left at the values most recently sent. If a transmitted packet fails to obtain a positive INPUT-ACCEPT response, it is recommended that a maximum of 8 re-tries is attempted.

(c) The sender shall transmit a data packet (a packet containing data bytes other than address/LCC/CRC etc.) if he has data to be sent and INPUT-PERMIT of the most recently received LCC is set to 1. Failing this, a status packet (LCC/address) shall be transmitted.

(d) As each packet is sent (data or status) the OUTPUT-PHASE bit shall be alternated 1 to 0, 0 to 1. If a packet is re-transmitted due to non-acceptance, the OUTPUT-PHASE bit is re-transmitted unchanged. Note that there is no requirement for other LCC bits to be left unchanged on re-transmission.

(e) In each packet sent, the OUTPUT-READY bit indicates (if set to 1) that the sender has further data packets over and above the data in the packet being sent, if any.

(f) When powered up, an equipment shall initially go into a "receive" state with zero LCC link status.

X-ON/X-OFF characters

41 X-ON/X-OFF is a Serial flow control protocol sent via the data path. It is not used in multi-address bus configurations. The rules for the use of X-ON/X-OFF characters are as follows:

(a) All ports shall respond to X-ON/X-OFF and may generate them if required.

(b) On receipt of an X-OFF character (1/3, DC3) (see Table 5.2) at any time a port shall be disabled from sending data. If the port was sending data then no more than 16 additional characters shall be sent.

(c) A port disabled by X-OFF may still hold the RTS line ON and in this condition must hold the data output at MARK.

(d) A port disabled by X-OFF can only be re-enabled by receipt of an X-ON (1/1, DC1) character.

(e) Tributaries shall wait indefinitely for the X-ON character. Link Masters shall wait at least 10 seconds before assuming Tributary failure.

(f) A port which may generate X-ON/X-OFF characters shall only do so when enabled by CTS.

(g) At power up the port shall assume the enabled condition.

CTR/RTS output and CTS input

42 These outputs and inputs provide a hard-wired means of controlling data flow.

43 The terminology is defined as follows:

CTR	-	Clear to Receive
RTS	-	Request to Send
CTS	-	Clear to Send

44 These lines are not used in multi-address systems.

45 The RA3700 Series equipments are always configured as data terminal equipments (DTE). When connected to a data communications equipment (DCE), e.g. a modem, the CTR/RTS output should be configured as RTS. When connected to another DTE, e.g. a computer, the CTR/RTS output should be configured as CTR.

46 Configuration of the CTR/RTS output is achieved using the receiver menu system.

RTS/CTS operation

47 The equipments should be connected as follows:

DTE (receiver)		DCE (modem)
RTS output	⟶	CTS input
CTS input	⟵	RTS output

48 The rules for RTS/CTS operation are as follows:

(a) RTS/CTS operation is identical for Tributary and Master ports and overrides all other protocol consideration.

(b) The RTS output of a port may be placed in the ON state as soon as there is data to send from that port.

(c) After RTS is placed in the ON condition a unit shall wait for the CTS line to respond with an ON condition.

(d) RTS must be maintained in the ON condition until the last bit has been transmitted, after which it must be returned to the OFF condition.

CTR/CTS operation

49 The equipments should be connected as follows:

DTE (receiver)		DTE (computer)
CTR output	⟶	CTS input
CTS input	⟵	CTR output

50 The rules for CTR/CTS operation are as follows:

(a) CTR/CTS operation is identical for Tributary and Master ports and overrides all other protocol considerations.

(b) The CTR output shall be placed in the ON state whenever the port is able to receive data.

(c) The CTR output may be returned to the OFF condition at any time.

(d) When the CTS input is in the OFF condition the data output shall be maintained at MARK (Binary 1). A port shall wait indefinitely for the CTS ON condition.

(e) When the CTS line goes to the ON condition then data may be transmitted from the port.

(f) If CTS changes from ON to OFF whilst data is being transmitted then no more than 2 additional characters shall be sent.

(g) When CTS protocol is not used the inputs should be pulled to the ON condition.

(h) At power-up the RTS line if selected shall be set to the OFF condition. The CTR line if selected shall be set to the ON condition.

Remote Link Configuration

51 The link parameters are normally configured via the front panel of the receiver but may be configured remotely from the controller, using the LINK command (see instruction set regarding format).

52 In order to allow the receiver to accept this command, the configure pin on the receiver's remote interface must be grounded (see Table 5.1 for connection details). In this configuration the receiver will respond to the following default link settings:

(a) 600 baud
(b) No LCC
(c) Zero address characters
(d) Even parity
(e) No CRC.

53 The receiver adopts the link configuration settings specified by the link command as soon as the 0 V is removed from the configure pin.

IEEE-488 LINK PROTOCOL

54 This section describes the link protocol used for transferring data over the IEEE-488 bus.

55 RA3700 Series equipments (IEEE-488 versions) have one IEEE-488 port. This is configured as a "Tributary" if the equipment is being used as a slave, or as a "Link Controller" if the equipment is in control of the link. At any time there must be only one active link controller on the bus. Typical system configurations are shown in Fig. 5.4.

Fig. 5.4 Typical IEEE Remote Control Configurations

56 Before an equipment can be used in a remote control system, various parameters must be preset so that all equipments in the system are compatible. Also, each equipment must be allocated a unique address. These parameters are set up as described in the Operators Manual.

IEEE-488 Bus

Introduction

57 The IEEE-488 interface is a communications bus between up to 15 equipments. Data is sent in a bit-parallel, byte-serial format. There are 16 transmission lines within the interface:

(a) 8 data lines (to transfer data between equipments and to carry certain IEEE-488 commands dependent upon the state of the management lines).

(b) 3 handshake lines (to control data transfer).

(c) 5 management lines (see "Interchange circuits" below).

58 The link controller is responsible for assigning who will talk on the bus (the "talker") and who will listen (the "listeners"). An equipment that is not addressed to talk or to listen will take no part in or have any effect upon data transfers. The handshake lines are used to ensure that a talker does not send data until all listeners are ready to accept. Thus, the data transfer will take place at the speed of the slowest listener.

Lines on the Bus

59 Details of the lines on the bus are defined in ANSI/IEEE Std. 488-1978. A summary is included below:

(a) Management Lines:

ATN - Attention	-	used to switch the use of the data lines between application dependent data and IEEE-488 commands.
IFC - Interface Clear	-	when asserted (for at least 100 µs), causes each interface on the bus to move to its quiescent state.
REN - Remote Enable	-	used to switch a responding interface between remote and local modes.
SRQ - Service Request	-	used by a tributary to request service from the link controller. The link controller will then need to interrogate each equipment on the bus to determine the originator of the SRQ.
EOI - End or Identify	-	serves two purposes. When EOI is asserted at the same time as ATN, it is a request for parallel poll data. Otherwise, it is asserted to indicate the last byte of a data stream (packet).

(b) Data Lines:

The 8 data lines are used to convey bit parallel data between equipments, one byte at a time.

(c) Handshake Lines:

The handshake lines are used to control the transfer of bytes across the data lines. They consist of:

NRFD	- Not Ready for Data	-	when no listener is driving this line low, the talker may send data.
DAV	- Data Valid	-	driven low by the talker when the data on the data lines is valid.
NDAC	- Not Data Accepted	-	driven low by a listener until it has accepted the data on the data lines.

Capabilities

60 The RA3700 Series equipments support the following optional features within the IEEE-488 standard:

Link Controller Capabilities

Capability to issue the IFC command
Capability to issue the REN command
Capability to respond to SRQ
Passing and receiving control

Tributary Capabilities

Equipments respond to IFC
Equipments respond to REN
Equipments respond to LLO
Capability to generate an SRQ

Electrical Characteristics

61 The electrical characteristics are defined in ANSI/IEEE Std. 488-1978.

Packet Framing

62 Characters are assembled into packets of up to 252 characters as follows:

Up to 248 printable data characters	0 or 3 Check Characters	Terminating Character(s)

(a) The data characters contain the actual command or data being sent over the link. Details of the command instruction set for the RA3700 Series are contained in this chapter.

(b) The equipment must be configured at the time of installation as to whether check characters are included in the transmitted and received messages. If selected, a 16 bit Cyclic Redundancy Code (CRC) is used. Details are contained in this chapter.

(c) The equipment must be configured at the time of installation as to which terminating characters are required. Either carriage return (CR) or carriage return plus line feed (CR + LF) may be selected.

Packet Timing

63 The rules for packet timing are given in the following paragraphs. The values given are the longest total response times allowed for the system, including any transmission delays. The aim, in general, for good system operation, would be to respond considerably faster, and the response times given to be treated as maxima rather than design targets:

(a) A packet shall be regarded as starting with the data that is immediately received following the unit being addressed to listen. A packet is terminated by receipt of a (CR). If a unit is re-addressed before receipt of the (CR), then any data received prior to the re-addressing is discarded.

(b) At a link controller, a received packet may be considered terminated if no byte is received for 100 ms and such a packet shall not be valid.

(c) At a tributary, a received packet may be considered terminated if IFC is detected and such a packet shall not be valid.

(d) Between the transmitted bytes, it is recommended that gaps should not exceed 100 ms although, subject to the above time-outs, no error should result if this time is exceeded.

(e) At a link controller, one second shall be allowed for the start of receipt of the reply from the time at which the tributary is enabled.

(f) At a tributary the reply should be available for transmission within 100 ms from the end of a received packet. Failure to meet this criterion, subject to the above clauses, will not, however, cause error.

(g) At a tributary, there shall be an indefinite wait for data from the link controller.

(h) At a link controller, packets may be generated as required.

(i) At a tributary, packets shall always and only be generated in response to valid packets.

Communication Protocol

64 Units transmit alternately over the link (half-duplex operation). Each responds to a packet from the other by sending a link status (minimum length) packet, even if they have no data to send. Such a packet comprises a terminator character alone.

65 A link controller may break the alternate transmission rule with one equipment by addressing another. Since packets not addressed to a tributary are ignored by that tributary, each tributary is unaware of this lack on continuity.

66 Physical control of byte transfers is accomplished by the handshake process as described in ANSI/IEEE Std. 488-1978.

67 Before any packet can be sent, the controller must establish the correct talker and listener using the commands defined in ANSI/IEEE Std. 488-1978.

Check Characters

68 The equipment may be configured to send check characters with the data packet so that integrity of the data can be checked at the receiving end of the link. The equipment will not reply to a packet which has incorrect check characters.

69 The equipment may be configured so that check characters are not sent. This will give a slight improvement of data throughput on good quality links.

70 The 3 check characters are calculated as follows:

(a) A 16-bit Cyclic Redundancy Code (CRC) is calculated using the CRC-16 polynominal. The (LF), (CR) and check characters are excluded. Parity, if present, is masked to zero and the data treated as 8-bit characters.

(b) The 16-bit residue is transmitted in the 3 check characters as (MS 4 bits), (next 6 bits), (LS 6 bits). 32 decimal - (20 Hex) is added to each character to provide ASCII printing characters.

(c) If a packet contains only a terminator character, the CRC check is not performed.

INSTRUCTION SET

71 This section gives details of the messages which are sent in the data character field of the packets previously described. Messages are formatted as follows:

[frame 1] ; [frame 2] ; ..... [frame N] ;

72 There are four principal types of frame:

(a) A forward COMMAND frame. This is actioned without reply (except for an empty packet to indicate that an acceptable packet has been received), unless it is in error.

e.g. F12.345M is a command frame to change receiver frequency.

(b) A STATUS frame which requests an equipment to respond with a revertive frame (see below). Status frames are prefixed by the letter "Q".

e.g. QF is a status frame requesting the receiver frequency.

(c) A REVERTIVE frame which is sent in reply to a status frame.

e.g. F12.345M sent in reply to QF is a revertive frame indicating the receiver frequency.

(d) An unsolicited REPORT may be sent by a receiver within the packet it sends in reply to another command.

e.g. ERR 2 might be sent by the receiver upon receipt of an invalid instruction.

73 The instruction set is described below. Details of number range, number format and command validity are contained in the summary tables at the end of this chapter. For commands relating to optional facilities, refer to the relevant option module chapter.

(1) **AF Level** **AFLnnn**
QAFL

QAFL is a request for a receiver to supply AF level information, in the range of 0 - 255. The data should be interpreted as in the table below. If a receiver is operating in the ISB mode, then the level of the monitored sideband is returned. The AFL message is revertive only.

AF levels:

Value	Level (approx.)
0 - 67	-10 dBm
68 - 75	-9 dBm
76 - 84	-8 dBm
85 - 95	-7 dBm
96 - 107	-6 dBm
108 - 120	-5 dBm
121 - 134	-4 dBm
135 - 151	-3 dBm
152 - 170	-2 dBm
171 - 190	-1 dBm
191 - 214	0 dBm
215 - 240	1 dBm
241 - 255	2 dBm

(2) **AGC Mode** **AGCn,n**
QAGC

The two digit numeric code represents the AGC/manual gain mode.

The first digit is the gain mode :

0 - AGC
1 - manual only
2 - manual with threshold

The second digit is the time constant :

0 - short
1 - medium
2 - long
3 - Link II data
4 - Link II normal

In manual only mode the receiver will ignore the time constant digit, but a digit must still be sent by the controller.

E.g. AGC0,1 respresents AGC with medium decay time constant.

(3) **Request all Settings** **QALL**

This instruction is a request for all the receiver settings and has the same effect as:-

QANT;QAGC;QBFO;QB;QCORL;QF;QFLG;QG;QM;QPASSB;QPASSF;QBWL;

The receiver replies with the above settings.

(4) **Receiver Antenna Outputs** **ANTnn**
QANT

This instruction is used to program the parallel output port from the receiver (normally used for antenna selection). The 4 lines are programmed by a numeric code in the range 00 to 15 on a single receiver and 00 to 03 on a dual receiver.

(5) **Audio Switching** **AUDIOn,n**

The receiver powers up with its detector ouputs switched to its loudspeaker amplifier. For some applications (e.g. HF DF) it is necessary to break this connection. This is accomplished with the audio command.

The first digit is :

0 for audio path broken
1 for audio path connected

The second digit is not used and should be set to 0.

(6) **BFO** **BFOnnnn**
QBFO

BFO is sent in floating point format (NF2). Superfluous trailing digits (e.g. tenths of Hz) are ignored. The valid BFO range for the receiver is -9.99 to +9.99 KHz.

E.g. BFO-0.8K or BFO-800 represents -800 Hz BFO
BFO2.0K or BFO 0.002M represents 2 KHz

(7) **IF Bandwidth** **Bn,nn**
QB

This instruction selects the IF bandwidth using 2 parameters - a bandwidth type and bandwidth number.

The bandwidth type is :

1 for USB bandwidths
2 for LSB bandwidths
3 for symmetrical bandwidths

Bandwidth numbers are assigned so that each bandwidth can be uniquely identified. They are in the range 0 to 15. In a remote control system all receivers must be configured so that a given bandwidth number always selects a filter with the same specification and also selects the same frequency offset. However, it is permissible for some equipments to be configured with more bandwidths than others. If a remotely controlled receiver is requested to select a bandwidth for which it has not been configured, it sends an error message and remains on the same bandwidth. The QBWL and QBCON commands may be used to obtain details of the bandwidths available on a receiver.

(8) **Bandwidth Configuration** **BCONn,nn,...**
QBCONn,nn

The "BCON" command is used to configure the receiver with the bandwidths which are available for selection from the front panel or via remote control. The data field has the following format :

n	bandwidth type (see instruction (7) above)
,nn	bandwidth number (see instruction (7) above)
,nn	filter position
,nn.nn	lower passband frequency, Flower
,nn.nn	upper passband frequency, Fupper
,nn.nn	frequency offset, Foff
,n	insert in (1) or remove from (0) configuration

Only one filter is configured by each command. Only the first 2 parameters apply to the "QBCON" command - it is used to request configuration data for a particular bandwidth. After bandwidth reconfiguration the bandwidth list will include all the bandwidths for which the receiver has just been configured. See Chapter 7 for further details of bandwidth configuration.

(9) **Built-In Test Equipment** **BITE n,nnn,"message"**
QBITE

The "BITE" instruction is used to set up the receiver to perform BITE tests and as a revertive message to report on the BITE status. The "QBITE" instruction is used by a controller to instruct a remote receiver to report on its BITE status. These commands may be issued by the controller whenever it is required to perform a BITE test or obtain the BITE status and also to obtain details of a fault indicated by a "FAULT" message.

The first digit of the "BITE" instuction represents the BITE level:

1 - power up BITE
2 - unit confidence BITE (full)
3 - not used, reserved for system BITE
4 - fault finding BITE
5 - factory BITE
6 - continuous BITE
7 - show fault
8 - unit confidence BITE (partial, used in dual receivers)

A receiver cannot be instructed to perform level 1 or level 6 tests (it does these automatically) although faults are reported at these levels (see below and "QFAULT").

The second number in the command represents the BITE test number. When issued in a "BITE" command it has the following effect:

Level 2 - Level 8 BITE tests start at this number and automatically increment until either a fault is found or until the last test is performed. When the last test is performed then the test number is set to 999 and the receiver awaits further instructions (see example 1).

Level 4 - the test indicated by the number is repeated continuously until otherwise instructed.

Level 5 - BITE tests start at this number and automatically increment, repeating continuously, until otherwise instructed or a fault is found.

Level 7 - in response to a QBITE command, the receiver sends details of the first fault with a test number higher than the test number specified (see example 2).

The "message" string sent with a BITE reply is the same string as displayed on the top line of the 40 character LCD on the front panel, when in the menu option 'SHOW FAULT'.

A "RCL" instruction is used to return the receiver to normal operation.

Note that the detailed fault messages obtained by selecting "More" on the front panel menu are generated locally in the controller, there being one message for each BITE test number.

Examples of how the BITE instructions are used are shown below.

EXAMPLE 1. Run unit confidence test.

The controller instructs the slave to start unit confidence test by sending the command: BITE 2,001," "

After responding with an empty packet to acknowledge receipt of the command, the slave starts to run the unit confidence test from test number 001. The controller may monitor the progress of the BITE test by sending to the slave the command: QBITE

The slave replies with: BITE 2,nnn, "message"
where nnn represents the number of the last test performed and the message gives the name of the test and an indication of a pass or failure. The controller may then send another QBITE to continue monitoring progress.

If the slave finds a fault, the test sequence will stop on that particular test. The sequence may be re-started by sending the command: BITE 2,nnn + 1"" where nnn is the number of the failed test.

While the slave is performing the BITE test, the controller may address and control another slave without interrupting the BITE test.

When the slave has completed the BITE test it will reply to the QBITE command with: BITE 2,999, "Unit test completed"

EXAMPLE 2. Fault reported by continuous BITE.

During operation, the slave receiver performs continuous BITE. The controller may poll the slave with the command: QFAULT

The slave replies with: FAULT 0 if there is no fault
or: FAULT 5 if a fault is detected.

On receipt of a FAULT 5 message, the controller can interrogate the slave to obtain information about the fault by sending the command: BITE 7,001, ""; QBITE

This command puts the slave into "show fault" mode and requests details of the first failure with a test number higher than 001.

The slave replies with an empty packet followed by an indication of this failure, e.g. BITE 7,260, "Front End" which indicates that the Front End Module 1st LO level is incorrect.

To obtain details of the next fault, the controller sends, for example: BITE 7,261,""; QBITE
In this command the test number specified is one higher than the last failure. The slave replies with the next fault, if any.

When there are no more faults to report, the slave replies with: BITE 7,999, "No more faults"

(10) **Bandwidth List** **BWLn,nn,n,nn,...**
QBWL

The "QBWL" command is used to instruct a remotely controlled receiver to send its bandwidth list. It does this with the "BWL" message which is followed by a list of bandwidths, each described in the same format as given under the B command. This list contains all the bandwidths configured in the receiver. Further details of the bandwidth configuration can then be obtained using the QBCON command.

(11) **COR Status** **Cn,n**
QC

This instruction indicates whether the COR threshold has been achieved and the state of the "SCAN INHIBIT" line.

First digit : 0 = COR level not achieved, 1 = COR level achieved
Second digit : 0 = SCAN INHIBIT off, 1 = SCAN INHIBIT on

(12) **Channel Recall** **CHANnn**
QCHAN

This instruction causes the slave receiver to operate on channel "nn" unless it is in delta mode. In delta mode, this instruction acts on the delta mode settings.

(13) **Clear All Channels** **CLEARALLCHANNELS**

This instruction sets all data in the receiver's channel store to defaults.

(14) **Change All Scan Flags** **CHGFn**

This instruction changes the scan flags in all 100 channels (0 = clear, 1 = set).

(15) **COR/Squelch Level** **CORLnnn**
QCORL

A 3 digit decimal number in the range 000 to 255 represents the COR threshold. 255 corresponds to the lowest (most senstitive) threshold.

E.g. CORL213 represents a level of 213 .

The last COR/Squelch level sent is remembered by a receiver when it is unaddressed or set to local. It is not changed until the receiver is set to local and the IF gain control is operated.

(16) **COR Control** **CORn,nn**
QCOR

This allows the user to set up how the rear panel COR output and the front panel "COR" legend operate. It is normally used during system configuration. An alternative method of doing this is to use the front panel menu system. The first parameter determines how COR is enabled :

n = 0 - COR facility disabled
n = 1 - COR facility enabled
n = 2 - COR facility enabled when squelch is selected

The second parameter sets the COR hang time. The range of values is 0.1s to 9.9s in 0.1s steps.

(17) **Diversity Control** **DIVMn**
(Serial Only) **QDIVM**

This is used to nominate a receiver as the master of a diversity pair.

n = 0 - Not a diversity master
n = 1 - Diversity master

(18) **Enter DELTA mode** **DLTA**

This instruction causes all subsequent operations to be performed on a remote receiver's delta mode settings. Note that the delta mode settings are not displayed on the slave receiver; it continues to display operational settings. The receiver remains in delta mode until either the "ENTR" or "RCL" instruction is received. This facility enables several parameters to be set up and simultaneously entered. It also allows settings to be sent to the receiver and stored in a channel without affecting operation on the current channel.

(19) **Enter** **ENTR**

This command has the same function as the ENTER button on the front panel. This instruction is used to set the receiver to the delta mode settings.

(20) **Error** **ERRn,"string1","string2"**

This message is only sent revertively upon receipt of an invalid instruction, syntax error or out-of-range parameter.

The severity code (n) is :

2 - Error causing non-execution of an instruction

String1 defines the command identifier in error to a maximum of six characters. A * is sent instead of control characters should they occur in the message.

String2 is a description of the error.

(21) **Frequency** **Fnnn.nnnnnn**
QF

This command causes the receiver to operate on the new frequency. The frequency may be sent in exponential notation (NF3), as a floating point number (NF2) or in fixed point format (NF1). The data field consists of a maximum of twelve digits (excluding the decimal point). At least one digit must be sent before the decimal point. Superfluous trailing digits (e.g. tenths of Hz) are ignored.

The only acceptable multipliers are :

M - MHz
K - KHz

The units of Hz are assumed if the multiplier is omitted. Revertive frequency data (and data originating from a master receiver) are in this (NF2) format in units of Hz. If the decimal point is omitted, then the data is decoded as if there were a trailing decimal point.

E.g. F15.789M or F15789K or F15789000 represents 15.789 MHz
F12345678. or F12345.678K represents 12.345678 MHz

(22) **Fault** **FAULTn**
QFAULT

The fault message is sent by the receiver in reply to the instructon QFAULT:

n = 0 - no fault
n = 5 - serious fault

This command is only sent revertively .

Note that the QFAULT command is sent out by a master receiver every 5 seconds. If a fault is returned, then the controller must set up the slave to show fault mode, using a BITE command. The QBITE command may then be used to determine the fault.

(23) **Channel Scan Flag** **FLGn**
QFLG

This command is used to set/clear the scan flag stored with the present channel (if any). In delta mode it acts on the delta mode channel:

n = 0 - clear scan flag
n = 1 - set scan flag

(24) **IF Gain** **Gnnn**
QG

A 3 digit decimal number in the range 000 to 255 represents the receiver manual IF gain. 255 corresponds to maximum gain.

The last IF gain number sent is remembered by a receiver when it is unaddressed or set to local. It is not changed until the receiver is set to local and the IF gain control is operated, or the receiver is addressed again and sent a new IF Gain command.

(25) **Equipment Identification** **ID"type","description","serial"**
QID

Parameter 3 is optional.

A request for ID is made using the instruction QID. This will cause the receiver to reply with its equipment identity:

e.g. ID "RA3701","HF RECEIVER","****" where **** is the serial number.

(26) **Link Configuration (Serial Only)** **LINK"flow",nnnn,nnnn,"parity","lcc","addressrx1", "crc",n,n,"addressrx2"**
QLINKn

All link parameters are optional.

The LINK command is used to configure the receiver with the link protocol. This command is only accepted if the configure pin is pulled to 0V. Alternatively, local configuration is possible using the front panel menu system of the RA3701 and RA3702 or switches on the RA3703 and RA3704.

The first parameter defines the flow control required. This may be either "RTS" or "CTR".

The second parameter defines the baud rate at which messages will be transmitted.

The third parameter defines the baud rate at which messages will be received.

The transmit and receive baud rates are equal. Any of the following baud rates will be accepted:

1. 50 Baud.
2. 75 Baud.
3. 110 Baud.
4. 150 Baud.
5. 300 Baud.
6. 600 Baud.
7. 1200 Baud.
8. 1800 Baud.
9. 2000 Baud.
10. 2400 Baud.
11. 4800 Baud.
12. 9600 Baud.

The "parity" parameter is defined in the form of a text string and may be "ODD", "EVEN" or "NONE".

The "lcc" parameter is defined in the form of a text string and may be "LCC" or "NOLCC".

The "addressrx1" parameter is defined in the form of a text string and allows setting up of the number of address characters and value of the address of the equipment under configuration. The value of the address is only applicable to configuration of a tributary port. eg "01" defines two address characters of value 01 on a tributary port but only defines two address characters on a master port. A master port does not have its own address, the address sent in the command being that of the slave being controlled. If a dual equipment then "addressrx1" defines the address of rx1.

The "crc" parameter is defined in the form of a text string and may be "CRC" or "NOCRC".

The seventh parameter defines whether free tune is enabled. This parameter is optional.

n = 0 - Free tune disabled.
n = 1 - Free tune enabled

The eighth parameter defines which port is to be configured. This parameter is optional, the configuration defaulting to the tributary port if omitted.

n = 0 - Configure tributary port.
n = 1 - Configure master port.

The "addressrx2" parameter is defined in the form of a text string and allows setting up of the number of address characters and value of the address of the second half of a dual equipment. It is only applicable to a tributary port and is not sent during configuration of a single receiver.

All parameters are sent by the receiver where applicable.

The QLINK command takes an optional parameter n which defines the port required. If omitted, then the tributary port configuration settings are always returned.

n = 0 - Tributary port settings required.
n = 1 - Master port settings required.

(27) **Receiver Mode** **Mn**
QM

A numeric code selects one of the following demodulation modes :

0 - AUX
1 - USB
2 - LSB
3 - AM
4 - FM
5 - CW
6 - FSK
7 - ISB/USB monitored
8 - ISB/LSB monitored

e.g. M5 represents CW.

(28) **Mute Receiver** **MUTEn**
QMUTE

The single digit command has the values:

0 - demute receiver
1 - mute receiver

(29) **Passband Tuning** **PASSBn,nn**
PASSFnnnn
QPASSB
QPASSF

Passband tuning is available only when the receiver is in the USB or LSB modes. If either of these commands is received when the receiver is not in one of these modes an error message is sent.

The PASSB command initiates passband tuning and selects the bandwidth number, as used with the "B" command. Only symmetrical bandwidths are acceptable. If an unacceptable bandwidth number is received (SSB or bandwidth not available) the receiver responds with an error message.

The PASSF command defines the passband tuning frequency. The data field obeys the same rules as the BFO frequency (described previously).

The QPASSB and QPASSF are used to obtain the passband tuning parameters. The parameters reverted are set to zero if passband tuning is not enabled.

Passband tuning mode is cancelled when any mode command is received.

(30) **Recall** **RCL**

This instruction has the same effect as the RCL key on a receiver front panel. The slave exits from "delta mode", and sets its displays to the operational settings. It is also used to exit BITE levels 2, 4, 5, 7 and 8.

(31) **Remote/Local (Serial Only)** **REMn**

This selects Remote or Local operation.

n = 0 - Local mode.
n = 1 - Remote control, with keyboard lockout.
n = 2 - Remote control, without keyboard lockout.

(32) **RF Amplifier** **RFAMPn**
QRFAMP

This controls the switching of the RF amplifier.

n = 0 - RF amplifier off
n = 1 - RF amplifier on
n = 2 - RF amplifier automatically switches on/off above / below a defined frequency.

(33) **RF Level** **RFLnnn**
QRFL

A 3 digit decimal number in the range 000 to 255 representing the received signal strength. The data should be interpreted as in the table below. Leading zeros are not omitted. This command is only sent revertively.

RF levels.

Value	Level (approx.)
226 - 255	0 dBµV
215 - 225	10 dBµV
203 - 214	20 dBµV
191 - 202	30 dBµV
180 - 190	40 dBµV
168 - 179	50 dBµV
156 - 167	60 dBµV
145 - 155	70 dBµV
133 - 144	80 dBµV
121 - 132	90 dBµV
110 - 120	100 dBµV
98 - 109	110 dBµV
0 - 97	120 dBµV

(34) **Subaddressing (Serial Only)** **Sn**

This command is accepted by receivers in diversity master mode only. It is sent by the controller of the diversity master in order to specify which of the diversity pair is required. The S command must precede each command in a packet.

n = 0 - Address diversity master receiver.
n = 1 - Address diversity slave receiver.
e.g. S1; QF; S1; QRFL

(35) **Scan Instruction** **SCANnn**
QSCAN

The scan instruction is used to start/stop a frequency sweep/channel scan and to control the direction of scan:

First Digit : 0 - stop sweep/scan
1 - start frequency sweep
2 - start channel scan
3 - rx set to frequency sweep stopped (revertive only)
4 - rx set to channel scan stopped (revertive only)

Second Digit : 0 - upward scan
1 - downward scan

(36) **Set up Channel Scan Parameters** **SCCHnn,nn,nnn,n**
QSCCH

This command sets the start/stop channels and the dwell time:

First parameter - start channel number
Second parameter - stop channel number
Third parameter - dwell time in NF2 format (range is 0.01 to 9.99s)
Fourth parameter - stop on COR control (0 = disable/1 = enable)

(37) **Set up Frequency Sweep Parameters** **SCFRnn,nn,nn,nnnnn,n**
QSCFR

This command sets the start , stop and step frequencies , the sweep rate and if COR is enabled when sweeping. All three frequency parameters can be NF1 , NF2 or NF3 notation .

First Parameter - start frequency
Second Parameter - stop frequency
Third Parameter - step frequency
Fourth parameter - stop on COR control (0 = disable/1 = enable)

(38) **Serial Number** **SN "serial number"**
QSN

This command is used to set the receiver's serial number.

(39) **Squelch** **SQUn**
QSQU

This command turns the squelch mode of the receiver on or off:

n = 0 - squelch off
n = 1 - squelch on

(40) **Store Channel Data** **STREnn**

The following parameters are stored in the channel nn (range 00 to 99):

Frequency
Mode
ACG mode and time constant
BFO (if mode is CW)
Bandwidth

If the receiver is in delta mode, then the delta mode settings are stored and the receiver remains in delta mode.

(41) Software Programme/Issue Number **SW"number","issue"**
QSW

The SW message is revertive only.

The strings are the receiver's programme number and issue.

(42) Enter Free Tune Mode (Serial Only) **Tn**

This instruction causes the receiver to enter free tune mode. The rest of the packet is decoded and a reply packet is transmitted from the slave. The receiver is then in free tune mode and any characters received are interpreted as increment/decrement characters as defined in the free tune summary table. A null character (ASCII zero) should be sent when changing from increment to decrement frequency. Free tune mode is terminated upon reception of a line feed character which may be the start of a new data packet. The parameter defines the free tune rate required.

n = 1 Slow tune rate.
n = 2 Medium tune rate.
n = 3 Fast tune rate.
n = 4 Variable tune rate.

74 **Commands Valid for Receiver Modes**

The table below shows in which modes of receiver operation commands sent from a controller are valid. (The states in the table refer to the mode of operation on the slave). Commands not valid over the IEEE-488 link are marked with an asterisk.

Command Identifier	BITE	Chan Scan	Freq Sweep	Delta Mode	Passband Tuning
AGC	NO	NO	YES	YES	YES
ANT	NO	YES	YES	YES	YES
AUDIO	NO	YES	YES	YES	YES
B	NO	NO	YES	YES	NO
BCON	NO	NO	NO	YES	NO
BFO	NO	NO	YES	YES	NO
BITE	YES	NO	NO	YES	YES
CHAN	NO	NO	NO	YES	YES
CLEARALLCHANNELS	NO	YES	YES	YES	YES
CHGF	NO	NO	NO	YES	NO
COR	NO	YES	YES	YES	YES
CORL	NO	YES	YES	YES	YES
DLTA	NO	NO	NO	YES	NO
DIVM *	NO	NO	NO	YES	NO
ENTR	NO	YES	YES	YES	YES
F	NO	NO	NO	YES	NO
FLG	NO	NO	NO	YES	NO
G	NO	YES	YES	YES	NO
ID	YES	YES	YES	YES	YES
LINK *	NO	NO	NO	YES	NO
M	NO	NO	YES	YES	YES
MUTE	NO	YES	YES	YES	YES
PASSB	NO	NO	NO	NO	YES
PASSF	NO	NO	NO	NO	YES
REM*	YES	YES	YES	YES	YES
RFAMP	NO	YES	YES	YES	YES
RCL	YES	YES	YES	YES	YES
S *	YES	YES	YES	YES	YES
SCAN	NO	YES	YES	NO	NO
SCCH	NO	YES	YES	YES	NO
SCFR	NO	YES	YES	YES	NO
SN	YES	YES	YES	YES	YES
SQU	NO	NO	YES	YES	YES
STRE	NO	NO	NO	YES	NO
T*	NO	NO	NO	YES	NO

75 In addition, Q (request) commands, which are responded to at all times, exist for all of the above, with the exceptions of:

1. CLEARALLCHANNELS
2. CHGF
3. DLTA
4. ENTR.
5. RCL
6. REM (Serial Only)
7. S (Serial Only)
8. STRE
9. T (Serial Only)

76 On a serial link only, the subaddress command "S" is only valid when sent to a diversity master receiver. If it is sent to a receiver which is not in diversity master mode then an error message to this effect is returned. Only Q commands are valid after an S command, any other instruction is rejected, with an error message returned.

Controller/Slave Commands

77 The table below lists those commands which are valid when sent by a controller to change the settings of a slave receiver and when sent by a slave in response to a request. Commands not valid over the IEEE-488 link are marked with an asterisk. Number formats are as follows:

NF1: e.g. 1, -2, 123, -12345
NF2: e.g. 1.1, -2.2, 123.456, -1.234
NF3: e.g. 1.2E+3, -1.23E-5, 123.456E+06

Command Identifier	Parameter Meaning	Range		Format
		Upper	Lower	
AGC	AGC Gain mode	2	0	NF1
	AGC time constant	4	0	NF1
ANT	Antenna number	15 or 3	0	NF1
AUDIO	Audio path	1	0	NF1
B	Current BW type	3	0	NF1
	Current BW number	15	0	NF1
BCON	Configuration BW type	3	1	NF1
	BW number	15	0	NF1
	Filter position	15	0	NF1
	Lower passband freq (kHz)	+9.99	-9.99	NF1/2
	Upper passband freq (kHz)	+9.99	-9.99	NF1/2
	Offset frequency (kHz)	+9.99	-9.99	NF1/2
	Remove/Insert BW	1	0	NF1
BFO	BFO frequency (kHz)	+9.99	-9.99	NF1/2
BITE	Type of BITE required	8	1	NF1
	Module & test number	999	001	NF1
	Description of test			Text
CHAN	Channel number	99	0	NF1
COR	COR function	2	0	
	COR hang time (secs)	9.9	0.1	NF1
CORL	COR level	255	0	NF1/2
DIVM*	Diversity master	1	0	NF1
F	Frequency (Hz)	29999999	0	NF1/2/3
FLG	Channel scan flag	1	0	NF1
G	Gain level	255	0	NF1
ID	Type number catalogue			Text
	Description			Text
	Serial number (optional)			Text
LINK*	Flow control (optional)			Text
	Transmit baud rate (optional)	9600	50	NF1
	Receive baud rate (optional)	9600	50	NF1
	Parity (optional)			Text
	LCC (optional)			Text
	Address (optional)			Text
	CRC (optional)			Text
	Free tune (optional)	1	0	NF1
	Port (optional)	1	0	NF1
	Address (optional)			Text

Controller/Slave Commands (continued)

Command Identifier	Parameter Meaning	Range		Format
		Upper	Lower	
M	Demodulation mode	8	1	NF1
MUTE	Mute/demute receiver	1	0	NF1
PASSB	Passband BW type	3	1	NF1
	Passband BW number	15	0	NF1
PASSF	Passband frequency (kHz)	+9.99	-9.99	NF1/2
RFAMP	RF amplifier function	2	0	NF1
SCAN	Scan mode	4	0	NF1
SCCH	Start channel	99	0	NF1
	Stop channel	99	0	NF1
	Dwell time (secs)	9.99	0.01	NF1/2
	Stop on COR	1	0	NF1
SCFR	Start frequency (Hz)	29999999	0	NF1/2/3
	Stop frequency (Hz)	29999999	0	NF1/2/3
	Step frequency (Hz)	1000000	100	NF1/2/3
	Sweep rate (Hz/sec)	1000000	10	NF1/2/3
	Stop on COR	1	0	NF1
SN	Serial number			Text

Controller Only Commands

78 The following is a list of the commands which are only valid when sent from a controller. Commands not valid over the IEEE-488 link are marked with an asterisk:

(1) CLEARALLCHANNELS
(2) CHGF
(3) DLTA
(4) ENTR
(5) REM *
(6) RCL
(7) S *
(8) STRE
(9) T*
(10) ALL Q COMMANDS.

Command Identifier	Parameter Meaning	Range		Format
		Upper	Lower	
CHGF	Set/clear all scan flags	1	0	NF1
REM *	Remote status	2	0	NF1
S *	Sub-address master/slave	1	0	NF1
STRE	Store channel	99	0	NF1
T*	Enter free tune, select tune rate	4	1	NF1

79 All Q commands are parameterless with the following exceptions:

Command Identifier	Parameter Meaning	Range		Format
		Upper	Lower	
QBCON	Bandwidth type	3	1	NF1
	Bandwidth number	15	0	NF1
QLINK *	Port required (optional)	1	0	NF1

Slave Only Commands

80 The table below lists those commands which are valid only when sent from a slave receiver.

Command Identifier	Parameter Meaning	Range		Format
		Upper	Lower	
ERR	Error severity (optional)	3	1	NF1
	Command (optional)			Text
	Error string (optional)			Text

81 The table below contains a list of those commands which are only valid when sent in response to Q commands.

Command Identifier	Parameter Meaning	Range		Format
		Upper	Lower	
AFL	Audio frequency level	255	0	NF1
BWL	Bandwidth type	3	1	NF1
	Bandwidth number	15	0	NF1
C	COR line status	1	0	NF1
	Scan line status	1	0	NF1
FAULT	Fault severity	5	0	NF1
RFL	RF level	255	0	NF1
SW	Program number			Text
	Program issue			Text

Error Messages

82 The following list describes the error mesages that may be generated by a slave receiver in response to commands received during unsuitable modes of operation.

E.1 GROUP 1 (serial only)

This message is sent in reply to all commands,with the exceptions of the REM and Q commands, if the receiver is in local operation.

(1) "RX NOT IN REMOTE"

E.2 GROUP 2

These messages are generated where ever a "NO" occurs in the table given in para 74.

(2) "BITE ACTIVE"

(3) "SCAN ACTIVE"

(4) "RX IN DELTA MODE"

(5) "PASSBAND TUNING ACTIVE"

E.3 GROUP 3

This message is generated to all of the commands detailed in para 81.

(6) "INVALID COMMAND"

E.4 GROUP 4

(7) "INVALID BANDWIDTH" - B and PASSB commands.

(8) "NOT IN CW MODE" - BFO command.

(9) "WRONG MODE" - PASSB command only valid during USB/LSB demodulation modes.

(10) "INVALID PASSBAND FREQUENCY" - PASSF command.

(11) "INVALID SERIAL NUMBER" - ID command.

(12) "FSK MODULE NOT FITTED" - M command.

(13) "ISB MODULE NOT FITTED" - M command.

(14) "PASS BAND TUNING NOT ACTIVE" - PASSF command.

(15) "LIMITS ERROR" - BCON and SCFR commands.

(16) "INVALID SCAN RATE" - SCFR command.

(17) "SUBADDRESSING ACTIVE" (serial only) - any command received other than a Q command when subaddressing in active.

(18) "NOT DIVERSITY MASTER" (serial only) - S command when received by a non diversity master.

(19) "CONFIG PIN HIGH" - LINK command.

(20) "INVALID BAUD RATE" - LINK command.

(21) "INVALID PARITY TEXT" - LINK command.

(22) "INVALID LCC TEXT" - LINK command.

(23) "INVALID CRC TEXT" - LINK command.

(24) "INVALID ADDRESS" - LINK command.

(25) "INVALID FLOW TEXT" - LINK command.

83 In addition, the following error messages may be generated by a slave receiver in response to any to any command that it has received.

(1) "INVALID IDENTIFIER"

(2) "COMMAND TOO LONG"

(3) "NO OF PARAMETERS"

(4) "NUMERIC DIGIT ERROR"

(5) "PARAMETER OUT OF RANGE"

(6) "TEXT CHARACTER ERROR"

Free Tune Frequency Increments (serial only)

84 The table below defines the actual frequency increments and decrements corresponding to each valid free tune character.

ASCII Chars and Codes (Hex)				Frequency Increment/Decrement			
Decrement		Increment		Slow	Medium	Fast	Variable
SPACE	20	P	50	1	200	1000	1
!	21	Q	51	2	400	2000	2
"	22	R	52	3	600	3000	3
£	23	S	53	4	800	4000	4
$	24	T	54	5	1000	5000	5
%	25	U	55	6	1200	6000	6
&	26	V	56	7	1400	7000	7
'	27	W	57	8	1600	8000	8
(	28	X	58	9	1800	9000	9
)	29	Y	59	10	2000	10000	10
*	2a	Z	5a	11	2200	11000	12
+	2b	L	5b	12	2400	12000	14
,	2c	\	5c	13	2600	13000	16
-	2d	|	5d	14	2800	14000	20
.	2e	”	5e	15	3000	15000	24
/	2f	-	5f	16	3200	16000	28
p	70	‘	60	17	3400	17000	34
q	71	a	61	18	3600	18000	40

Free Tune Frequency Increments (continued)

ASCII Chars and Codes (Hex)				Frequency Increment/Decrement			
Decrement		Increment		Slow	Medium	Fast	Variable
r	72	b	62	19	3800	19000	50
s	73	c	63	20	4000	20000	60
t	74	d	64	21	4200	21000	70
u	75	e	65	22	4400	22000	85
v	76	f	66	23	4600	23000	100
w	77	g	67	24	4800	24000	120
x	78	h	68	25	5000	25000	150
y	79	i	69	26	5200	26000	180
z	7a	j	6a	27	5400	27000	220
{	7b	k	6b	28	5600	28000	260
|	7c	l	6c	29	5800	29000	300
}	7d	m	6d	30	6000	30000	370
~	7e	n	6e	31	6200	31000	450
DEL	7f	o	6f	32	6400	32000	540
@	40	0	30	33	6600	33000	640
A	41	1	31	34	6800	34000	770
B	42	2	32	35	7000	35000	900
C	43	3	33	36	7200	36000	1100
D	44	4	34	37	7400	37000	1300
E	45	5	35	38	7600	38000	1600
F	46	6	36	39	7800	39000	2000
G	47	7	37	40	8000	40000	2300
H	48	8	38	41	8200	41000	2800
I	49	9	39	42	8400	42000	3300
J	4a	:	3a	43	8600	43000	4000
K	4b	;	3b	44	8800	44000	5000
L	4c	<	3c	45	9000	45000	6000
M	4d	=	3d	46	9200	46000	7000
N	4e	>	3e	47	9400	47000	8000
O	4f	?	3f	48	9600	48000	10000

TABLE 5.2

The ASCII Character Set

Bits b_7	b_6	b_5	b_4	b_3	b_2	b_1	Column / Row	0	0	0	0	1	1	1	1
								0	0	1	1	0	0	1	1
								0	1	0	1	0	1	0	1
			0	0	0	0	0			SP	0	@	P	\	p
			0	0	0	1	1		(X-ON)	!	1	A	Q	a	q
			0	0	1	0	2			"	2	B	R	b	r
			0	0	1	1	3		(X-OFF)	£	3	C	S	c	s
			0	1	0	0	4			$	4	D	T	d	t
			0	1	0	1	5			%	5	E	U	e	u
			0	1	1	0	6			&	6	F	V	f	v
			0	1	1	1	7			/	7	G	W	g	w
			1	0	0	0	8			(	8	H	X	h	x
			1	0	0	1	9			)	9	I	Y	i	y
			1	0	1	0	10	LF		*	:	J	Z	j	z
			1	0	1	1	11			+	;	K	[	k	{
			1	1	0	0	12			,	<	L	\	l	|
			1	1	0	1	13	CR		-	=	M	]	m	}
			1	1	1	0	14			.	>	N	^	n	~
			1	1	1	1	15			/	?	O	-	o	DEL

CHAPTER 6

FRONT END MODULE

CONTENTS

ILLUSTRATIONS

CHAPTER 6

FRONT END MODULE

INTRODUCTION

1 The Front End Module accepts the antenna input signal between 15 kHz and 30 MHz and mixes it with the output of the 1st LO Synthesiser Module to produce a signal at the 1st IF of 41.4 MHz. After filtering and amplification this signal is mixed with the 40 MHz output of the Reference/BFO Module to produce a signal at the 2nd IF of 1.4 MHz which is then passed to the IF/AF Module.

Fig.6.1 Receiver Block Diagram

2 A wideband 1.4 MHz IF output is also provided for use with external equipment.

MODULE DESCRIPTION

3 The following description should be read in conjunction with the Front End Module Block and Circuit Diagrams included in this chapter. Component references shown on the Block Diagram allow it to be related to the Circuit Diagram.

Input Protection

4 Input protection circuits are provided, designed to protect the receiver from lighting strikes and from continuous overloads of up to 50 V emf. The circuits include a LIGHTING ARRESTOR, a FUSE and PROTECTION DIODES.

5 The LIGHTING ARRESTOR (SG1) strikes at about 90 volts, thereby limiting the voltage applied to the next stages. The 1 Amp FUSE (FS1) provides protection for the receiver in the event of failure of the other protection circuits or of an overload greatly exceeding the specification. PROTECTION DIODES D3, D4, D5, D6 and D7 are connected in a limiter circuit to limit the signal voltage applied to further receiver input stages.

Muting Circuit

6 The muting circuit contains an OVERLOAD DETECTOR, an ANTENNA RELAY and a MUTE CONTROL circuit providing antenna relay and RF muting. RF muting is distinguished from antenna relay muting by the fact that it is electronic, muting the 1st mixer drive level and the 1st and 2nd IF amplifiers. Muting of the module will occur as a result of:

(a) An RF input signal exceeding approximately +18 dBm.

(b) A BITE signal generated by the processor.

(c) A rear panel hardware mute signal.

(d) A mute signal generated by the processor in response to a remote command.

7 When the RF input signal exceeds approximately +18 dBm, the OVERLOAD DETECTOR, through the MUTE CONTROL circuit, applies both ANTENNA RELAY (RLC) and RF mute, thus providing a high degree of muting.

8 During BITE operation the processor mutes the ANTENNA RELAY and, during BITE tests, switches on the NOISE GENERATOR to provide a test signal for injection, via the ANTENNA RELAY, on to the RF path. In this mode the RF muting is disabled to allow the test signal to pass through the RF circuits.

9 The MUTE CONTROL circuit may also be activated to mute the receiver by an external hardware input via the Processor Module rear panel. Another external mute facility is also available via the bus interface circuits. This responds to the appropriate muting command sent to the Processor when the receiver is under remote control.

10 Link LK4 on the printed circuit board is provided so that the action of the ANTENNA RELAY in response to the two above external muting signals can be inhibited if required, leaving the RF muting still available. This facility is provided for use in systems where frequent muting and de-muting takes place such as ARQ systems. Even when inhibited in this way, the ANTENNA RELAY still performs its overload protection function.

30 MHz Low Pass Filter and RF Amplifier

11 The 30 MHz LOW PASS FILTER stages prevent signals on the 1st Image and 1st IF frequencies from reaching the mixer. They also filter the 1st LO mixer breakthrough signal thus allowing only a low level of re-radiation from the antenna socket. The low pass filter is implemented in two stages, one preceding and one following the RF amplifier.

12 The RF AMPLIFIER, giving a gain of about 9 dB, may be switched in or out to provide optimum sensitivity or intermodulation performance as required. Selection of the amplifier is achieved either through the Front Panel menu system or by sending the appropriate remote command. RF AMPLIFIER SELECTION RELAY circuits either side of the RF AMPLIFIER perform the switching.

1st Mixer and Drive Amplifiers

13 The 1st LO input from the 1st LO Synthesiser Module is passed through a 40 MHz HIGH PASS FILTER to reject any noise or spurious signals below 30 MHz. It is then amplified by the 1st LO AMPLIFIERS to provide a high level drive signal to the 1st MIXER. A 1st LO LEVEL DETECTOR is provided to monitor the 1st LO drive level to the 1st MIXER for the receiver BITE system.

14 The 1st MIXER is a switching mixer consisting of a ring of four FETs. The FETs are switched at the 1st LO frequency, mixing the incoming RF signal from the antenna to produce the 1st IF of 41.4 MHz.

41.4 MHz Crystal Filter

15 The 1st MIXER output is fed via a MIXER TERMINATION CIRCUIT to a 41.4 MHz CRYSTAL FILTER. This functions as a "roofing" filter with a centre frequency of 41.4 MHz and a bandwidth of 12 kHz to protect the succeeding receiver circuits from out of band signals. It also defines the widest available IF bandwidth when the IF filters on the IF/AF Module are bypassed.

41.4 MHz IF Amplifiers

16 The 41.4MHz IF AMPLIFIER section consists of two tuned FET stages (TR14 and TR12) with variable gain plus a fixed gain bipolar transistor amplifier (TR10) driving a four-section LC BAND PASS FILTER.

17 The gain of each amplifier stage (TR14 and TR12) is controlled by adjusting the current through PIN diodes D1 and D2, which are connected across the tuned circuit of each amplifier respectively. This control is achieved since, at 41.4 MHz, the PIN diodes behave as variable resistors as their current is varied accordingly. Hence, as their current is varied by the AGC, the resistance shunting the tuned circuit is also varied, thus changing the stage gain.

18 As the signal at the antenna increases above a defined threshold, the gate voltage for the first FET stage (TR14) is increased in proportion by ML5(d) in the AGC DRIVE CIRCUIT. This optimises the amplifier's noise figure for small signals and the signal handling performance for large signals.

AGC Drive Circuit

19 The function of the AGC DRIVE CIRCUIT is to convert the 1st IF AGC voltage, which is provided by the IF/AF Module, to a current to drive the two PIN diodes and to control the gate voltage applied to TR14. The linear change in the 1st IF AGC voltage is converted to a logarithmic change in PIN diode current in order to obtain the required linear 1st IF AGC voltage versus gain reduction characteristic.

20 R16, R94 and ML3(d) provide a temperature compensated reference voltage. ML5(a) and associated components act as a virtual earth amplifier and the linear voltage to log current conversion is performed by transistors ML3(b) and ML3(c) which drive the PIN diodes. The purpose of transistor ML3(a) is to linearise the AGC characteristic at high input signal levels when the PIN diode currents are largest.

2nd Mixer and Drive Circuit

21 The 2nd MIXER is a diode ring switching mixer driven by a 40 MHz signal provided by the Reference/BFO Module. This 40 MHz signal is amplified to provide a sufficiently large signal to switch the mixer diodes. A 2nd LO LEVEL DETECTOR is provided so that the mixer LO drive level may be monitored by the receiver BITE system. The 2nd MIXER converts the 1st IF signal at 41.4 MHz to the 2nd IF of 1.4 MHz.

1.4 MHz Low Pass Filter and IF Amplifier

22 The 1.4 MHz LOW PASS FILTER at the 2nd MIXER output suppresses unwanted products of the mixing process and the 1.4 MHz IF signal is then amplified by the 1.4 MHz IF AMPLIFIER before being passed to the IF/AF Module.

23 A rear panel 1.4 MHz wideband IF output is provided by an 1.4 MHz IF OUTPUT BUFFER to drive external equipment such as a panoramic adaptor. The bandwidth of this output is 12 kHz and is determined by the roofing filter bandwidth (FL1).

24 A 1.4 MHz IF LEVEL DETECTOR is provided at the output from the module and this is used for the BITE tests.

Bus Interface

25 A unique hardwired code is received on the Module Address input to the Front End Module via the motherboard. This code is used by the ADDRESS DECODER to detect addresses on the Module Address Bus from the Processor Module and then produce read or write pulses according to the status of the R/W input. These pulses allow the Processor to read data from the 3-STATE BUFFER or write data to the DATA LATCH, using the Module Data Bus. Pulses on the strobe input ensure the correct timing of write pulses. The 3-STATE BUFFER gives the Processor access to the Front End Module identification code and also the mute status. The DATA LATCH outputs are used to control the NOISE GENERATOR, RF AMPLIFIER, MUTE CONTROL and the BITE MULTIPLEXER.

BITE Measurement System

26 The BITE measurement system, comprising the BITE MULTIPLEXER operating in conjunction with a BITE COMPARATOR, allows the Processor Module to measure various voltages and levels in the Front End Module. The voltage to be measured is selected by the BITE MULTIPLEXER and compared in the BITE COMPARATOR with a voltage generated by a digital to analogue converter (DAC) in the Processor Module. The Processor measures the level of the selected voltage by applying voltages representing upper and lower limits to the comparator and then monitoring the resulting output.

FAULT FINDING

General

27 Fault finding techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the Front End Module is contained in the following sections.

BITE Tests

28 The following BITE tests for the Front End Module are arranged in the order in which they are performed or presented for selection.

TEST NUMBER : 351

TITLE : BITE hardware

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : DAC 1 line is set to 2.55 volts (i.e. max). BITE multiplexer input X1 (+5volts) is selected and the output of the BITE multiplexer is checked to ensure that it is low.

LIMITS : Less than 0.8 V at TP2.

FAULT DIRECTORY : Fault No. 2

TEST NUMBER : 352, 353, 354, 355, 356

TITLE : +5 V rail, +15V rail, +24V rail, +12V rail, -15V rail.

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : The appropriate BITE multiplexer input is selected and the supply voltage is checked.

LIMITS :

Test No.	Supply	Mux. Input	Mux. Limits (TP2)	
			Lower	Upper
352	+5 V	X2	1.78 V	2.22 V
353	+15 V	X3	1.70 V	2.21 V
354	+24 V	X4	1.73 V	2.45 V
355	+12 V	X5	1.55 V	2.11 V
356	-15 V	X6	1.65 V	2.24 V

FAULT DIRECTORY : Fault No. 4

TEST NUMBER : 357

TITLE : 1st mix drive lvl.

PERFORMED : Continuous.

DESCRIPTION : BITE multiplexer input X8 is selected and the 1st LO level detector output is measured at the operating frequency.

LIMITS :

Mux. Input		PL5 (RF voltage)	
Lower	Upper	Lower	Upper
0.8V	-	0.55 V pk-pk	-

FAULT DIRECTORY : Fault No. 6

TEST NUMBER : 358

TITLE : 1st mix drive swp.

PERFORMED : Unit confidence test, select test.

DESCRIPTION : BITE multiplexer input X8 is selected. The output of the 1st LO level detector is measured as the receiver frequency is swept from 0 Hz to 30 MHz in 5 MHz steps.

LIMITS :

Mux. Input		PL5 (RF voltage)	
Lower	Upper	Lower	Upper
0.8 V	-	0.55 V pk-pk	-

FAULT DIRECTORY : Fault No.6

TEST NUMBER : 359

TITLE : 2nd mix drive lvl.

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : BITE multiplexer input X11 is selected and the 2nd LO level detector output is measured at the operating frequency.

LIMITS :

Mux. Input		TP10 (40 MHz signal)	
Lower	Upper	Lower	Upper
1.0 V	-	4 V pk-pk	-

FAULT DIRECTORY : Fault No. 7

TEST NUMBER : 360

TITLE : RX gain

PERFORMED : Unit confidence test, select test.

DESCRIPTION : The noise source in the Front End Module is switched on to provide a low level test signal. The change in the output from the AGC detector in the IF/AF Module is measured to check the overall receiver gain. In the unit confidence test the IF/AF Module gain is measured before this test so that a failure in test number 360 indicates a fault in the Front End Module.

LIMITS : Lower limit 200 mV (Change in DIV AGC BITE voltage)

FAULT DIRECTORY : Fault No. 8

TEST NUMBER : 361

TITLE : 1st IF gain (control)

PERFORMED : Unit confidence test, select test.

DESCRIPTION : BITE multiplexer input X7 is selected to measure the 2nd IF output level from the Front End Module. The receiver is tuned to 6 kHz to provide a test signal. The receiver is set to manual gain and the manual gain voltage is adjusted for a nominal voltage of 1.5 V at X7. The 1st IF AGC voltage is then measured by selecting BITE multiplexer input X10. The receiver frequency is then incremented in 500 Hz steps causing the IF output level to fall as the test signal moves out at the roofing filter (FL1) passband. This is continued until the IF output BITE voltage has fallen by 6 dB. The receiver gain is then adjusted to restore the IF output to its original starting level. The 1st IF AGC BITE voltage is then measured and compared to its first measurement. The change in 1st IF AGC voltage is checked against its defined limits.,

LIMITS :

Measured at	Min	Max
TP4 (1st IF AGC voltage change for 6dB change in 1st IF gain)	860 mV	-
TP2 (corresponding change at BITE comparator).	200 mV	-

FAULT DIRECTORY : Fault No. 9

Fault Directory

29 Use the following fault directory to identify the fault condition and take the necessary corrective action. Note that all inputs are assumed to be correct.

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
1	Fails to run BITE tests for Front End Module.	Address decoding/module ident. not responding	Check address decoding/module ident. logic operation using signature analysis routine if necessary.
2	BITE hardware fault.	Comparator/multiplexer inoperative.	Use BITE test 351 to check comparator operation. Select all BITE tests for this module to check multiplexer action for all analogue inputs. Use signature analysis routine to check multiplexer addressing.
3	BITE indicates failure but manual check shows no fault.	(a) BITE hardware fault. (b) Faulty BITE detector.	(a) As above. (b) Check operation of suspect BITE detector.
4	Power supply fault within module.	(a) Faulty component drawing excess current or open circuit choke. (b) +12V regulator on module faulty.	(a) Locate and replace faulty component. (b) Check voltages around ML1 and TR15.
5	Unable to control one or more functions.	Module interface faulty.	Check status of appropriate select line using oscilloscope.
6	1st mixer drive level low.	Faulty 1st LO drive circuit.	Follow 1st mixer LO drive check procedure.
7	2nd mixer drive level low.	Faulty 2nd LO drive circuit.	Follow 2nd mixer LO drive check procedure.
8	Low sensitivity/gain.	Low gain in signal path.	Follow AGC drive check procedure.
10	Out-of band IMPs, cross-modulation.	(a) Low LO drive to 1st mixer. (b) 1st mixer faulty. (c) Distortion in stages up to and including roofing filter.	(a) See Fault No. 6. (b) Check components, especially FETs. (c) Follow relevant part of the signal path check procedure.
11	Internal spurious responses.	Incorrectly fitting covers and gaskets.	Refit correctly.
12	In-band IMPs	Distortion in any stage of signal path.	See Fault No. 6,7 and 8.
13	No response to external mute (from rear panel or remote control).	Faulty mute circuit.	Follow mute circuit check procedure. Use signature analysis routine to check mute circuit output signals.
14	Poor selectivity.	Alignment requires adjustment.	Follow alignment procedure.

1st Mixer LO Drive Check Procedure

30 Measure the LO drive level by connecting PL5 to the oscilloscope input, set for 50 ohms input impedance. With LK3 set to positions A and C in turn, ensure that the waveform is greater than 0.55 V pk-pk at 71.4 MHz.

2nd Mixer LO Drive Check Procedure

31 Measure the 40 MHz drive level to the 2nd mixer at TP10, using the oscilloscope set to high impedance, and check that it is above 4 V pk-pk.

Signal Path Check Procedure

Overall module gain test

32 Set the AGC to manual and set the IF gain control fully clockwise. Switch the RF amp in and inject a test signal of -73 dBm at the antenna input (SK2). Measure the IF output level at TP7 using the RF millivoltmeter high impedance probe. If the gain does not conform to the signal level chart (see Fig. 6.2), then perform the next test.

1.4 MHz IF amplifier test

33 Set the AGC to manual and set the IF gain control fully clockwise. Switch the RF amp in and inject a test signal of -73 dBm at the antenna input (SK2). Measure the IF output at TP9 using the RF millivoltmeter high impedance probe. Check that the result agrees with the signal level chart. If the result is correct, adjust R17 in accordance with the alignment procedure (para 60) before checking voltages around the suspect 1.4 MHz IF amplifier. If the test fails then proceed with the following tests in sequence until the fault is found.

Protection circuit, LPF and RF amplifier test

34 Inject a test signal of 0dBm at the antenna input (SK2). The gain from the antenna input may be checked against the signal level chart first at LK9, then at LK5. For each test remove the link and connect the RF millivoltmeter set for 50 ohms input impedance. Repeat the test at LK5 with the RF amplifier switched into circuit and check that the gain has increased by 9dB as shown in the signal level chart.

1st mixer and roofing filter test

35 Before checking these circuits ensure that the 1st LO drive level is sufficent (see para 30). Inject a test signal of 0dBm at the antenna input (SK2). Measure the gain from the antenna input to LK7, by removing the appropriate link and connecting the RF millivoltmeter set for 50 ohms input impedance. The gain should correspond to that shown in the signal level charts. If this figure is low then check the insertion loss of the roofing filter (FL1) by injecting a test signal of 0 dBm at LK6 and measuring the output at LK7. Check the measurement figure against the signal level chart.

41.4 MHz IF amplifier test

36 Because the IF amplifier gain is AGC controlled, the AGC drive circuit should be verified first (see para 39). If this is satisfactory, proceed with checking the IF amplifier as follows.

37 Set the AGC to manual and set the IF gain control fully clockwise (i.e. maximum gain). Switch the RF amp in. Remove connector PL2 from PL2 on the IF/AF Module (this will allow a larger signal through the 1st IF amplifier stages by effectively disconnecting the IF/AF overload AGC circuit). Inject a test signal of –48 dBm at the antenna input (SK2). Measure the gain from the antenna input to TP8, TP13 and LK8, in turn, using the RF millivoltmeter high impedance probe. Check that the gains are as shown on the signal level chart. Refit connector PL2 to PL2 on the IF/AF Module.

2nd mixer test

38 Prior to checking the 2nd mixer, ensure that the 2nd LO drive level is sufficient (see para 31). Switch the RF amp in and inject a test signal of –48 dBm at the antenna input (SK2). Measure the gain from antenna input to TP9 using the RF millivoltmeter high impedance probe. Check that the gain is as shown on the signal level chart.

AGC Drive Circuit Check Procedure

39 Set the AGC to manual. As the IF gain control is turned anti-clockwise the 1st IF AGC voltage is reduced and the current through PIN diodes D1 and D2 is increased. This reduces the gain of IF amplifiers TR14 and TR12. The table below indicates the gain reduction, voltages and currents which may be measured as the 1st IF AGC voltage, at TP4, is varied using the IF gain control.

AGC Voltage (TP4)	Gain Reduction	TP5 & TP6 Voltage	R84 & R61 Voltage	D1 & D2 Current
10V	0 dB	0.15 mV	15 mV	15 µA
8V	16 dB	0.50 mV	50 mV	50 µA
6V	32 dB	1.75 mV	175 mV	175 µA
2V	64 dB	20 mV	2000 mV	2 mA
0V	80 dB	50 mV	5000 mV	5.0 mA

Muting Circuit Check Procedure

40 Set the AGC to manual and set the IF gain control fully clockwise. Connect PL1/23B to 0V to activate the 'hardware' mute (the MUTE legend should appear on the centre display). Check that the mute circuit inhibits the AGC drive circuit by ensuring TP4 is at 0V.

Signature Analysis Routine

41 This routine checks that the module control signals are interfaced and decoded correctly from the module bus.

Processor module DIL switch settings: SW4,7 OFF
SW1,2,3,5,6,8 ON

Signature Analyser connections are made via the extender assembly test points:-

Start: 9A Negative trigger
Stop: 9A Negative trigger
Clock: 8A Positive trigger
Earth: 1A

Note : Signatures xxxxF signify a flashing probe indicator.

Signal	Signature	Test Node					Remarks
+5v	U399						
OV	0000						
		DATA BUS INTERFACES					
M-D0	OP81	PL1/7A	ML9/18	ML8/3			Module bus
M-D1	006F	PL1/7B	ML9/16	ML8/4			Module bus
M-D2	8230	PL1/6A	ML9/14	ML8/7			Module bus
M-D3	431P	PL1/6B	ML9/12	ML8/8			Module bus
M-D4	2389	PL1/5A	ML9/9	ML8/13			Module bus
M-D5	0001	PL1/5B	ML9/7	ML8/14			Module bus
M-D6	0CP7	PL1/4A	ML9/5	ML8/17			Module bus
M-D7	0A54	PL1/4B	ML9/3	ML8/18			Module bus
		ADDRESS DECODER					
M-A4	0000	PL1/10A	R150	ML12/10			Module bus
M-A5	0001	PL1/10B	R152	ML12/12			Module bus
M-A6	0001	PL1/9A	R156	ML12/13			Module bus
M-A7	U399	PL1/9B	R157	ML12/15			Module bus
0	0000	PL1/14A	R167	ML12/9			Module address
1	0000	PL1/14B	R164	ML12/11			Module address
2	0000	PL1/13A	R160	ML12/14			Module address
3	U399	PL1/13B	R159	ML12/1			Module address
M-R/W	0A54	PL1/8B	R148	ML10/9	ML10/12	ML10/13	Module bus
M-STB	0000F	PL1/8A	R149	ML11/10			Module bus
A=B	U398	ML12/6	ML11/11	ML10/10			Address decoder
ML10/8	U9FF	ML10/8	ML9/1	ML9/19			Address decoder
ML11/8	0000F	ML11/8	MLML8/11				Address decoder
ML10/11	U9FH	ML10/11	ML11/9				Address decoder

Signal	Signature	Test Node						Remarks
		MODULE IDENT AND 3-STATE BUFFER (ML9)						
ML9/2	U399	ML9/2						ID
0V	0000	ML9/4	ML9/6	ML9/8	ML9/11			ID
0V	0000	ML9/13	ML9/15					ID
ML9/17	U399	ML9/17	ML7/2	ML7/7	R131	R133	D18	Overload
		DATA LATCH (BITE Multiplexer) (ML8)						
Q0	026A	ML8/2	ML13/10					CONTROL A
Q1	8036	ML8/5	ML13/11					CONTROL B
Q2	4118	ML8/6	ML13/14					CONTROL C
Q3	218U	ML8/9	ML13/13					CONTROL D
ML8/12	11F4	ML8/12	R141					RF mute
ML8/15	0000	ML8/15	R122					RF amp
ML8/16	05U3	ML8/16	R119					Noise gen.
ML8/19	0000	ML8/19	R139					Ant. relay

ALIGNMENT

42 This procedure details the adjustments required for aligning the Front End Module.

Test Equipment

43 The following items of test equipment, as detailed in Chapter 2, are required for aligning the Front End Module:

(1) BITE Kit.
(2) Spectrum Analyser and Tracking Generator.
(3) Signal Generator.
(4) RF millivoltmeter.
(5) AC voltmeter.

Preliminary

44 Remove the Front End Module from the receiver and place it on the bench next to the receiver. Remove the top cover from the module to gain access to the preset components (leave the bottom cover fitted). Reconnect the module to the receiver using the extender assembly provided with the BITE Kit. Adjust the preset components according to the following alignment procedure.

3 - Section Low Pass Filter

45 Connect the tracking generator output, set to -10dBm, to the antenna input (SK2). Remove the shorting link from LK9. Connect the spectrum analyser input to LK9 (position B). Adjust coils L25,L24, and L23 for stopband notches (minimum amplitude) at the centre frequencies given below:

L25 : 77.80MHz
L24 : 40.97 MHz
L23 : 48.41 MHz

46 Repeat as necessary. Check that the insertion loss is less than 2 dB up to 30 MHz. Check that the stopband up to 100 MHz is better than 38 dB. Refit shorting link on LK9 position A.

4 - Section Low Pass Filter

47 Remove the shorting links from LK9 and LK5. Connect the tracking generator output, set to -10 dBm, to LK9 (position D). Connect the spectrum analyser input to LK5 (position D). Ensure that the RF amplifier is switched out of circuit. Adjust coils L12, L11 and L10 for stopband notches at the centre frequencies given below:

L12 : 46.53 MHz
L11 : 41.40 MHz
L10 : 57.88 MHz

48 Repeat procedure as necessary and then adjust coil L13 for minimum insertion loss up to 30 MHz with the spectrum analyser set to display the filter passband from 20 MHz to 30 MHz. Check that the insertion loss up to 30 MHz is less than 2 dB and that the stopband up to 100 MHz is better than 60 dB. Refit shorting links on LK9 position A and LK5 position C.

Overall 30 MHz Low Pass Filter

49 Remove the shorting link from LK5 and ensure that the RF amplifier is switched out of circuit. Connect the tracking generator output, set to - 10 dBm, to the antenna input (SK2). Connect the spectrum analyser input to LK5 (position D) to display the overall filter passband from 20 MHz to 30 MHz. Adjust L13 to achieve minimum insertion loss up to 30 MHz. Check that the insertion loss up to 30 MHz is less than 2 dB. Refit shorting link on LK5 position C.

1st LO 40 MHz High Pass Filter

50 Remove the shorting link from LK1. Connect the tracking generator output, set to -10 dBm, to PL4 (1st LO input). Connect the spectrum analyser input to LK1 (position A). Adjust coils L4 and L3 for stopband notches at the centre frequencies given below:

L4 : 17.60 MHz
L3 : 26.05 MHz

51 Repeat as necessary. Check that the insertion loss is less than 2.5 dB from 41.4 MHz to 71.4 MHz. Check that the stopband up to 26.05 MHz is better than 46 dB. Refit shorting link on LK1 position B.

1st Mixer/Roofing Filter

52 Remove the shorting links from LK5 and LK7. Connect the 1st LO input (PL4) to the 1st LO Synth. Module using the coaxial lead in the BITE kit and tune the receiver to 15.02 MHz. Connect the signal generator output, set to –20 dBm at a frequency of 15.02 MHz CW, to LK5 (position B). Connect the spectrum analyser input to LK7 (position D). Set the spectrum analyser frequency to 41.4 MHz.

53 With the mixer output signal displayed, adjust coils L8 and L9 to achieve maximum amplitude at 41.4 MHz. Repeat the alignment procedure as necessary with the spectrum analyser set for greater sensitivity.

54 Disconnect the signal generator from LK5 and measure its output level in dBm on the RF millivoltmeter. Note the reading and reconnect the signal generator to LK5 (position B). Substitute the RF millivoltmeter for the spectrum analyser and note the mixer output level as before.

55 Subtract the meter reading noted at LK7 from that noted at LK5 in order to obtain the mixer/filter insertion loss in dB. Ensure that this figure is less than 10 dB. Refit shorting links on LK5 position C and LK7 position C.

1st IF Amplfiers and (unadjusted) AGC Range

56 Remove the shorting links from LK7 and LK8. Connect the signal generator output, set to –77 dBm at a frequency of 41.4 MHz, CW, to LK7 (position B). Connect the spectrum analyser input to LK8 (position A). Set the AGC to manual and set the IF gain control and R16 fully clockwise. Set the cores of L16, L18, L22, L21, L20 and L19 approximately midway within the coil former.

57 Adjust coils L16, L18, L22, L21, L20 and L19 to give a maximum signal output at 41.4 MHz. Repeat alignment sequence as necessary with the spectrum analyser set for greater sensitivity.

58 Disconnect the lead from the signal generator and connect it to the tracking generator output, set to –20 dBm. Ensure that the filter characteristic is displayed on the analyser and set its output level at 41.4 MHz to the top of the analyser screen. Adjust coils L20 and L21 to obtain a filter shape such that the level at 38.6 MHz (2nd image frequency) is greater than –40 dB relative to the level at 41.4 MHz. Ensure that the level at 41.4 MHz does not drop by more than 2 dB whilst adjusting L20 and L21.

59 Disconnect the lead from the tracking generator and reconnect it to the signal generator output. Ensure that the output level at 41.4 MHz is –49 dBm ± 3 dB. Note the value.

60 Set the IF gain control fully counter-clockwise. Increase the signal generator output level from –77 dBm to achieve the same ouput level as noted in the previous paragraph. The (unadjusted) AGC range is given by the required increase in the signal generator output level, which should be greater than 65 dB. Refit shorting links on LK7 position C and LK8 position B.

Module Gain and AGC Adjustment

61 Set the IF gain control fully clockwise and switch the RF amplifier into circuit using the menu system. Ensure that the 1st LO input is connected to the 1st LO Synth. Module and the receiver is tuned to 15.02 MHz. Connect the 40 MHz input (PL3) to the Reference/BFO Module using the coaxial lead in the BITE kit.

62 Connect the signal generator output, set to -73 dBm at a frequency of 15.02 MHz, CW, to the antenna input (SK2). Connect the AC voltmeter to the 1.4 MHz IF output (PL2), terminated into 1 kohm, and set to read mV. Connect the digital multimeter to TP4 to measure the 1st IF AGC voltage . Carry out the following adjustment procedure to set the module gain (to 64 dB) and to adjust the 1st IF AGC characteristic.

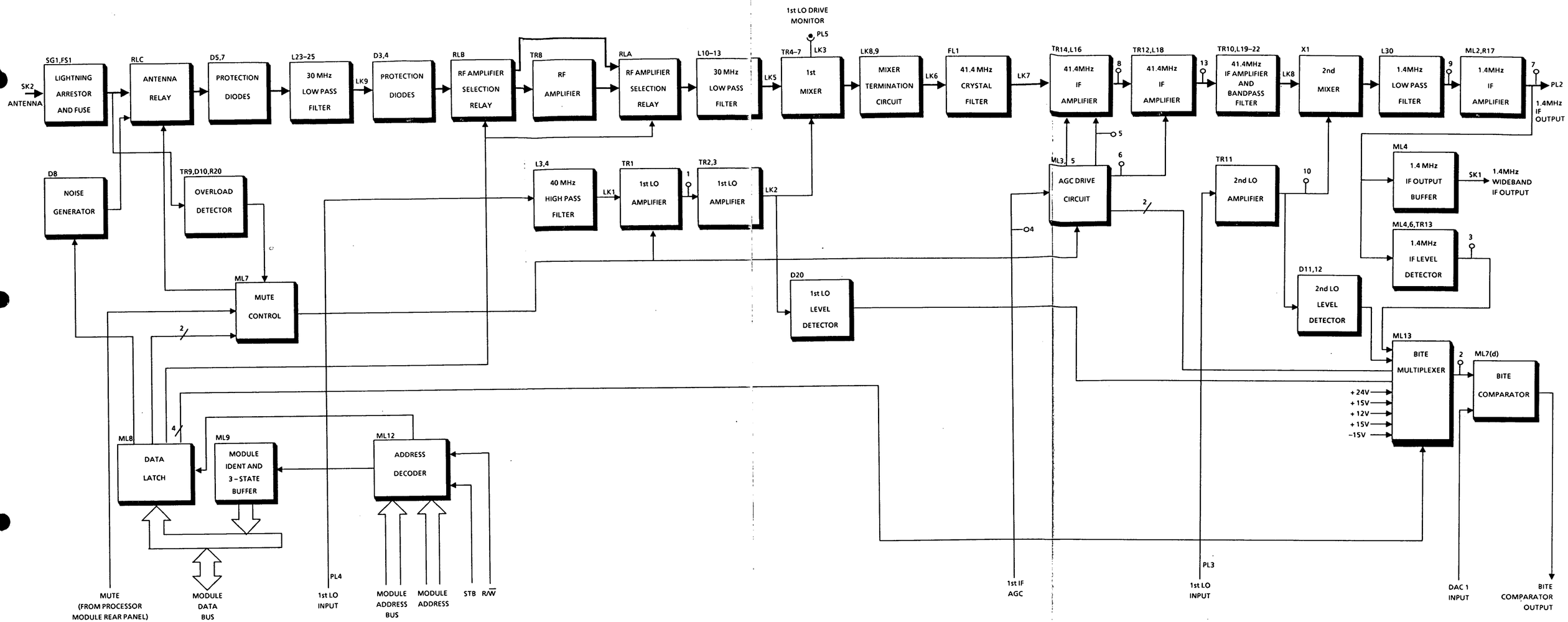
63 With R16 set fully clockwise and the 1st IF AGC voltage set to 10 V (i.e. maximum), adjust R17 to give an IF output of 90mV ± 2mV. Next adjust R16 to give a meter reading of 80mV ± 2mV. Set the AC voltmeter to read dBm and note the reading.

64 Adjust the IF gain control to give a 1st IF AGC voltage of 0V. Increase the signal generator output level from -73 dBm to achieve the same AC voltmeter reading as noted in para.62. The (adjusted) AGC range is given by the required increase in signal generator output level, which should be greater than 80 dB.

PARTS LIST

65 The Racal part number for a complete Front End Module is ST86486.

66 Information on the identification and handling of SMDs is provided in Chapter 2. The parts list for the Front End Module is as follows:



Front End Module: Block Diagram **Fig.6.3**

FTS 730-04 = Tx/Rx

BERT

FTS 727 = PROJ

CHAPTER 7

IF/AF MODULE

CONTENTS

TABLE

ILLUSTRATIONS

CHAPTER 7

IF/AF MODULE

INTRODUCTION

1 The IF/AF Module contains the 1.4 MHz filters, the second IF amplifier with AGC circuits and the demodulators with associated audio stages.

Fig 7.1 Receiver Block Diagram

MODULE DESCRIPTION

2 The following description should be read in conjunction with the IF/AF Module Block and Circuit Diagrams included with this chapter. Component references shown on the Block Diagram allow it to be related to the Circuit Diagram.

IF Filters

3 The IF/AF Module can accommodate up to five IF filters, the type and bandwidth of which are dependent on the receiver specification. For example, a typical receiver may be supplied with three symmetrical filters of 300 Hz, 1 kHz and 6 kHz plus two sideband filters of 2.7 kHz each.

4 In some versions of the receiver, additional symmetrical bandwidths may be obtained by offsetting the sideband filters so that they appear to be symmetrical. This is achieved by automatically shifting the lst LO synthesiser and BFO frequencies when the bandwidth is selected. Likewise, symmetrical bandwidths can also be offset to make them appear as sideband filters. The procedure for configuring these bandwidths is provided in this chapter.

5 The filters are bypassed when the 12 kHz bandwidth is selected and the selectivity is then determined by the roofing filter in the Front End Module.

6 The 1.4 MHz IF input is interfaced to all of the filters via an emitter follower BUFFER AMPLIFIER, the desired filter output being selected by diode switches in a FILTER SWITCHING circuit. In this circuit, unwanted filter outputs are shunted by forward biased diodes connected across the output, as determined by a logic low placed on select lines from the bus interface circuits. Unwanted filters are isolated from the others by series diodes which are reversed biased when the select lines are pulled down, thus blocking the select signal.

7 For the wanted filter the appropriate shunt diode is switched out of circuit by a logic high appearing on its select line. This allows the filter output signal to pass through the now forward biased series diode to the IF amplifier stages.

8 If ISB is fitted the output of FL5 is automatically routed to the ISB IF output when ISB is selected, instead of the main IF.

9 As a result of sideband inversion occurring in the 1st MIXER (Front End Module), the USB filter (FL5) output represents the LSB of the received signal.

IF Amplifiers

10 The selected IF filter output is amplified in a two-stage differential AGC CONTROLLED AMPLIFIER. This configuration provides high gain and an AGC range of 60 dB.

11 The gain of these two differential amplifiers is controlled by a variable current source formed by ML7(c), ML4(c) and associated components. In this circuit the current through ML4(c) is proportional to the 2nd IF AGC voltage on TP11.

12 A temperature compensated bias voltage for the two tail transistors, ML3(d) and ML3(c), of the two differential amplifiers is provided by R44, R46, R29 and ML3(e). A fixed bias is also provided for both amplifiers. This is derived from ML4(d) and applied to the base of ML3(a) and ML4(a).

13 When the AGC current through ML4(c) is zero, the voltages on the base of both ML3(a) and (b) in the first amplifier stage are equal and the two transistors pass the same current giving maximum gain. As the 2nd IF AGC voltage increases, the AGC current also increases. A voltage drop occurs across R38, reducing the base voltage and therefore the current through ML3(b). This reduces the amplifier gain. The same action occurs in the second amplifier stage.

14 Thermistor R7 is included in the current source to compensate for the temperature dependent characteristics of the transistors in the two amplifier stages. The thermistor varies the AGC current in response to changes in temperature and thereby stabilises the gain of the IF amplifiers.

15 The amplified IF output is passed through an LC WIDEBAND FILTER and applied to emitter-follower BUFFER AMPLIFIER stages to provide 1.4 MHz at the rear panel IF OUT socket (SK1) at a level of 100 mV into 50 ohms.

16 A buffered IF output is also taken to the demodulation circuits to produce the audio outputs.

Mode Selection

17 For AM and FM modes the MODE SELECT routes the main IF signal to a LIMITER AND FM DISCRIMINATOR. In the case of CW and SSB modes the BFO signal is selected instead to provide the necessary carrier frequency for demodulation of the IF signal.

Demodulation

18 In the FM mode, the modulated IF signal is applied to the LIMITER AND FM DISCRIMINATOR comprising ML1, ML35(a) and associated components. The discriminator employs a quadrature tuned circuit centred on 1.4 MHz and adjustable by means of L4. The resultant amplified audio signal is then passed to the AUDIO SWITCH.

19 In the AM mode, the IF signal is passed through the LIMITER section and a further LIMITING AMPLIFIER. This removes any amplitude modulation and provides a carrier signal at the level required by the PRODUCT DETECTOR. The IF signal is fed to the signal port and the PRODUCT DETECTOR acts as a synchronous AM detector.

20 For SSB and CW demodulation, the BFO signal is passed through the LIMITER and LIMITING AMPLIFIER and fed to the carrier port of the PRODUCT DETECTOR. The IF signal is fed directly to the signal port and is mixed with the BFO signal in the PRODUCT DETECTOR to produce an audio output.

21 The appropriate audio output is then selected by the AUDIO SWITCH and passed to the AF stages.

AF Stages

22 The audio is first passed through an active AUDIO LOW PASS FILTER with a 3 dB point occurring at approximately 10 kHz, amplified in an AUDIO AMPLIFIER AND SQUELCH SWITCH circuit, and then directed on to the audio outputs and LINE OUTPUT AMPLIFIER by an AUDIO SELECT circuit. This circuit switches the audio through emitter follower transistor amplifiers to provide a choice of internal or external audio for the front panel loudspeaker and provide audio to optional modules. The audio levels are monitored by an AUDIO DETECTOR AND METERING circuit which rectifies and filters the audio signal to provide a DC level to the BITE multiplexer.

23 The audio power amplifier for driving the final audio outputs is contained in the Front Panel Assembly together with the volume control.

24 A two-stage operational amplifier is used as the LINE OUTPUT AMPLIFIER, its gain being adjustable by means of a preset potentiometer accessible through the top of the module. The line output is made available from a 600 ohm centre-tapped transformer.

AGC Circuit

25 The AGC circuit controls the gain of the 1st and 2nd IF amplifiers in order to maintain a constant output from the receiver as the antenna input level changes. The gain of the IF amplifiers is controlled in such a way as to obtain optimum signal to noise ratio over the entire sensitivity range of the receiver.

AGC Detection

26 The AGC DETECTOR is fed with the IF signal and provides an output in the form of a level which follows the modulation envelope of the signal.

27 Two PEAK DETECTORS followed by FAST and SLOW INTEGRATORS form the basis of the AGC control circuits.

28 When the antenna input signal increases, the output of PEAK DETECTOR 1 rises above the voltage applied by the AGC REFERENCE to the FAST INTEGRATOR, ML9(a) Pin 3, causing the output on TP19 to fall. The time constant of the integrator is determined by C68 and R98.

29 At the same time, the output of PEAK DETECTOR 2 feeds the SLOW INTEGRATOR whose output voltage falls more slowly than the FAST INTEGRATOR because of the longer time constant determined by C62 and R95.

30 In the AGC/MANUAL GAIN COMBINER the outputs of both integrators are combined such that the smallest voltage is chosen to take control. This chosen output voltage is then used, after further processing, to control the gain of the 1st and 2nd IF amplifiers.

31 After an increase in input signal, the FAST INTEGRATOR output voltage will rapidly reduce the receiver gain to restore the receiver output to the correct level. However, if it remained in control of the gain, the AGC would tend to 'follow' the signal modulation and cause distortion. To prevent this, the SLOW INTEGRATOR takes control when its output drops below that of the FAST INTEGRATOR. It does this because its PEAK DETECTOR is fed with a larger output from the AGC DETECTOR output potential divider chain (R148, R149, R153, R155).

32 When the SLOW INTEGRATOR takes control the action of ML9(c) holds the FAST INTEGRATOR output at a slightly higher level than the SLOW INTEGRATOR output, ready to respond again in the event of a further increase in signal level.

33 In addition to providing good distortion performance, this system also reduces the time the receiver is de-sensitised after a short noise spike. This is because the SLOW INTEGRATOR does not have time to respond fully and therefore have to decay with its long time constant.

34 Three AGC DECAY TIME CONSTANTS are normally switched into circuit to provide a choice of short, medium or long discharge times for the SLOW INTEGRATOR when the signal level falls.

35 When the short decay time constant is selected for AM and FM modes, PEAK DETECTOR 2 is bypassed so that the mean carrier level as detected by the AVERAGE DETECTOR is used to control the SLOW INTEGRATOR. The fast integrator circuit is switched out in this mode.

Manual Gain

36 The MANUAL GAIN CONTROL voltage derived from the processor DAC 2 line is also combined in the AGC/MANUAL GAIN COMBINER along with any diversity AGC voltage from another receiver. A separate rear panel manual gain input is also provided for use with external equipment. This allows, for example, a control voltage from DF equipment to override the combined output voltage.

AGC Distribution

37 For the entire input signal range of the receiver the AGC DISTRIBUTION circuit distributes the AGC control voltage between the 1st and 2nd IF amplifiers as shown in Fig. 7.2 in order to achieve optimum receiver noise performance.

38 For the first 40 dB of receiver gain reduction above the AGC operating threshold the gain control is provided in the 2nd IF. Gain control for the next 80 dB is then in the 1st IF, the remaining 20 dB of gain control being again in the 2nd IF.

39 With AGC selected a signal below the AGC operating threshold results in the voltage present at the combined AGC output (TP20) being set to maximum (about +10 V). This sets the 2nd IF AGC voltage to minimum and the 1st IF AGC voltage to maximum to give maximum receiver gain. As the signal level increases to above the AGC operating threshold, ML7(a) output increases to reduce the 2nd IF gain.

40 Over the first 40 dB of AGC control the threshold level set by preset R4 and applied to integrator ML10(b) is higher than the 2nd IF AGC voltage. This holds the integrator output at 10 V and the 1st IF AGC voltage remains at maximum for maximum 1st IF gain.

41 When this threshold is exceeded, ML10(b) starts to ramp down causing the 1st IF AGC voltage to decrease and therefore reduce the 1st IF gain. This voltage is also routed back to affect the threshold being applied to ML7(a), resulting in its voltage output, and therefore the 2nd IF gain, being held constant.

42 When the 1st IF AGC voltage reaches minimum, ML7(a) output once again increases to provide a reduction in 2nd IF gain up to the limit of the AGC range.

43 If ISB is fitted the ISB AGC is combined with the main AGC in this circuit and the largest of the two, representing the strongest signal, controls the 1st IF gain. Each 2nd IF for the sidebands is then controlled separately with 40 dB of independence between them.

AGC Overload Detection

44 Since the AGC is derived from the filtered IF signal, front end overload could occur if the AGC fails to act on a strong signal outside the bandwidth of the selected filter but within the bandwidth of the roofing filter. An OVERLOAD AGC DETECTOR responds to this condition and drives the 1st IF AGC to cause a reduction in gain.

AGC Hang

45 With long AGC selected, a drop in signal level causes the AGC to 'hang' for two seconds before decaying. This function is performed by an AGC HANG circuit to which the AGC REFERENCE is applied.

46 Under AGC control, ML17(c) output charges C76 via D19. ML17(d) output is high, switching in the AGC DECAY TIME CONSTANTS to provide normal decay on the incoming signal. As soon as the signal level drops, ML17(c) output goes low. This in turn causes ML17(d) output to go low, switching the AGC DECAY TIME CONSTANTS out of circuit and the AGC hangs. This situation continues until C76 discharges via R122 and falls below the voltage set by R129 and R132, causing ML17(d) output to go high again and reconnecting the AGC DECAY TIME CONSTANTS.

47 If AGC hang is not required, TR5 is switched on to clamp ML17(d) into its high output state.

AGC Dump

48 Dump latch ML15(b) in the LINK 11 AGC AND DUMP CONTROL circuit is set by the processor after a frequency entry or mode change, or on receipt of a command from the rear panel or by remote control. The latch output activates the AGC DUMP thus dumping the AGC control voltage. This results in a rapid increase in gain until the IF output signal is detected once more by the AGC HANG circuit to reset the latch.

49 With the special data transmission LINK 11 AGC facility selected the decay characteristic of the AGC control voltage is controlled by the action of comparator ML11(b) and latch ML15(b). This occurs only in the presence of a signal 10 dB above the AGC threshold as defined by R102, R109 and causes the output of comparator ML11(b) to be high when LINK 11 AGC is enabled. .

50 A fall in signal level is sensed by ML11(d) clocking ML11(b) output to the output of latch ML15(b), thereby activating AGC DUMP and causing a rapid discharge of the AGC control voltage. The latch output also charges C74, via R121, to provide an automatic reset facility.

Squelch and COR Operation

51 The squelch circuit operates the SQUELCH SWITCH to de-mute the audio outputs and provides an open collector 'COR' output on the rear panel connector of the Processor Module when a signal is detected above the squelch level (set by the IF gain control). Squelch is inoperative in manual AGC mode.

52 In normal AGC mode the squelch level may be set in the range -20 dB to +40 dB relative to the AGC threshold. This level is established by the DAC 2 input from the processor. In variable threshold AGC mode the squelch level is automatically set to be 3 dB above the AGC threshold.

53 For squelch levels above the AGC threshold a voltage on the DAC 2 input is taken via the MANUAL GAIN CONTROL buffer and compared in SQUELCH THRESHOLD DETECTOR 1 with the DIV AGC control voltage from the AGC/MANUAL GAIN COMBINER . In the event of squelch levels below the AGC threshold the DAC 2 voltage is compared in SQUELCH THRESHOLD DETECTOR 2 with a voltage derived from the AGC DETECTOR.

54 A SQUELCH COMPARATOR monitors the output of the two squelch threshold detectors and, when a signal exceeds the squelch level, presents a logic low status signal. The Processor reads the signal via the module data bus, de- muting the audio output and switching the COR output on.

55 The Processor also regularly monitors the SQUELCH COMPARATOR to detect when the signal drops below the squelch level and then, after a preset time, mutes the audio and switches off the COR.

Bus Interface

56 A unique hardwired code is received on the Module Address input to the IF/AF Module via the motherboard. This code is used by the ADDRESS DECODER to detect addresses on the Module Address Bus from the Processor Module and then produce read or write pulses according to the status of the R/W input. These pulses allow the Processor to read data from the 3- STATE BUFFER or write data to any DATA LATCH, using the Module Data Bus. Pulses on the strobe input ensure correct timing of write pulses. The 3-STATE BUFFER gives the Processor access to the IF/AF Module identification code and also the squelch status. The DATA LATCH outputs are used to select various functions throughout the module and to control a BITE MULTIPLEXER.

BITE Measurement System

57 The BITE measurement system, comprising the BITE MULTIPLEXER operating in conjunction with a BITE COMPARATOR, allows the Processor Module to measure various voltages and operating levels in the IF/AF Module. The voltage to be measured is selected by the BITE MULTIPLEXER and compared in the BITE COMPARATOR with a voltage generated by a digital to analogue converter (DAC) in the Processor Module. The Processor measures the level of the selected voltage by applying voltages representing upper and lower limits to the comparator and then monitoring the resulting output.

58 For some BITE tests, test signals generated within the receiver are injected into the IF/AF Module. These signals include a BFO signal applied via a BFO SWITCH AND ATTENUATOR to the filters so that the IF amplifier gain, the IF filter passband, and the 2nd IF AGC operation may be checked. For checking the demodulators a test signal is obtained from the Front End Module by tuning the receiver to 0 MHz and modulating this signal.

IF FILTER CONFIGURATION

59 The receiver requires the following data defining the IF crystal filters fitted to the receiver. The information is stored in the EEPROM on the Processor Module.

(1) Bandwidth number.
(2) Filter position.
(3) Filter passband limits.
(4) Offset frequency.

60 This data may be entered from the front panel of the receiver using the menu system. For remotely controlled receivers the data may be entered on the front panel of the controller and sent to the receiver via the remote control link.

61 Each bandwidth provided by the IF filters is defined as being either USB, LSB, or SYM (symmetrical) and has a unique bandwidth number assigned to it. This number is used in remote control systems to select the required bandwidth. To ensure that the correct filter is selected, each filter position on the board must also be defined. This is the "FL" number which appears on the printed circuit board. Information defining the upper and lower filter passband limits is also required.

62 Table 7.1 indicates the bandwidth information which is entered for receivers containing the standard set of crystal filters. Note that the 2.7 kHz symmetrical bandwidth is obtained by offsetting the 2.7 kHz USB filter. In addition, the 12 kHz symmetrical bandwidth is determined by the roofing filter in the Front End Module (bypass mode). The bandwidth information for other filter options is contained in Appendix A.

TABLE 7.1

Bandwidth Configuration Data

(for Filter Option Code "LA")

Filter Type	Displayed Bandwidth	BW No.	Filter Position	Passband Freq.		Offset Freq.
				Lower	Upper	
USB	2.7 kHz	00	04	300	3000	0
LSB	2.7 kHz	00	05	-3000	-300	0
SYM	300 Hz	00	03	-150	150	0
SYM	1.0 kHz	01	02	-500	500	0
SYM	2.7 kHz	02	04	-1350	1350	-1650
SYM	6.0 kHz	03	01	-3000	3000	0
SYM	12.0 kHz	04	06	-6000	6000	0

63 The procedure for configuring the IF filters for the above parameters is as follows:

(1) Press MENU until the following level 6 menu options are presented on the right-hand display:

BW SERIAL FREQ S/W
PORTS RES I/D

(2) Press M1 to select the BW option and the security code prompt appears.

(3) Enter the receiver security code and the following menu is presented:

USB LSB SYM EXIT

(4) Select the required option. For example, to configure the USB filter in the standard receiver, proceed as follows.

(5) Press M1 to select USB.

(6) The receiver requests the bandwidth number for use in remote control systems.

Press 0 0 ENTER

(7) The following menu is presented:

Insert Remove

(8) Press M1 to select Insert.

(9) The receiver requests the filter position to be entered. For the USB filter in the standard receiver:

Press 0 4 ENTER

(10) The receiver requests the lower passband frequency.

Press 0 3 ENTER to program in + 300 Hz.

(11) The receiver requests the upper passband frequency.

Press 3 ENTER to program in +3000 Hz.

(12) The receiver requests the frequency offset.

Press 0 ENTER to program in zero offset.

(13) The display returns to the menu illustrated at step 3. If required, repeat the above procedure for any other bandwidths which are to be configured.

64 A frequency offset facility is available to make sideband filters produce symmetrical bandwidths and symmetrical filters produce either upper or lower sidebands. For example, to configure a 300 Hz symmetrical filter so that it is centred on 2 kHz in the upper sideband, follow the example given above using the following data:

Step (5) - select USB
Step (6) - enter the required bandwidth number
Step (8) - select "Insert"
Step (9) - enter the appropriate filter position (03 for the 300 Hz filter in the standard receiver)
Step (10) - program in +1850 Hz
Step (11) - program in +2150 Hz
Step (12) - program in +2000 Hz

65 To remove a bandwidth from the memory, follow steps (1) to (6), entering the bandwidth number which is no longer required at step (6). When the step (7) menu is presented, select "Remove" to erase the bandwidth data from the memory.

FAULT FINDING

General

66 Fault finding techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the IF/AF Module is contained in the following sections.

BITE Tests

67 The following BITE tests for the IF/AF Module are arranged in the order in which they are performed or presented for selection.

TEST NUMBER	:	301
TITLE	:	BITE hardware
PERFORMED	:	Continuous, unit confidence test, select test
DESCRIPTION	:	DAC 1 line is set to 2.55 volts (i.e. max). BITE multiplexer input X1 (+ 5volts) is selected and the output of the BITE comparator is checked to ensure that it is low.
LIMITS	:	Less than 0.8 V at TP5.
FAULT DIRECTORY	:	Fault No. 2

TEST NUMBER : 302,303,304,305

TITLE : + 5V rail, +15V rail, +10V rail, -15V rail.

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : The appropriate BITE multiplexer input is selected and the supply voltage is checked.

LIMITS :

Test No.	Supply	Mux. Input	Mux. Limits (TP5)	
			Lower	Upper
302	+5 V	X2	1.78 V	2.22 V
303	+15 V	X3	1.70 V	2.21 V
304	+10 V	X4	1.90 V	2.36 V
305	- 15 V	X5	1.65 V	2.24 V

FAULT DIRECTORY : Fault No. 4

TEST NUMBER : 306

TITLE : IF amplifier

PERFORMED : Unit confidence test,select test.

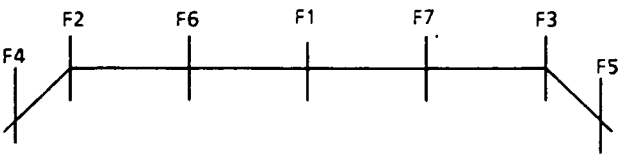
DESCRIPTION : The gain of the 2nd IF amplifier is checked by tuning the receiver to 5.02 MHz and switching the BFO input at 1.4 MHz (receiver BFO tuned to 0 kHz) via the IF filter bypass, through the IF amplifiers and into the AGC detector. BITE multiplexer input X10 is selected and DAC 2 input is adjusted to give a reading of between 1.90 and 1.94 V at X10. BITE multiplexer input X7 is then selected to measure the AGC detector output.

LIMITS :

Mux. Input		AGC Det. Output (TP9)	
Lower	Upper	Lower	Upper
0.2 V	-	0.2 V	-

FAULTY DIRECTORY : Fault No. 6

TEST NUMBER	:	307
TITLE	:	IF filter
PERFORMED	:	Unit confidence test, select test
DESCRIPTION	:	The receiver is tuned to 5.02 MHz. Level checks of all configured filters are then performed using the BFO as the test signal for the following frequencies:



F1	:	centre frequency
F2	:	lower passband cut off
F3	:	upper passband cut off
F4,F5	:	-12 dB point

LIMITS	:	F1	:	reference level
		F2,F3,F6,F7	:	± 6 dB relative to reference
		F4,F5	:	-12 dB relative to reference
FAULTY DIRECTORY	:	Fault No. 7		

TEST NUMBER	:	308
TITLE	:	2nd IF AGC
PERFORMED	:	Unit confidence test, select test
DESCRIPTION	:	The receiver is tuned to 5.02 MHz. The first configured filter is selected and injected with the BFO signal. The first check ensures that the DIV AGC is between 1.8 and 2.1 V. If the voltage is less than 1.8 V, the BFO frequency is moved down the filter passband until the starting condition is reached. The BFO is then swept in 50 Hz steps. This attenuates the BFO signal, causing the AGC to increase the 2nd IF gain to compensate. For each step, BITE multiplexer inputs X7 and X10 are selected to measure the detected AGC and diversity AGC outputs. The detected AGC should remain constant as the diversity AGC increases. When the AGC runs out of range, the diversity AGC reaches its maximum and stays constant and for subsequent steps of the BFO the detected AGC output falls. The change in levels indicates that the 2nd IF AGC has a minimum of 30 dB AGC range (typically 40 dB).
FAULT DIRECTORY	:	Fault No. 8

TEST NUMBER	:	309
TITLE	:	AGC detector
PERFORMED	:	Unit confidence test, select test.
DESCRIPTION	:	The receiver is tuned to 0 Hz to provide a test signal to the IF/AF Module. Short AGC and the peak detectors are selected. BITE multiplexer input X7 is selected to measure the AGC detector output level. The average detector is then selected and the output of the average detector is measured once again.
LIMITS	:	Peak detector output between 1.25 and 1.85 V. Average detector output ±0.3V of peak detector output.
FAULT DIRECTORY	:	Fault No. 9

TEST NUMBER	:	310
TITLE	:	AGC distribution
PERFORMED	:	Unit confidence test, select test.
DESCRIPTION	:	The IF/AF Module is set to manual gain and BITE multiplexer inputs X10 (diversity AGC), X9 (2nd IF AGC) and X8 (1st IF AGC) are selected in turn at various settings of the manual gain. The levels are measured to ensure the correct distribution of gain control voltages.
LIMITS	:	

Manual Gain Setting	Multiplexer Inputs		
	X10	X9	X8
2.55V	1.76V - 2.55V	0V - 0.3V	1.76V - 2.55V
2.09V	1.57V - 2.51V	0.3V - 0.7V	1.76V - 2.55V
1.86V	1.38V - 2.33V	0.6V - 1.3V	1.65V - 2.55V
1.63V	1.20V - 2.80V	0.7V - 1.3V	1.30V - 2.30V
1.40V	1.02V - 1.68V	0.7V - 1.3V	0.83V - 1.61V
1.16V	0.82V - 1.42V	0.7V - 1.3V	0.36V - 0.90V
0.93V	0.64V - 1.15V	0.7V - 1.4V	0V - 0.40V
0.70V	0.46V - 0.90V	1.1V - 1.9V	0V - 0.30V

FAULTY DIRECTORY	:	Fault No. 10

TEST NUMBER	:	311
TITLE	:	AGC decay
PERFORMED	:	Unit confidence test, select test.
DESCRIPTION	:	The receiver is tuned to 0 Hz to provide a test signal to the IF/AF Module and the filter bypass is selected. BITE multiplexer input X10 is selected to measure the diversity AGC level. The test signal is then removed by tuning the receiver to 5.02 MHz and the diversity AGC is measured again after a delay appropriate to the decay selected. In all cases, the level is checked to ensure that it has increased by at least 350 mV (30 dB).
LIMITS	:	For 350 mV increase: Short 90 ms Medium 400 ms Long 2.5 ms Link 11 42 ms
FAULT DIRECTORY	:	Fault No. 11

TEST NUMBER	:	312
TITLE	:	AGC hang
PERFORMED	:	Unit confidence test, select test
DESCRIPTION	:	The receiver is tuned to 0 Hz to provide a test signal. The IF/AF Module is set to filter bypass and short decay with hang. BITE multiplexer input X10 is selected to measure the diversity AGC level. The test signal is then removed by tuning the receiver to 5.02 MHz. After 1.2 seconds the diversity AGC level is again measured to check that it is within 50 mV of the first reading. After a further 1.8 seconds another measurement is made to check that the level has increased by at least 350 mV above the first reading.
FAULT DIRECTORY	:	Fault No. 11

TEST NUMBER	:	313
TITLE	:	AGC dump
PERFORMED	:	Unit confidence test, select test
DESCRIPTION	:	The receiver is tuned to 0 Hz to provide a test signal. The IF/AF Module is set to filter bypass. The long AGC time constant is also selected with AGC hang disabled. BITE multiplexer input X10 is selected to measure the diversity AGC level ensuring it is less than 1.63 V. The test signal is then removed by tuning the receiver to 5.02 MHz followed by an AGC dump. The diversity AGC level is again measured after a 25 ms delay ensuring that it is greater than 1.86V.
FAULT DIRECTORY	:	Fault No. 12

TEST NUMBER	:	314
TITLE	:	Product detector
PERFORMED	:	Unit confidence test,select test
DESCRIPTION	:	The receiver is tuned 0 Hz to provide a test signal. The IF/AF Module is set to filter bypass, CW mode and short time constant. A 1 kHz audio tone is produced by tuning the BFO to 1 kHz (1.401 MHz input signal). BITE multiplexer input X6 is selected to measure the audio detector output level.
LIMITS	:	0.54 V to 2.4 V at the BITE multiplexer input.
FAULT DIRECTORY	:	Fault No. 13

TEST NUMBER	:	315
TITLE	:	AM detector
PERFORMED	:	Unit confidence test, select test.
DESCRIPTION	:	The receiver is tuned to 0 Hz to provide a test signal. The IF/AF Module is set to filter bypass, AM mode and short time constant. The test signal is switched on and off by selecting and deselecting buffer amplifier TR1 to produce a 500 Hz 100% modulated AM signal. BITE multiplexer input X6 is selected to measure the audio detector output level.
LIMITS	:	0.54 V to 2.4 V at the BITE multiplexer input.
FAULT DIRECTORY	:	Fault No. 14

TEST NUMBER	:	316
TITLE	:	FM detector
PERFORMED	:	Unit confidence test, select test.
DESCRIPTION	:	The receiver is tuned to 0 Hz to provide a test signal. The IF/AF Module is set to filter bypass, FM mode and short time constant. The audio amplifier in the IF/AF Module is selected to obtain an extra 10 dB of audio gain. The test signal is switched in frequency between 0 Hz and 1kHz at a rate of 20 ms. This produces a frequency modulated signal of 1 kHz deviation and 50 Hz tone. BITE multiplexer input X6 is selected to measure the audio detector output level.
LIMITS	:	Greater than 0.54 V at the BITE multiplexer input.
FAULT DIRECTORY	:	Fault No. 15

Fault Directory

68 Use the following fault directory to identify the fault condition and take the necessary corrective action. Note that all inputs to the module are assumed to be correct.

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
1	Fails to run BITE tests for IF/AF Module.	Address decoding/module ident. not responding.	Check address decoding/module ident logic operation using signature analysis routine if necessary.
2	BITE hardware fault.	Comparator/multiplexer inoperative.	Use BITE test 301 to check comparator operation. Select all BITE tests for this module to check multiplexer operation for all analogue inputs. Use signature analysis routine to check multiplexer addressing.
3	BITE indicates failure but manual check shows no fault.	(a) BITE hardware fault. (b) Faulty BITE detector.	(a) As above. (b) Check operation of suspect BITE detector.
4	Power supply fault within module.	(a) Faulty component drawing excess current or open circuit choke L1 to L3. (b) 10V regulator on module faulty.	(a) Locate and replace faulty component. (b) Check voltages around ML2, ML17(a) and TR9.
5	Unable to select one or more functions	Module interface faulty	Check status of appropriate select line using signature analysis routine or oscilloscope.
6	Poor sensitivity	Low gain in signal path.	Run IF amplifier BITE test (306). Follow the IF gain check procedure.
7	Filter selectivity fault	(a) Filter configuration data incorrect. (b) Filter missing, damaged or fails to meet specification. (c) Filter switching circuit not functioning.	(a) Check configuration data (see para 59) (b) Carry out selectivity check (Chapter 4). (c) Check circuit voltages and control line levels (using oscilloscope) with each filter selected in turn.
8	Insufficent 2nd IF AGC range.	(a) AGC distribution incorrect. (b) Low 2nd IF gain.	(a) See Fault No. 10. (b) See Fault No. 6.
9	Detected AGC output incorrect.	(a) AGC detector inoperative. (b) Low 2nd IF gain	(a) Check voltage levels around circuit. (b) See Fault No. 6.
10	Incorrect manual gain control	(a) DAC 2 unable to set manual gain levels. (b) AGC distribution not functioning or set up correctly.	(a) Check voltage levels around manual gain control circuit. (b) Follow the AGC distribution check procedure and then check alignment.
11	AGC time constants incorrect	(a) AGC selection logic faulty (b) Slow integrator inoperative.	(a) Check switching outputs of logic control circuit. (b) Follow the AGC time constant check procedure.

Fault Directory (continued)

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
12	No AGC dump	Control voltages to link 11 and AGC dump control incorrect or AGC dump switches inoperative.	Check voltages around these circuits in accordance with the AGC time constant check procedure.
13	No CW/SSB demodulation	(a) Product detector faulty. (b) Audio select switch faulty. (c) Limiter faulty (ML1). (d) Audio low pass filter or audio select faulty.	(a) Check circuit voltages. Check IF present on TP16 and carrier present on TP10. (b) Check control voltage and signal flow. (c) Check carrier present on TP10. (d) Check signal flow path to TP2.
14	No AM demodulation.	(a) Mode select switch faulty if CW/SSB signals are detected. (b) Limiter (ML1), product detector, low pass filter, or audio select faulty.	(a) Check control voltage and signal flow. (b) As Fault No. 13.
15	No FM demodulation	FM discriminator (ML1) or audio select switch faulty if CW/AM signals are detected.	Check circuit voltages.
16	Excessive in band IMPs.	Faulty IF filter, IF amp or AGC.	Follow the in band IMP check procedure.
17	Distorted audio	Faulty demodulators (ML1, ML24) or audio stages.	Follow the distortion check procedure.
18	Squelch inoperative	(a) Squelch switch not muting audio amplifier. (b) No squelch command to processor.	(a) Check control voltage. (b) Monitor TP13 and rotate IF gain control to check operation of squelch threshold detectors/comparator.
19	Poor overall selectivity.	(a) Filters suspect. (b) Misalignment in IF stages	(a) See Fault No. 7. (b) Follow alignment procedure.

IF Gain Check Procedure

69 Set the AGC to manual and turn the IF gain control fully clockwise. Check TP20 reads +10 V ± 250 mV. If not, carry out the AGC distribution check procedure. Select the filter bypass (12 kHz bandwidth). Inject a 1.4 MHz test signal of – 49 dBm (800 µV p.d.) at PL2 and terminate PL5 with 50 ohms to provide a 50 ohm impedance at PL2. Connect an RF millivoltmeter set to 50 ohms input impedance to SK1 and check that the reading is in accordance with trace 3 on the signal level chart (Fig.7.3). Repeat the above procedure with the IF gain control set for +8V ± 100 mV on TP20 and a signal input of –9 dBm (80mV p.d.), again repeating for +3V ± 100 mV on TP20 and +11 dBm (0.8V p.d.) at the IF input, as shown in Fig.7.3 (traces 1 and 2).

70 If the output fails to meet the level shown, use the signal level chart to check the gain of each stage with the RF millivoltmeter set to high impedance. If the checks reveal a fault in the AGC controlled stages, carry out the AGC distribution check procedure to verify the 2nd IF AGC control voltage. For a slight deviation in gain, adjust R5 as described in the alignment procedure in an attempt to meet specification.

AGC Distribution Check Procedure

71 Set the AGC to manual, remove any signal at PL2, and turn the IF gain control fully clockwise. Check that +10V ± 250 mV is present on TP20 and TP4, and 0V present on TP11. Refer to Fig.7.2 and check that the voltages on these test points follow the graph as the IF gain control is rotated counter clockwise. If the voltages fail to follow, continue as below.

72 At 40 dB gain reduction (8V ± 250 mV on TP20) the points marked on the graph are set by R4 as described in the alignment procedure. Before adjusting R4, carry out the following circuit checks:

(a) Check that the voltage drop across D13 is not excessive as this will increase the time TP4 stays at 10V.

(b) Check that the fixed bias on the non-inverting input of ML10(b) is 1.4V nominal, measured at TP21. If incorrect, the 1st IF AGC (TP4) may ramp down too soon.

(c) Check the feedback voltage from TP4 to ML7(a) pin 3. If incorrect this may prevent the 2nd IF AGC (TP11) reaching its plateau.

AGC Time Constant Check Procedure

AGC decay failure

73 Set the receiver to 0 Hz and CW mode. Select the filter bypass (12 kHz bandwidth) and short AGC. Check that the voltage on TP9 is 1.5 V ± 100 mV and ML10(a) pins 2 and 3 are at 1.1 V nominal. Remove the test signal by rapidly tuning the receiver to greater than 20 kHz and check that the voltages on TP9 and ML10(a) pin 2 decrease. While the AGC is regaining control, check that the voltage on TP18, and therefore the DIV AGC voltage (TP20), starts to ramp up at the rate given in the table below (a storage oscilloscope may be necessary for viewing the waveforms).

Time Constant	Voltage Change (Nominal)
Short	18.75 V/S
Medium	5V/S
Long *	0.6V/S
Link II data	47V/S
Link II normal	5V/S

* Note that a 2 second hang is automatically set in long AGC.

74 If the voltage at TP18 is correct but not at TP20, check that the manual gain voltage is not overriding the AGC/manual gain combiner.

AGC hang failure

75 Set the receiver to 0 Hz and CW mode. Select the filter bypass (12 kHz bandwidth) with long AGC. Check that the voltage on TP9 is 1.5V. Remove the test signal by rapidly tuning the receiver to greater than 20 kHz and check that the voltage on TP9 decreases. The voltage on TP18 and TP20 should remain constant (hang) for a nominal 2 seconds before decaying at 0.6 V/s.

76 If the check fails, run the AGC hang BITE test (312) and monitor the level on TP12 using an oscilloscope. This should drop from +15V down to 0V for a nominal 2 seconds before reverting back to +15V and the cycle repeated. If the 0V period deviates from the 2 seconds by more than ±0.5 seconds then check the time constant components C73 and R122. If the trace is always high, check that the select line is low, switching TR5 off and thus enabling the hang circuit. If the trace is always low, check C76 is discharging via D19 and check comparator ML17(d) pin 12 is at 2.6 V. For both cases of TP12 being high or low, check the comparator operation of ML17(c) and (d).

AGC dump failure

77 Set the receiver to 0 Hz and CW mode. Select the filter bypass (12 kHz bandwidth) with long AGC. Check that the voltage on TP9 is 1.5V. Remove the test signal by rapidly tuning the receiver to greater than 20 kHz, the voltages on TP18 and TP20 should hang (assuming no failure in the AGC hang circuit). Press the ENTER key before the hang period has expired (i.e. less than 1.5 seconds) to check that the AGC dump causes the voltages on these test points to rise rapidly to 10V ± 250 mV.

78 If this check fails, run the AGC dump BITE test (713) and monitor the waveform on TP14 and TP15 using an oscilloscope. A 20 ms positive-going dump pulse should be present on TP14. If this pulse is less than 10 ns or greater than 40 ms, check the time constant components C74 and R121. If the trace is always high, check C74 is charging via R121 and produces a positive-going pulse at TP15, via D20, to reset ML15(b). If the trace is always low, check that ML15(b) SET input is being asserted to allow dump operation. If these checks prove correct and the AGC is not being dumped, check that the AGC dump signal causes the AGC dump switches (TR4, ML8(a), (b)) to operate correctly.

In band IMP Check Procedure

79 Excessive IMPs may be caused by one of the following:

(1) Faulty IF filter: Measure the IMPs for each filter fitted to the module with the receiver set to long AGC to determine whether one filter is worse than others; replace suspect filter.

(2) Gain fault: If the above check shows that IMPs are poor for all filters, carry out the IF gain check procedure to check stage gain. If a stage is providing excessive gain, check the circuit voltages around suspect stage.

(3) AGC fault: Check suspect time constant using the AGC time constant check procedure. With the receiver tuned to 0 Hz, check that the voltage on TP18 is higher than that on TP19. This verifies that the fast integrator is not in control.

Distortion Check Procedure

80 If distortion is poor on FM only, suspect ML1. However, first try adjusting L4 for minimum distortion. If no improvement, check the FM discriminator circuit voltages before replacing.

81 If distortion is poor on AM, CW and SSB, suspect the product detector, ML24, checking its circuit voltages before replacing.

82 For poor distortion on all modes, check that a clean AGC voltage is present on TP11 and the remaining audio stages comprising the low pass filter, audio switching and output stages, do not introduce distortion to the demodulated audio signal.

Signature Analysis Routine

83 This routine checks that the module control signals are interfaced and decoded correctly from the module bus.

Processor module DIL switch settings: SW1,4,7 OFF
SW2,3,5,6,8 ON

Signature analyser connection and settings:

Start: 9A Extender assembly, negative trigger
Stop: 9A Extender assembly, negative trigger
Clock: 8A Extender assembly, positive trigger
Earth: 1A Extender assembly

Note : Signatures xxxxF signify a flashing probe indicator.

Signal	Signature	Test Node			Remarks
+5V	H9A0				
0V	0000				
		DATA BUS INTERFACE			
M-D0	654F	PL1/7A	R162	ML18/18 ML22/3	Module bus
M-D1	4764	PL1/7B	R163	ML18/16 ML22/6	Module bus
M-D2	P300	PL1/6A	R156	ML18/14 ML22/10	Module bus
M-D3	1PUA	PL1/6B	R157	ML18/12 ML22/14	Module bus
M-D4	UACU	PL1/5A	R152	ML18/9 ML19/3	Module bus
M-D5	089H	PL1/5B	R154	ML18/7 ML19/6	Module bus
M-D6	718F	PL1/4A	R150	ML18/5 ML19/10	Module bus
M-D7	4H04	PL1/4B	R151	ML18/3 ML19/14	Module bus
		ADDRESS DECODER			
M-A0	UF4A	PL1/12A	R177	ML30/14	Module address
M-A1	0CH4	PL1/12B	R178	ML30/10	Module address
M-A2	PU8U	PL1/11A	R175	ML30/6	Module address
M-A4	0000	PL1/10A	R172	ML27/10	Module address
M-A5	0001	PL1/10B	R173	ML27/12	Module address
M-A6	0001	PL1/9A	R169	ML27/13	Module address
M-A7	H9A0	PL1/9B	R170	ML27/15	Module address
0	0000	PL1/14A	R187	ML27/9	Module address
1	0000	PL1/14B	R188	ML27/11	Module address
2	0000	PL1/13A	R174	ML27/14	Module address
3	H9A0	PL1/13B	R185	ML27/1	Module address

Signature Analysis Routine (continued)

Signal	Signature	Test Node					Remarks
		ADDRESS DECODER					
M-R/W	3571	PL1/8B	R203	ML33/1	ML33/2	ML32/12	Module bus
M-STB	0000F	PL1/8A	R211	ML32/1			Module bus
A=B	H9A1	ML27/6	ML32/10	ML32/13			Addr. decoder
ML33/3	PFH	ML33/3	ML32/2				Addr. decoder
ML32/3	H9A0	ML32/3	ML32/4	ML32/5			Addr. decoder
ML32/6	0000F	ML32/6	ML32/9				Addr. decoder
ML32/8	H9A0	ML32/8	ML30/3				Addr. decoder
ML32/11	PFH0	ML32/11	ML18/1	ML18/19			ID Buffer
D	H9A0	ML30/4	ML29/11				Addr. decoder
C	PU8U	ML30/5	ML29/12				Addr. decoder
B	0CH4	ML30/11	ML29/13				Addr. decoder
A	UF4A	ML30/13	ML29/10				Addr. decoder
		INTERNAL DATA BUS					
D0	654F	ML22/4	ML20/4	ML25/4	ML23/4	ML28/4	Data bus
D1	4764	ML22/5	ML20/6	ML25/6	ML23/5	ML28/5	Data bus
D2	P300	ML22/11	ML20/8	ML25/8	ML23/8	ML28/8	Data bus
D3	1PUA	ML22/13	ML20/10	ML25/10	ML23/10	ML28/10	Data bus
D4	UACU	ML19/4	ML20/16	ML25/16	ML23/16	ML28/16	Data bus
D5	089H	ML19/5	ML20/18	ML25/18	ML23/18	ML28/18	Data bus
D6	718F	ML19/11	ML20/20	ML25/20	ML23/20	ML28/20	Data bus
D7	4H04	ML19/13	ML20/22	ML25/22	ML23/22	ML28/22	Data bus
		DATA LATCH (BITE Selection) (ML28)					
0V	0000	ML28/1	ML28/3	ML28/13	ML28/15		
ML28/5	59FP	ML28/5	ML31/10				CONTROL A
ML28/7	HUC3	ML28/7	ML31/11				CONTROL B
ML28/9	9F8H	ML28/9	ML31/14				CONTROL C
ML28/11	3H12	ML28/11	ML31/13				CONTROL D
ML29/3	0000F	ML29/3	ML28/2	ML28/14			Latch Strobe
		DATA LATCH (Audio Selection) (ML28)					
MM	6HHH	ML28/17	ML8/12				AGC Threshold
J	F5CA	ML28/19	ML34/9				Audio select
CC	1189	ML28/21	ML39/6				Audio mute
A	6PA5	ML28/23	R19				Main IF select

Signature Analysis Routine (continued)

Signal	Signature	Test Node			Remarks
		DATA LATCH (AGC Selection) (ML23)			
EE	11FC	ML23/5	ML12/13		Peak 1 det.
FF	6529	ML23/7	ML12/6		Averg. det.
GG	5U58	ML23/9	ML12/5		Peak 2 det.
HH	F260	ML23/11	ML8/6		Manual gain
II	0FUF	ML23/17	ML13/5		AGC decay TC
JJ	6CC2	ML23/19	ML13/6		AGC decay TC
KK	H815	ML23/21	ML13/12		AGC decay TC
LL	8U21	ML23/23	R124		Hang select
ML29/2	000F	ML29/2	ML23/2	ML23/14	Latch Strobe
		DATA LATCH (Mode/Audio selection) ML25			
Y	75UU	ML25/5	ML34/11		Mode select
L	UC6U	ML25/7	ML34/10	R201	Mode select
S	CF27	ML25/9	ML36/13		Audio select
P	1U83	ML25/11	ML36/6		Audio select
N	4P51	ML25/17	ML36/12		Audio select
R	66C8	ML25/19	ML36/5		Audio select
M	72FF	ML25/21	ML39/12		Audio/squelch
DD	APC1	ML25/23	R113		Link 11
ML29/14	0000	ML29/1	ML25/2	ML25/14	Latch Strobe
		DATA LATCH (Filter Decode and Selection)			
ML20/5	F610	ML20/5	ML5/10		Filter decoder
ML20/7	76A8	ML20/7	ML5/13		Filter decoder
ML20/9	2PU4	ML20/9	ML5/12		Filter decoder
V	H4FH	ML20/17	R24		ISB out select
W	7UF6	ML20/19	R16		IF out select
X	2A43	ML20/21	R28		IF out select
H	447P	ML20/23	R260		BFO select
B	82HA	ML20/11	R10		FL5 select
C	P536	ML5/3	R27		FL4 select
D	15F5	L5/14	R39		FL3 select
E	8AP2	ML5/2	R48		FL2 select
F	8H45	ML5/15	R57		FL1 select
G	4571	ML5/1	R37		Bypass select
ML29/1	0000F	ML29/1	ML20/2	ML20/14	Latch Strobe
		AUDIO DUMP			
ML15/4	000F	ML15/4	ML29/7		Audio dump
ML15/3	0000F	ML15/3	ML29/6		Audio dump
BB	P0FA	ML15/1	R193		Audio dump

ALIGNMENT

84 This procedure details the adjustments required for aligning the IF/AF Module.

Test Equipment

85 The following items of test equipment, as detailed in Chapter 2, are required for aligning the IF/AF Module:

(1) Digital Multimeter.
(2) Signal Generator.
(3) RF Millivoltmeter.
(4) 50 ohm Load.
(5) BITE Kit.

Preliminary

86 Remove the IF/AF Module from the receiver and place it on the bench next to the receiver. Remove the top cover from the module to gain access to the preset components (leave the bottom cover fitted). Reconnect the module to the receiver using the extender assembly and coaxial leads provided with the BITE Kit. Adjust the preset components according to the procedure given below.

AGC Distribution Adjustment

87 Set the AGC to manual and adjust the IF gain control for +6V ± 100 mV at TP20 (DIV AGC). Adjust R4 for +5V ± 100 mV at TP4.

AGC Threshold Adjustment

88 Set the AGC to manual and turn the IF gain control fully clockwise for +10V ± 250 mV at TP20 (DIV AGC).

89 Connect the 50 ohm load to PL5 and the signal generator output to PL2, set to 1.4 MHz at a level of -49 dBm (800 µV pd).

90 Adjust R5 for 100mV rms at the IF output (SK1), measured on the RF millivoltmeter set to 50 ohms input impedance.

2nd IF AGC Slope Adjustment

91 Set the AGC to manual and adjust the IF gain control for +8V ± 100 mV at TP20 (DIV AGC).

92 Connect the 50 ohm load to PL5 and the signal generator output to PL2, set to 1.4 MHz at a level of -9 dBm (80 mV pd).

93 Adjust R6 for 100 mV rms at the IF output (SK1), measured on the RF millivoltmeter set to 50 ohms input impedance.

Wideband Filter Adjustment

94 Select the filter bypass (12 kHz bandwidth) and set the AGC to manual. Adjust the IF gain control for + 10V at TP20 (DIV AGC).

95 Connect the 50 ohm load to PL5 and the signal generator to PL2, set to 1.4 MHz at a level of - 49 dBm.

96 Adjust L5 and L6 for peak IF output at SK1, measured on the RF millivoltmeter set to 50 ohms input impedance.

97 Increase the signal generator frequency until the RF voltmeter reading decreases by 2 dB and note the frequency setting of the signal generator. Repeat for a decrease in signal generator frequency from the centre and note the frequency setting.

98 Check that the difference between the two signal generator frequency settings is 25kHz ±5kHz, symmetrical about the 1.4 MHz centre frequency.

99 Repeat the above procedure at the - 30 dB points and check that the frequency difference is 200 kHz ± 5kHz. Tune the signal generator over the bandwidth to check symmetry. Re-adjust R5 and R6 as necessary.

100 If the desired bandwidth is unobtainable by the above method of adjustment, further investigation into a possible fault condition is necessary which may require the use of a tracking generator with spectrum analyser.

PARTS LIST

101 The Racal part number for a complete LA option IF/AF Module is ST86484LA. For information on other options contact Racal Communications Limited.

102 Information on the identification and handling of SMDs is provided in Chapter 2. The parts list for the IF/AF Module is as follows:

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R1		50k	Variable, Linear, Cermet		10	940858G	
R2		3k3	Thick Film Network			939677T	
R3		3k3	Thick Film Network			939677T	
R4		20k	Variable, Linear, Cermet		10	940869U	
R5		500R	Variable, Linear, Cermet		10	940864R	
R6		1k	Variable, Linear, Cermet		10	940865Y	
R7		1k	Thermistor 3825 Disc			943998W	
R8	B2	47k	Thick Film Chip	0.125	2	943910E	473
R9	B2	47k	Thick Film Chip	0.125	2	943910E	473
R10	B5	1k	Thick Film Chip	0.125	2	943890L	102
R11	B0	1k	Thick Film Chip	0.125	2	943890L	102
R12	C1	10k	Thick Film Chip	0.125	2	943902F	103
R13	C1	22k	Thick Film Chip	0.125	2	943906B	223
R14	C7	4k7	Thick Film Chip	0.125	2	943898N	472
R15	C5	4k7	Thick Film Chip	0.125	2	943898N	472
R16	C4	1k	Thick Film Chip	0.125	2	943890L	102
R17	C0	470R	Thick Film Chip	0.125	2	943886I	471
R18	C6	4k7	Thick Film Chip	0.125	2	943898N	472
R19	C2	10k	Thick Film Chip	0.125	2	943902F	103
R20	C1	100R	Thick Film Chip	0.125	2	943878J	101
R21	C1	3k3	Thick Film Chip	0.125	2	943896P	332
R22	C5	10R	Thick Film Chip	0.125	2	943865X	100
R23	C0	3k3	Thick Film Chip	0.125	2	943896P	332
R24	C5	1k	Thick Film Chip	0.125	2	943890L	102
R25	D5	4k7	Thick Film Chip	0.125	2	943898N	472
R26	D0	1k	Thick Film Chip	0.125	2	943890L	102
R27	D5	1k	Thick Film Chip	0.125	2	943890L	102
R28	D5	1k	Thick Film Chip	0.125	2	943890L	102
R29	D8	150R	Thick Film Chip	0.125	2	943880O	151
R30	D6	4k7	Thick Film Chip	0.125	2	943898N	472
R31	D5	4k7	Thick Film Chip	0.125	2	943898N	472
R32	E8	3k3	Thick Film Chip	0.125	2	943896P	332
R33	E8	150R	Thick Film Chip	0.125	2	943880O	151
R34	E0	3k3	Thick Film Chip	0.125	2	943896P	332
R35	E9	10k	Thick Film Chip	0.125	2	943902F	103
R36	E9	150R	Thick Film Chip	0.125	2	943880O	151
R37	E4	1k	Thick Film Chip	0.125	2	943890L	102
R38	E8	120R	Thick Film Chip	0.125	2	943879Q	121
R39	E5	1k	Thick Film Chip	0.125	2	943890L	102
R40	E0	1k	Thick Film Chip	0.125	2	943890L	102
R41	F8	220R	Thick Film Chip	0.125	2	943882M	221
R42	F8	4k7	Thick Film Chip	0.125	2	943898N	472
R43	F6	4k7	Thick Film Chip	0.125	2	943898N	472
R44	F8	4k7	Thick Film Chip	0.125	2	943898N	472
R45	F8	47R	Thick Film Chip	0.125	2	943873W	470
R46	G9	2k2	Thick Film Chip	0.125	2	943894R	222
R47	G1	8k2	Thick Film Chip	0.125	2	943901O	822
R48	G5	1k	Thick Film Chip	0.125	2	943890L	102
R49	G0	1k	Thick Film Chip	0.125	2	943890L	102
R50	G8	220R	Thick Film Chip	0.125	2	943882M	221
R51	G0	4k7	Thick Film Chip	0.125	2	943898N	472
R52	H6	4k7	Thick Film Chip	0.125	2	943898N	472
R53	H8	4k7	Thick Film Chip	0.125	2	943898N	472
R54	H0	1k	Thick Film Chip	0.125	2	943890L	102
R55	H8	1k5	Thick Film Chip	0.125	2	943892J	152
R56	J8	1k	Thick Film Chip	0.125	2	943890L	102
R57	J5	1k	Thick Film Chip	0.125	2	943890L	102
R58	J0	33k	Thick Film Chip	0.125	2	943908Z	333

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R59	J0	27k	Thick Film Chip	0.125	2	943907S	273
R60	J8	27k	Thick Film Chip	0.125	2	943907S	273
R61	J2	2k2	Thick Film Chip	0.125	2	943894R	222
R62	J6	4k7	Thick Film Chip	0.125	2	943898N	472
R63	J4	1k	Thick Film Chip	0.125	2	943890L	102
R64	J2	100k	Thick Film Chip	0.125	2	943914A	104
R65	J2	270k	Thick Film Chip	0.125	2	943919N	274
R66	J1	10k	Thick Film Chip	0.125	2	943902F	103
R67	J1	33k	Thick Film Chip	0.125	2	943908Z	333
R68	J9	56k	Thick Film Chip	0.125	2	943911V	563
R69	K8	22R	Thick Film Chip	0.125	2	943869T	220
R70	K5	33k	Thick Film Chip	0.125	2	943908Z	333
R71	K9	33R	Thick Film Chip	0.125	2	943871Y	330
R72	K9	56k	Thick Film Chip	0.125	2	943911V	563
R73	K7	100k	Thick Film Chip	0.125	2	943914A	104
R74	K7	10k	Thick Film Chip	0.125	2	943902F	103
R75	K6	1k5	Thick Film Chip	0.125	2	943892J	152
R76	K5	15k	Thick Film Chip	0.125	2	943904D	153
R77	K5	22k	Thick Film Chip	0.125	2	943906B	223
R78	K4	39k	Thick Film Chip	0.125	2	943909Q	393
R79	K4	150k	Thick Film Chip	0.125	2	943916I	154
R80	K9	4k7	Thick Film Chip	0.125	2	943898N	472
R81	K3	2k7	Thick Film Chip	0.125	2	943895Y	272
R82	K1	100k	Thick Film Chip	0.125	2	943914A	104
R83	K1	150k	Thick Film Chip	0.125	2	943916I	154
R84	K0	6k8	Thick Film Chip	0.125	2	943900H	682
R85	K0	1k8	Thick Film Chip	0.125	2	943893A	182
R86	K7	10k	Thick Film Chip	0.125	2	943902F	103
R87	L2	10k	Thick Film Chip	0.125	2	943902F	103
R88	L2	68k	Thick Film Chip	0.125	2	943912C	683
R89	L4	5k6	Thick Film Chip	0.125	2	943899E	562
R90	L1	1k5	Thick Film Chip	0.125	2	943892J	152
R91	L1	1k	Thick Film Chip	0.125	2	943890L	102
R92	L1	100k	Thick Film Chip	0.125	2	943914A	104
R93	L0	150k	Thick Film Chip	0.125	2	943916I	154
R94	L0	10k	Thick Film Chip	0.125	2	943902F	103
R95	L5	6k8	Thick Film Chip	0.125	2	943900H	682
R96	L4	330R	Thick Film Chip	0.125	2	943884K	331
R97	L7	220k	Thick Film Chip	0.125	2	943918G	224
R98	L6	22k	Thick Film Chip	0.125	2	943906B	223
R99	L6	4k7	Thick Film Chip	0.125	2	943898N	472
R100	L3	100k	Thick Film Chip	0.125	2	943914A	104
R101	L5	22k	Thick Film Chip	0.125	2	943906B	223
R102	M2	1k2	Thick Film Chip	0.125	2	943891C	122
R103	M1	47k	Thick Film Chip	0.125	2	943910E	473
R104	L7	3k9	Thick Film Chip	0.125	2	943897W	392
R105	M5	220k	Thick Film Chip	0.125	2	943918G	224
R106	M5	47k	Thick Film Chip	0.125	2	943910E	473
R107	M4	3k3	Thick Film Chip	0.125	2	943896P	332
R108	M1	4k7	Thick Film Chip	0.125	2	943898N	472
R109	M0	22k	Thick Film Chip	0.125	2	943906B	223
R110	M0	33k	Thick Film Chip	0.125	2	943908Z	333
R111	M7	4k7	Thick Film Chip	0.125	2	943898N	472
R112	M1	8k2	Thick Film Chip	0.125	2	943901O	822
R113	M3	10k	Thick Film Chip	0.125	2	943902F	103
R114	M3	10k	Thick Film Chip	0.125	2	943902F	103

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R115	M2	4k7	Thick Film Chip	0.125	2	943898N	472
R116	M2	1k8	Thick Film Chip	0.125	2	943893A	182
R117	M6	47k	Thick Film Chip	0.125	2	943910E	473
R118	M6	12k	Thick Film Chip	0.125	2	943903M	123
R119	M5	10k	Thick Film Chip	0.125	2	943902F	103
R120	M2	1M	Thick Film Chip	0.125	2	945100R	105
R121	M1	220k	Thick Film Chip	0.125	2	943918G	224
R122	N4	150k	Thick Film Chip	0.125	2	943916I	154
R123	N4	27k	Thick Film Chip	0.125	2	943907S	273
R124	N3	22k	Thick Film Chip	0.125	2	943906B	223
R125	N8	10k	Thick Film Chip	0.125	2	943902F	103
R126	N8	10k	Thick Film Chip	0.125	2	943902F	103
R127	N8	22R	Thick Film Chip	0.125	2	943869T	220
R128	N7	1k	Thick Film Chip	0.125	2	943890L	102
R129	N4	47k	Thick Film Chip	0.125	2	943910E	473
R130	N2	33k	Thick Film Chip	0.125	2	943908Z	333
R131	N5	10k	Thick Film Chip	0.125	2	943902F	103
R132	N4	10k	Thick Film Chip	0.125	2	943902F	103
R133	N8	5k6	Thick Film Chip	0.125	2	943899E	562
R134	P6	1k	Thick Film Chip	0.125	2	943890L	102
R135	N1	10k	Thick Film Chip	0.125	2	943902F	103
R136	N5	47k	Thick Film Chip	0.125	2	943910E	473
R137	P9	1k	Thick Film Chip	0.125	2	943890L	102
R138	P8	1k	Thick Film Chip	0.125	2	943890L	102
R139	P8	10k	Thick Film Chip	0.125	2	943902F	103
R140	P8	560R	Thick Film Chip	0.125	2	943887Z	561
R141	P5	10k	Thick Film Chip	0.125	2	943902F	103
R142	P5	1k2	Thick Film Chip	0.125	2	943891C	122
R143	P9	1k	Thick Film Chip	0.125	2	943890L	102
R144	P5	100R	Thick Film Chip	0.125	2	943878J	101
R145	P4	10R	Thick Film Chip	0.125	2	943865X	100
R146	P9	22R	Thick Film Chip	0.125	2	943869T	220
R147	R8	39R	Thick Film Chip	0.125	2	943872F	390
R148	R8	1k	Thick Film Chip	0.125	2	943890L	102
R149	R8	5k6	Thick Film Chip	0.125	2	943899E	562
R150	R1	22k	Thick Film Chip	0.125	2	943906B	223
R151	R1	22k	Thick Film Chip	0.125	2	943906B	223
R152	R1	22k	Thick Film Chip	0.125	2	943906B	223
R153	R8	820R	Thick Film Chip	0.125	2	943889X	821
R154	R1	22k	Thick Film Chip	0.125	2	943906B	223
R155	R8	3k3	Thick Film Chip	0.125	2	943896P	332
R156	S1	22k	Thick Film Chip	0.125	2	943906B	223
R157	S1	22k	Thick Film Chip	0.125	2	943906B	223
R158	S9	10k	Thick Film Chip	0.125	2	943902F	103
R159	S9	1k	Thick Film Chip	0.125	2	943890L	102
R160	S8	820R	Thick Film Chip	0.125	2	943889X	821
R161	S8	47R	Thick Film Chip	0.125	2	943873W	470
R162	S1	22k	Thick Film Chip	0.125	2	943906B	223
R163	S1	22k	Thick Film Chip	0.125	2	943906B	223
R164	S8	470R	Thick Film Chip	0.125	2	943886I	471
R165	S8	6k8	Thick Film Chip	0.125	2	943900H	682
R166	S8	3k3	Thick Film Chip	0.125	2	943896P	332
R167	S7	330R	Thick Film Chip	0.125	2	943884K	331
R168	S7	470R	Thick Film Chip	0.125	2	943886I	471
R169	T3	22k	Thick Film Chip	0.125	2	943906B	223
R170	T2	22k	Thick Film Chip	0.125	2	943906B	223

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R171	T9	3k3	Thick Film Chip	0.125	2	943896P	332
R172	T3	22k	Thick Film Chip	0.125	2	943906B	223
R173	T2	22k	Thick Film Chip	0.125	2	943906B	223
R174	T3	22k	Thick Film Chip	0.125	2	943906B	223
R175	T2	22k	Thick Film Chip	0.125	2	943906B	223
R176	T7	56R	Thick Film Chip	0.125	2	943875U	560
R177	T3	22k	Thick Film Chip	0.125	2	943906B	223
R178	T2	22k	Thick Film Chip	0.125	2	943906B	223
R179	T1	33k	Thick Film Chip	0.125	2	943908Z	333
R180	T7	1k	Thick Film Chip	0.125	2	943890L	102
R181	V9	3k3	Thick Film Chip	0.125	2	943896P	332
R182	V8	3k3	Thick Film Chip	0.125	2	943896P	332
R183	V8	390R	Thick Film Chip	0.125	2	943885B	391
R184	V8	3k3	Thick Film Chip	0.125	2	943896P	332
R185	T2	22k	Thick Film Chip	0.125	2	943906B	223
R186	T1	33k	Thick Film Chip	0.125	2	943908Z	333
R187	V3	22k	Thick Film Chip	0.125	2	943906B	223
R188	V2	22k	Thick Film Chip	0.125	2	943906B	223
R189	V1	33k	Thick Film Chip	0.125	2	943908Z	333
R190	V7	470R	Thick Film Chip	0.125	2	943886I	471
R191	V1	33k	Thick Film Chip	0.125	2	943908Z	333
R192	V6	220R	Thick Film Chip	0.125	2	943882M	221
R193	V6	6k8	Thick Film Chip	0.125	2	943900H	682
R194	V2	10k	Thick Film Chip	0.125	2	943902F	103
R195	W9	10R	Thick Film Chip	0.125	2	943865X	100
R196	W7	8k2	Thick Film Chip	0.125	2	943901O	822
R197	W9	390R	Thick Film Chip	0.125	2	943885B	391
R198	W7	4k7	Thick Film Chip	0.125	2	943898N	472
R199	W6	100k	Thick Film Chip	0.125	2	943914A	104
R200	W8	22k	Thick Film Chip	0.125	2	943906B	223
R201	W7	100k	Thick Film Chip	0.125	2	943914A	104
R202	W6	18k	Thick Film Chip	0.125	2	943905K	183
R203	W2	22k	Thick Film Chip	0.125	2	943906B	223
R204	W2	10k	Thick Film Chip	0.125	2	943902F	103
R205	W9	1k2	Thick Film Chip	0.125	2	943891C	122
R206	W6	10k	Thick Film Chip	0.125	2	943902F	103
R207	X7	220k	Thick Film Chip	0.125	2	943918G	224
R208	X6	150k	Thick Film Chip	0.125	2	943916I	154
R209	X6	47k	Thick Film Chip	0.125	2	943910E	473
R210	X5	10k	Thick Film Chip	0.125	2	943902F	103
R211	X2	22k	Thick Film Chip	0.125	2	943906B	223
R212	X8	47k	Thick Film Chip	0.125	2	943910E	473
R213	X7	330k	Thick Film Chip	0.125	2	943920L	334
R214	X5	18k	Thick Film Chip	0.125	2	943905K	183
R215	X5	15k	Thick Film Chip	0.125	2	943904D	153
R216	X5	10k	Thick Film Chip	0.125	2	943902F	103
R217	X4	10k	Thick Film Chip	0.125	2	943902F	103
R218	X4	120k	Thick Film Chip	0.125	2	943915R	124
R219	X4	100k	Thick Film Chip	0.125	2	943914A	104
R220	X4	27k	Thick Film Chip	0.125	2	943907S	273
R221	Y9	3k3	Thick Film Chip	0.125	2	943896P	332
R222	X8	100k	Thick Film Chip	0.125	2	943914A	104
R223	Y8	82k	Thick Film Chip	0.125	2	943913T	823
R224	Y4	1k5	Thick Film Chip	0.125	2	943892J	152
R225	Y3	1k5	Thick Film Chip	0.125	2	943892J	152
R226	Y8	8k2	Thick Film Chip	0.125	2	943901O	822
R227	Y2	330k	Thick Film Chip	0.125	2	943920L	334

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R228	Y2	33k	Thick Film Chip	0.125	2	943908Z	333
R229	Y2	33k	Thick Film Chip	0.125	2	943908Z	333
R230	Y5	47k	Thick Film Chip	0.125	2	943910E	473
R231	Y4	1k5	Thick Film Chip	0.125	2	943892J	152
R232	Y4	10k	Thick Film Chip	0.125	2	943902F	103
R233	Y4	6k8	Thick Film Chip	0.125	2	943900H	682
R234	Y3	150R	Thick Film Chip	0.125	2	943880O	151
R235	Y8	8k2	Thick Film Chip	0.125	2	943901O	822
R236	Y8	4k7	Thick Film Chip	0.125	2	943898N	472
R237	Y2	100k	Thick Film Chip	0.125	2	943914A	104
R238	Y2	33k	Thick Film Chip	0.125	2	943908Z	333
R239	Y2	10k	Thick Film Chip	0.125	2	943902F	103
R240	Y5	1k	Thick Film Chip	0.125	2	943890L	102
R241	Y4	8k2	Thick Film Chip	0.125	2	943901O	822
R242	Y9	10k	Thick Film Chip	0.125	2	943902F	103
R243	Z8	100k	Thick Film Chip	0.125	2	943914A	104
R244	Z6	100k	Thick Film Chip	0.125	2	943914A	104
R245	Z6	47k	Thick Film Chip	0.125	2	943910E	473
R246	Y5	47k	Thick Film Chip	0.125	2	943910E	473
R247	Z7	220k	Thick Film Chip	0.125	2	943918G	224
R248	Z3	100k	Thick Film Chip	0.125	2	943914A	104
R249	Z9	2k2	Thick Film Chip	0.125	2	943894R	222
R250	Z5	1k	Thick Film Chip	0.125	2	943890L	102
R251	Z2	10k	Thick Film Chip	0.125	2	943902F	103
R252	Z2	100k	Thick Film Chip	0.125	2	943914A	104
R253	Z5	47k	Thick Film Chip	0.125	2	943910E	473
R254	Z5	1k	Thick Film Chip	0.125	2	943890L	102
R255	Z8	10R	Thick Film Chip	0.125	2	943865X	100
R256	Z2	56k	Thick Film Chip	0.125	2	943911V	563
R257	Z2	330k	Thick Film Chip	0.125	2	943920L	334
R258	Z6	680R	Thick Film Chip	0.125	2	943888G	681
R259	Z5	10k	Thick Film Chip	0.125	2	943902F	103
R260	Z9	1k	Thick Film Chip	0.125	2	943890L	102
R261	Z5	100k	Thick Film Chip	0.125	2	943914A	104
R262	Z4	10R	Thick Film Chip	0.125	2	943865X	100
R263	J3	100k	Thick Film Chip	0.125	2	943914A	104
R264	J6	100k	Thick Film Chip	0.125	2	943914A	104
R265	J6	100k	Thick Film Chip	0.125	2	943914A	104
Capacitors				V			
C1		470µ	Electrolytic	40	-10 +50	941812L	
C2		470µ	Electrolytic	40	-10 +50	941812L	
C3	B7	10n	Ceramic Chip	50	10	941775D	
C4	B2	10n	Ceramic Chip	50	10	941775D	
C5	B1	10n	Ceramic Chip	50	10	941775D	
C6	B7	47p	Ceramic Chip	50	5	941795H	
C7	B6	10n	Ceramic Chip	50	10	941775D	
C8	C8	68p	Ceramic Chip	50	5	941797F	
C9	B7	10n	Ceramic Chip	50	10	941775D	
C10	B5	10n	Ceramic Chip	50	10	941775D	
C11	C2	10n	Ceramic Chip	50	10	941775D	
C12	C0	100n	Ceramic Chip	50	20	945146T	

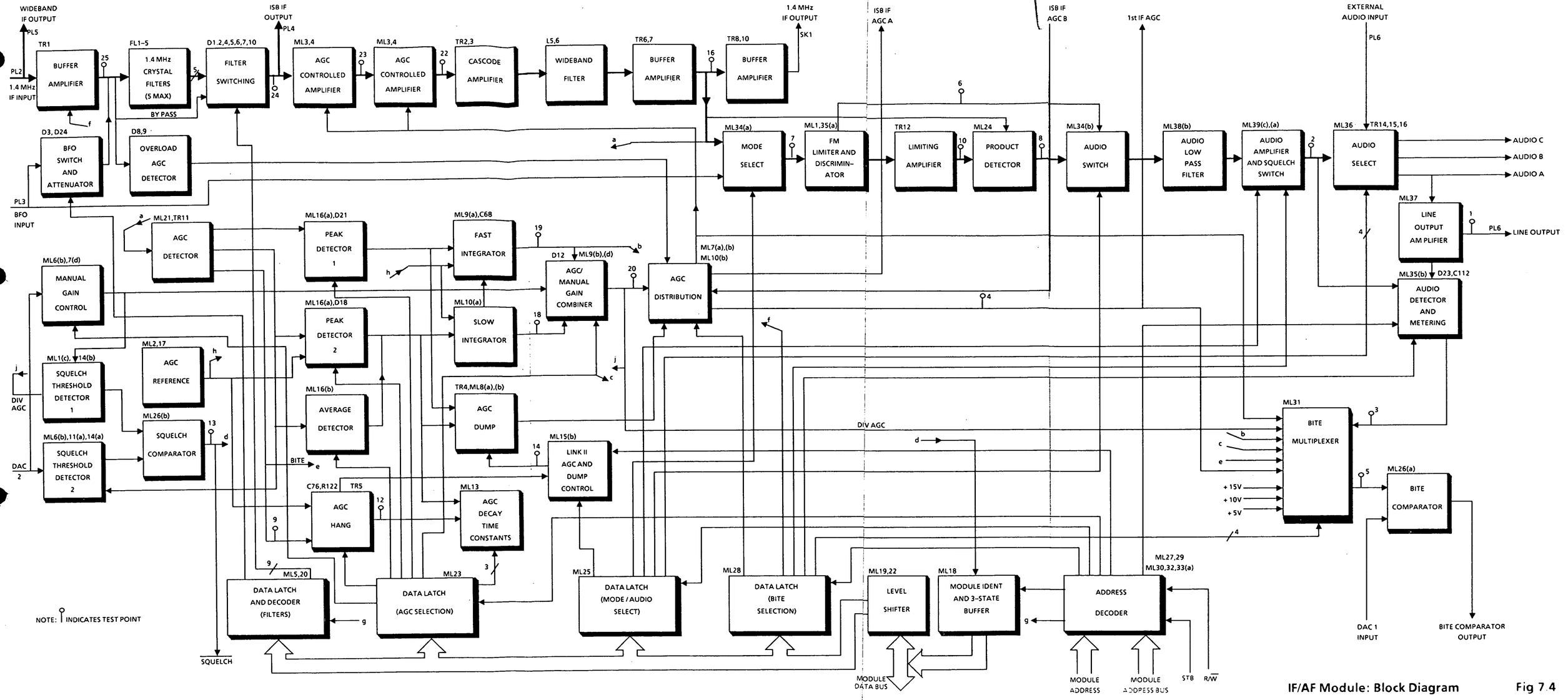
Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C13	C7	10n	Ceramic Chip	50	10	941775D	
C14	C5	10n	Ceramic Chip	50	10	941775D	
C15	C1	100n	Ceramic Chip	50	20	945146T	
C16	C0	10n	Ceramic Chip	50	10	941775D	
C17	D5	10n	Ceramic Chip	50	10	941775D	
C18	D5	10n	Ceramic Chip	50	10	941775D	
C19	D1	68p	Ceramic Chip	50	5	941797F	
C20	D7	47p	Ceramic Chip	50	5	941795H	
C21	D6	10n	Ceramic Chip	50	10	941775D	
C22	D7	10n	Ceramic Chip	50	10	941775D	
C23	E9	100n	Ceramic Chip	50	20	945146T	
C24	D8	10n	Ceramic Chip	50	10	941775D	
C25	E4	10n	Ceramic Chip	50	10	941775D	
C26	E5	10n	Ceramic Chip	50	10	941775D	
C27	E9	10n	Ceramic Chip	50	10	941775D	
C28	E9	10n	Ceramic Chip	50	10	941775D	
C29	E8	10n	Ceramic Chip	50	10	941775D	
C30	E7	47p	Ceramic Chip	50	5	941795H	
C31	E6	10n	Ceramic Chip	50	10	941775D	
C32	E1	68p	Ceramic Chip	50	5	941797F	
C33	F8	100n	Ceramic Chip	50	20	945146T	
C34	F7	10n	Ceramic Chip	50	10	941775D	
C35	F9	1µ	Tantalum Chip	35	20	945049Z	
C36	F6	1µ	Tantalum Chip	35	20	945049Z	
C37	F8	10n	Ceramic Chip	50	10	941775D	
C38	F9	100n	Ceramic Chip	50	20	945146T	
C39	G9	10n	Ceramic Chip	50	10	941775D	
C40	G7	47p	Ceramic Chip	50	5	941795H	
C41	G6	10n	Ceramic Chip	50	10	941775D	
C42	G1	68p	Ceramic Chip	50	5	941797F	
C43	G7	10n	Ceramic Chip	50	10	941775D	
C44	G8	10n	Ceramic Chip	50	10	941775D	
C45	G1	10n	Ceramic Chip	50	10	941775D	
C46	H8	4µ7	Tantalum Chip	35	20	945051E	
C47	H6	100n	Ceramic Chip	50	20	945146T	
C48	H1	68p	Ceramic Chip	50	5	941797F	
C49	H9	10n	Ceramic Chip	50	10	941775D	
C50	J7	47p	Ceramic Chip	50	5	941795H	
C51	J6	10n	Ceramic Chip	50	10	941775D	
C52	J0	10n	Ceramic Chip	50	10	941775D	
C53	J7	10n	Ceramic Chip	50	10	941775D	
C54	J1	100n	Ceramic Chip	50	20	945146T	
C55	J9	10n	Ceramic Chip	50	10	941775D	
C56	K4	10n	Ceramic Chip	50	10	941775D	
C57	J2	100n	Ceramic Chip	50	20	945146T	
C58	J8	2p2	Ceramic Chip	50	0.25	941781E	
C59	J6	10n	Ceramic Chip	50	10	941775D	
C60	J6	10n	Ceramic Chip	50	10	941775D	
C61	K9	10n	Ceramic Chip	50	10	941775D	
C62	K4	10n	Ceramic Chip	50	10	941775D	
C63	K2	10n	Ceramic Chip	50	10	941775D	
C64	K1	10n	Ceramic Chip	50	10	941775D	
C65	L5	3µ3	Tantalum Chip	16	20	945050N	
C66	L8	1n5	Ceramic Chip	50	5	945148B	
C67	L8	100n	Ceramic Chip	50	20	945146T	
C68	L6	100n	Ceramic Chip	50	20	945146T	
C69	L3	100n	Ceramic Chip	50	20	945146T	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C70	L8	22p	Ceramic Chip	50	5	941791L	
C71	M3	100n	Ceramic Chip	50	20	945146T	
C72	L1	10n	Ceramic Chip	50	10	941775D	
C73	M8	1n5	Ceramic Chip	50	5	945148B	
C74	M0	100n	Ceramic Chip	50	20	945146T	
C75	M8	10n	Ceramic Chip	50	10	941775D	
C76	N4	10µ	Tantalum Chip	35	20	945053C	
C77	N2	100n	Ceramic Chip	50	20	945146T	
C78	N2	100n	Ceramic Chip	50	20	945146T	
C79	N9	4µ7	Tantalum Chip	35	20	945051E	
C80	N0	100n	Ceramic Chip	50	20	945146T	
C81	N8	10n	Ceramic Chip	50	10	941775D	
C82	N1	10n	Ceramic Chip	50	10	941775D	
C83	P5	100n	Ceramic Chip	50	20	945146T	
C84	P4	100n	Ceramic Chip	50	20	945146T	
C85	P9	100n	Ceramic Chip	50	20	945146T	
C86	P8	100n	Ceramic Chip	50	20	945146T	
C87	P5	10n	Ceramic Chip	50	10	941775D	
C88	R2	10n	Ceramic Chip	50	10	941775D	
C89	S7	10n	Ceramic Chip	50	10	941775D	
C90	S9	10n	Ceramic Chip	50	10	941775D	
C91	S8	100n	Ceramic Chip	50	20	945146T	
C92	S9	10n	Ceramic Chip	50	10	941775D	
C93	S9	10n	Ceramic Chip	50	10	941775D	
C94	T7	10n	Ceramic Chip	50	10	941775D	
C95	T7	10n	Ceramic Chip	50	10	941775D	
C96	T7	100n	Ceramic Chip	50	20	945146T	
C97	T8	100n	Ceramic Chip	50	20	945146T	
C98	T7	100n	Ceramic Chip	50	20	945146T	
C99	V9	10n	Ceramic Chip	50	10	941775D	
C100	V9	100n	Ceramic Chip	50	20	945146T	
C101	V8	4µ7	Tantalum Chip	35	20	945051E	
C102	V6	1n5	Ceramic Chip	50	5	945148B	
C103	V6	1µ0	Tantalum Chip	35	20	945049Z	
C104	W8	1µ0	Tantalum Chip	35	20	945049Z	
C105	W9	10n	Ceramic Chip	50	10	941775D	
C106	W8	100n	Ceramic Chip	50	20	945146T	
C107	W8	100n	Ceramic Chip	50	20	945146T	
C108	W7	1n	Ceramic Chip	50	10	941772O	
C109	W7	6µ8	Tantalum Chip	16	20	945147K	
C110	X9	6µ8	Tantalum Chip	16	20	945147K	
C111	X7	100n	Ceramic Chip	50	20	945146T	
C112	X6	1µ0	Tantalum Chip	35	20	945049Z	
C113	X8	10n	Ceramic Chip	50	10	941775D	
C114	X1	10n	Ceramic Chip	50	10	941775D	
C115	Y9	100n	Ceramic Chip	50	20	945146T	
C116	Y1	100n	Ceramic Chip	50	20	945146T	
C117	Y1	100n	Ceramic Chip	50	20	945146T	
C118	Y0	100n	Ceramic Chip	50	20	945146T	
C119	Y7	1n5	Ceramic Chip	50	5	945148B	
C120	Y7	2n7	Ceramic Chip	50	10	945149I	
C121	Y1	100n	Ceramic Chip	50	20	945146T	
C122	Y1	100n	Ceramic Chip	50	20	945146T	
C123	Y0	100n	Ceramic Chip	50	20	945146T	
C124	Z8	100n	Ceramic Chip	50	20	945146T	
C125	Z1	33µ	Tantalum Chip	10	20	945054T	
C126	Z1	10µ	Tantalum Chip	35	10	945053C	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C127	Z0	10µ	Tantalum Chip	35	10	945053C	
C128	Z6	4µ7	Tantalum Chip	35	20	945051E	
C129	Z4	10µ	Tantalum Chip	35	10	945053C	
C130	Z8	100n	Ceramic Chip	50	20	945146T	
C131	Z9	100n	Ceramic Chip	50	20	945146T	
Inductors				W			
L1		3µH3	Choke	0.2	10	940025C	
L2		1µH0	Choke	0.2	10	938966Z	
L3		3µH3	Choke	0.2	10	940025C	
L4		-	Choke, variable			945099O	
L5		-	Coil Assembly			ST87451	
L6		-	Coil Assembly			ST87451	
L7		15µ0H	Choke		10	945098X	
Transformers							
T1			Transformer Assembly			ST87452	
Diodes							
D1	C6		BAW 52			943952U	
D2	C6		BAS 16			943951D	
D3	D2		BAS 16			943951D	
D4	D6		BAW 56			943952U	
D5	E5		BAW 56			943952U	
D6	F6		BAW 56			943952U	
D7	G6		BAW 56			943952U	
D8	G1		BAW 56			943952U	
D9	H1		BAS 16			943951D	
D10	J6		BAW 56			943952U	
D11	K3		BAS 16			943951D	
D12	K6		BAW 56			943952U	
D13	L2		BAS 16			943951D	
D14	L7		BAS 16			943951D	
D15	M7		BZX84-C, 2V7 Zener			945101Y	
D16	M2		BZX84-C, 3V3 Zener			945103W	
D17	M1		BAS 16			943951D	
D18	M6		BAS 16			943951D	
D19	N5		BAS 16			943951D	
D20	N0		BAW 56			943952U	
D21	N6		BAS 16			943951D	
D22	W5		BAS 16			943951D	
D23	X7		BAS 16			943951D	
D24	Z9		BAS 16			943951D	
Transistors							
TR1	C1		BC 849 NPN			943941W	
TR2	J8		BC 849 NPN			943941W	
TR3	K8		BC 849 NPN			943941W	
TR4	L5		BC 849 NPN			943941W	
TR5	N3		BC 849 NPN			943941W	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Transistors							
TR6	N8		BC 849 NPN			943941W	
TR7	N8		BC 849 NPN			943941W	
TR8	P8		BC 849 NPN			943941W	
TR9	P4		BC 849 NPN			943941W	
TR10	P8		BC 849 NPN			943941W	
TR11	S8		BC 859 PNP			943942N	
TR12	T6		BC 849 NPN			943941W	
TR13	V6		BC 849 NPN			943941W	
TR14	Y5		BC 849 NPN			943941W	
TR15	Y5		BC 849 NPN			943941W	
TR16	Z5		BC 849 NPN			943941W	
Integrated Circuits		CAUTION: *SSD - STATIC SENSITIVE DEVICES					
ML1			3189,FM IF System			938977N	
ML2			01, +10V Reference			945020M	
ML3	E8		3046, Transistor Array			945025P	
ML4	G8		3046, Transistor Array			945025P	
ML5	H4	*SSD	4028, BCD to Decimal Decoder			943992C	
ML6	J0	*SSD	5260, Dual Operational Amplifier			945450H	
ML7	K4		324, Quad Operational Amplifier			945026G	
ML8	K2	*SSD	4066, Quad Bilaterial Switch			945043V	
ML9	L6		324, Quad Operational Amplifier			945026G	
ML10	L4	*SSD	5260, Dual Operational Amplifier			945450H	
ML11	L0		339, Quad Voltage Comparator			945023R	
ML12	M6	*SSD	4066, Quad Bilateral Switch			945043V	
ML13	M4	*SSD	4066, Quad Bilateral Switch			945043V	
ML14	M2		1458, Dual Operational Amplifier			945022K	
ML15	N1	*SSD	4013, Dual D-Type Flip-Flop			943991L	
ML16	N6		324, Quad Operational Amplifier			945026G	
ML17	N4		324, Quad Operational Amplifier			945026G	
ML18	P2	*SSD	74HC244, Octal Line Driver			943987I	
ML19	R3	*SSD	40109, Quad Level Shifter			945045D	
ML20	R4	*SSD	4508, Dual 4-Bit Latch			945046K	
ML21	S9		3046, Transistor Array			945025P	
ML22	S3	*SSD	40109, Quad Level Shifter			945045D	
ML23	S4	*SSD	4508, Dual 4-Bit Latch			945046K	
ML24	T8		1496, Balanced Modulator/Demodulator			945027X	
ML25	T4	*SSD	4508, Dual 4-Bit Latch			945046K	
ML26	V1		339, Quad Voltage Comparator			945023R	
ML27	V2	*SSD	74HC85, 4-Bit Magnitude Comparator			943978S	
ML28	V4	*SSD	4508, Dual 4-Bit Latch			945046K	
ML29	W2	*SSD	4028, BCD to Decimal Decoder			943992C	
ML30	W1	*SSD	40109, Quad Level Shifter			945045D	
ML31	X4	*SSD	4067, 16-Channel Multiplexer			945044M	
ML32	X3	*SSD	74HC00, Quad 2-Input NAND Gate			943968V	
ML33	X1	*SSD	74HC00, Quad 2-Input NAND Gate			943968V	
ML34	X8	*SSD	4053, Triple 2-Channel Multiplexer			945041X	
ML35	Y7		1458 , Dual Operational Amplifier			945022K	
ML36	Y6	*SSD	4066, Quad Bilateral Switch			945043V	
ML37	Z3		1458, Dual Operational Amplifier			945022K	
ML38	Z8		1458, Dual Operational Amplifier			945022K	
ML39	Z7	*SSD	4066, Quad Bilateral Switch			945043V	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Connectors							
PL1			Plug, 64-Way			940339G	
PL6			Plug, 15-Way			945165Q	
Filters							
FL1			1.4 MHz Filter, 6 kHz Sym.			BD86660	
FL2			1.4 MHz Filter, 1 kHz Sym.			BD86661	
FL3			1.4 MHz Filter, 300 Hz Sym.			BD86662	
FL4			1.4 MHz Filter, 2.7 kHz LSB			BD86658	
FL5			1.4 MHz Filter, 2.7 kHz USB			BD86659	
Miscellaneous							
W1			Cable Assembly			BA87136	
W2			Cable Assembly			BA87136	
W3			Cable Assembly			BA87136	
W4			Cable Assembly			BA87136	
W5			Cable Assembly			BA87135	
TP1 to TP25			Terminal, Assembly (test points)			936148X	



IF/AF Module: Block Diagram

Fig 7.4

CHAPTER 8

FIRST LO SYNTHESISER MODULE

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TABLE

ILLUSTRATIONS

CHAPTER 8

FIRST LO SYNTHESISER MODULE

INTRODUCTION

1 The lst LO Synthesiser Module provides the first local oscillator signal in the range 41.4 to 71.4 MHz for injection into the 1st mixer in the Front End Module. The synthesiser is based on a phase-locked loop (PLL) locked to a 20 MHz reference produced by the Reference/BFO Module.

Fig. 8.1 Receiver Block Diagram

Basic Synthesiser Operation

2 The basic frequency synthesiser is shown in Fig. 8.2. The output of the voltage controlled oscillator (VCO) is divided by 'N' and compared in a phase comparator with a reference signal. The phase comparator output is filtered and used to control the VCO frequency. Phase lock is achieved when the divided VCO frequency and reference signal are equal in frequency and phase.

3 Use is made of an LSI device containing synthesiser control circuitry. This controls the division ratio of the divide by 'N' stage in a way that allows fractional division ratios to be obtained. Consequently, tuning resolution down to 1 Hz steps is achieved using a single phase- locked loop. The synthesiser control device is programmed with frequency setting data sent by the Processor via the module data bus.

Fig. 8.2 Basic Frequency Synthesiser

MODULE DESCRIPTION

4 The following description should be read in conjunction with the 1st LO Synthesiser Block and Circuit Diagrams included with this chapter. Component references shown on the Block Diagram allow it to be related to the Circuit Diagram.

Voltage Controlled Oscillator

5 The 1st LO output frequency is derived from a VCO comprising a switched range oscillator.

6 A VCO RANGE SWITCHING circuit allows the VCO to be operated in eight switched ranges using three fixed capacitors as shown in Table 8.1. The capacitors are switched into circuit in a binary sequence by means of transistor switches controlled by the Processor via the module data bus.

TABLE 8.1

VCO Range Switching

Range	Receiver Freq. (MHz)	Components Switched In	
7	0.000000 to 1.800000	C45,C50,C51	R68,R74
6	1.800001 to 3.600000	C50,C51	R68,R74
5	3.600001 to 6.800000	C45,C51	R68
4	6.800001 to 9.400000	C51	R68
3	9.400001 to 12.700000	C45,C50	R74,R75
2	12.700001 to 16.300000	C50	R74
1	16.300001 to 23.700000	C45	R75
0	23.700001 to 30.000000	NONE	NONE

7 A DC control voltage is applied to varactor diodes connected to the VCO tuned circuit. An increase in the varactor voltage causes a decrease in varactor capacitance and hence an increase in oscillator frequency, and vice versa.

AGC Circuit

8 An AGC CIRCUIT maintains the VCO output constant over the frequency range by setting the VCO bias current in response to variations in the VCO output. The circuit detects an increase in VCO output to provide a corresponding decrease in bias current to reduce the gain, and vice-versa.

1st LO Output

9 The output of the VCO is buffered to a CASCODE OUTPUT AMPLIFIER which provides the required drive level at the correct impedance for the 1st LO output.

10 In addition, the VCO signal is fed back to the phase-locked loop via an ISOLATION BUFFER. The resulting signal is then passed through an ECL PULSE SHAPER AND BUFFER to provide a suitable clock for driving the PROGRAMMABLE DIVIDER.

Programmable Dividers

11 In the PROGRAMMABLE DIVIDER, the oscillator frequency is first divided by a dual modulus prescaler, ML2. The prescaler divides by either 5 or 6 depending on the logic level at the output of ML9(a).

12 Counters ML10 and ML11 are loaded with a preset number by the SYNTHESISER CONTROL device and then start counting down. The prescaler, ML2, is set to divide-by-6 using gate ML9(a). The output of this gate is at logic low whilst counting is in progress because at least one of the counter Q outputs will be at logic high.

13 When the ML11 count sequence reaches number 1, the output of gate ML9(a) goes high, setting the prescaler to divide-by-5 and inhibiting ML11 from counting down any further. Counter ML10 continues counting down until it reaches zero at which point a carry out pulse reloads the counters and the sequence is repeated. A timing diagram for a divide-by- 43 sequence is shown in Fig. 8.3.

14 Before application to the PHASE COMPARATOR for comparison with the 1 MHz reference signal on the other input, the carry out pulse is synchronised to the counters clock by the DIVIDER RECLOCKING latch.

Synthesiser Control

15 The SYNTHESISER CONTROL device, ML14, allows the VCO output frequency to be incrementally adjusted in steps which are much less in size than the 1 MHz reference frequency. Computation circuitry within this device processes frequency setting data loaded in from the Processor data bus to control the division ratio of the PROGRAMMABLE DIVIDER. The actual division ratio is constantly varied between integer values for brief periods of time to give the required non-integer division ratio necessary for fractional division of the feedback signal, thus achieving the required synthesiser resolution.

16 For a frequency resolution down to 1 Hz steps, the SYNTHESISER CONTROL is supplemented by a CLOCK DIVIDER FOR 1 HZ STEPS circuit consisting of a BCD rate divider controlled by processed data from ML14. Data to this device is sent in a binary sequence. For a 1 Hz step, input A of ML13 is high and for a 7 Hz step, inputs A, B and C are high.

17 Spurious sidebands produced by the action of varying the division ratio are reduced at the PHASE COMPARATOR output by the application of an analogue signal. This compensating signal is derived by analogue to digital conversion of data provided by the SYNTHESISER CONTROL device.

Reference Input

18 The 20 MHz reference input is applied to a DIVIDE-BY-4 stage and the resulting 5 MHz output is converted to 9 V CMOS levels by a LEVEL SHIFTER before application to the SYNTHESISER CONTROL device, ML14. This clocks ML14 and produces the required 1 MHz reference for the PHASE COMPARATOR after synchronising it with the 5 MHz signal in the REFERENCE RECLOCKING circuit.

Phase Comparator and Loop Integrator

19 The PHASE COMPARATOR produces output pulses of length proportional to the phase difference between the reference and divided feedback inputs. When the Q outputs of both D-type latches in the PHASE COMPARATOR are high, the reset output (TP8) of the flip-flop formed by ML15(a) to (c) goes low. This clears both latches to determine the width of the PHASE COMPARATOR output pulses and causes the Q outputs of both D-type latches to go high again. These outputs cause the reset output of ML15 to go high, ready for the next cycle.

20 The timing relationship between the PHASE COMPARATOR inputs and outputs is shown in Fig. 8.4. Waveforms are given for the in-lock condition and the out-of-lock condition, when the VCO frequency can be either too high or too low.

21 The output pulses are applied to a CURRENT PUMP consisting of switching transistors; this produces a mean current output which varies linearly with the phase difference between the two input signals. The circuit action is as follows.

22 Considering first the in-lock condition and referring to the circuit diagram it can be seen that 150ns pulses are produced at the base of TR17. For each pulse, TR17 switches on and a current I flows out of the integrator (ML1) i.e. I is negative. During the remainder of the cycle the current I into the integrator is such that the average current over the whole 1 µs period is zero and the LOOP INTEGRATOR output voltage remains constant. Under these conditions the short pulses from ML12 pin 5 are insufficent to switch TR18 on and therefore TR16 is switched off.

23 For VCO frequencies too high the wider pulses now produced at the base of TR18 switch it and TR16 on. Current is pumped into the integrator and the average current over the whole cycle is positive. The output of the integrator ramps down reducing the VCO varactor voltage, and hence the VCO frequency, until phase lock occurs.

24 For VCO frequencies too low, pulses longer than 150 ns are now produced at the base of TR17, switching it on for a longer time than the in-lock condition. This causes more current to flow out of the integrator and the average current over the whole cycle is now negative. The output of the integrator ramps up, increasing the VCO varactor voltage and hence the VCO frequency until phase lock occurs.

25 To compensate for variations in loop gain over the VCO frequency range caused by the change in division ratio, a PULSE WIDTH TO VOLTAGE CONVERTER circuit is included. In this circuit, Schottky diodes D13 and D14 detect the PROGRAMMABLE DIVIDER output pulses for integration by ML7(b) into a voltage which increases with an increase in division ratio. This voltage is then used in the CURRENT PUMP to vary the PHASE COMPARATOR gain in proportion to the VCO frequency.

Loop Amplifier and Loop Filter

26 The LOOP INTEGRATOR output voltage is applied to a LOOP AMPLIFIER AND LINEARISATION circuit. The amplifier gain is adjusted in two ways to compensate for the variation in VCO tuning sensitivity with frequency. Firstly, three resistors are switched into circuit depending on the chosen VCO range, as shown in Table 8.1. Secondly, the amplifier gain is altered when its output voltage exceeds 12.5 V, causing D10 to become forward biased. Both these linearisation methods keep the loop gain constant over each switched VCO range and also over the entire VCO frequency coverage.

27 After amplification and linearisation, the voltage is then filtered in the LOOP FILTER and applied as the control voltage to the VCO varactor diodes.

Fast Lock Detector

28 The phase lock loop is brought into lock more quickly following a frequency change by the action of a FAST LOCK DETECTOR. This consists of a limit comparator which senses an out-of-lock varactor voltage resulting from an abrupt change in frequency in either direction. The FAST LOCK DETECTOR activates quad transmission gate ML8. Three of the now closed sections of this gate are used to modify the LOOP INTEGRATOR and LOOP FILTER by widening the loop bandwidth, and also bring the FAST LOCK DRIVER into operation to force a rapid return to the phase locked condition.

Bus Interface

29 A unique hardwired code is received on the Module Address input to the 1st LO Synthesiser Module via the motherboard. This code is used by the ADDRESS DECODER to detect addresses on the Module Address Bus from the Processor Module and then produce read or write pulses according to the status of the R/W input. These pulses allow the Processor to read data from the 3-STATE BUFFER or write data to the DATA LATCHES, using the Module Data Bus. Pulses on the strobe input ensure correct timing of write pulses. The 3-STATE BUFFER gives the Processor access to the module identification code. The DATA LATCH outputs are used to control the various functions throughout the module and enable the 3-STATE BUFFER to transfer frequency setting data to the SYNTHESISER CONTROL.

BITE Measurement System

30 The BITE measurement system, comprising a BITE MULTIPLEXER operating in conjunction with a BITE COMPARATOR, allows the Processor to measure various voltages and operating levels in the 1st LO Synthesiser Module. The voltage to be measured is selected by the BITE MULTIPLEXER and compared in the BITE COMPARATOR with a voltage generated by a digital to analogue converter (DAC) in the Processor Module. The Processor measures the level of the selected voltage by applying voltages representing upper and lower limits to the comparator and then monitoring the resulting output.

FAULT FINDING

General

31 Fault finding techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the 1st LO Synthesiser Module is contained in the following sections.

BITE Tests

32 The following BITE tests for the 1st LO Synthesiser Module are arranged in the order in which they are performed or presented for selection.

TEST NUMBER : 251

TITLE : BITE hardware

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : DAC 1 line is set to 2.55 volts (i.e. max). BITE multiplexer input X1 (+5.2 volts) is selected and the output of the BITE comparator is checked to ensure that it is low.

LIMITS : Less than 0.8 V at TP3.

FAULT DIRECTORY : Fault No. 2

TEST NUMBER : 252, 253, 254, 255, 256

TITLE : +5.2V rail, +15V rail, +24V rail, +9V rail, -15V rail.

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : The appropriate BITE multiplexer input is selected and the supply voltage is checked.

LIMITS :

Test No.	Supply	Mux. Input	Mux. Limits (TP3)	
			Lower	Upper
252	+5.2 V	X2	1.83 V	2.33 V
253	+ 15 V	X3	1.70 V	2.21 V
254	+24 V	X4	1.73 V	2.45 V
255	+ 9 V	X5	1.90 V	2.36 V
256	-15 V	X6	1.65 V	2.24 V

FAULT DIRECTORY : Fault No. 4

TEST NUMBER : 257

TITLE : Synth. varactor

PERFORMED : Continuous.

DESCRIPTION : BITE multiplexer input X10 is selected. The varactor voltage is measured at the operating frequency.

LIMITS :

Mux. Input		Varactor Line	
Lower	Upper	Lower	Upper
0.4V	2.25V	3.7V	20.7V

FAULT DIRECTORY : Fault No. 5

TEST NUMBER : 258

TITLE : Synth. range

PERFORMED : Unit confidence test, select test.

DESCRIPTION : BITE multiplexer input X10 is selected and the varactor voltage is checked on each synthesiser range. Measurements are made at 10 kHz above and below each range change point.

LIMITS : Less than 1.3V on TP3 at 10 kHz above range change point.
Greater than 1.4V on TP3 at 10 kHz below range change point.

FAULT DIRECTORY : Fault No. 6

TEST NUMBER	:	259
TITLE	:	Synth. sweep.
PERFORMED	:	Unit confidence test, select test.
DESCRIPTION	:	BITE multiplexer input X10 is selected. The synthesiser frequency is swept from zero to 1.8MHz in 100 kHz steps and the varactor line is measured at each step to check that the voltage monotonically increases.
LIMITS	:	Greater than a 10 mV increase on TP3 for every 100 kHz step.
FAULT DIRECTORY	:	Fault No. 7

TEST NUMBER	:	260
TITLE	:	Synth. o/p level.
PERFORMED	:	Unit confidence test, select test.
DESCRIPTION	:	BITE multiplexer input X9 is selected and the detected synthesiser output level is measured at receiver frequencies of 0 MHz, 10 MHz, 20 MHz and 30 MHz.
LIMITS	:	

Mux. Level		Output Level	
Lower	Upper	Lower	Upper
1V	—	+12 dBm	—

FAULT DIRECTORY	:	Fault No. 8

Fault Directory

33 Use the following fault directory to identify the fault condition and take the necessary corrective action. Note that all inputs to the module are assumed to be correct.

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
1	Fails to run BITE tests for 1st LO Synth Module.	Address decoding/module ident, not responding	Check address decoding/module ident logic operation using signature analysis routine if necessary.
2	BITE hardware fault	Comparator/multiplexer inoperative	Use BITE test 251 to check comparator operation. Select all BITE tests for this module to check multiplexer operation for all analogue inputs. Use signature analysis routine to check multiplexer addressing.
3	BITE indicates failure but manual check shows no fault.	(a) BITE hardware fault. (b) Faulty BITE detector	(a) As above. (b) Check operation of suspect BITE dectector.
4	Power supply fault within module.	(a) Faulty component drawing excess current or open circuit choke L1 to L4. (b) Supply regulator faulty.	(a) Locate and replace faulty component. (b) Check voltage levels around suspect regulator.
5	Synthesiser frequency incorrect.	No 1MHz reference to PLL or PLL out of lock.	Follow synthesiser loop check procedure.
6	Synthesiser frequency incorrect on one or some ranges.	Range or VCO switching fault.	Check action of VCO or loop amplifier range switching components.
7	Synthesiser frequency incorrect for part of a range.	VCO linearisation or range switching fault.	Check operation of dividers, pulse width to voltage converter and VCO linearisation.
8	Synthesiser level (PL2) low or varies with frequency.	VCO or output stage fault,	Check signal levels around these circuits.
9	Synthesiser responds slowly to sudden tuning changes.	Fast lock circuit not functioning.	Check circuit levels.

Synthesiser Loop Check Procedure

1 MHz reference for phase comparator

34 Check the reference input to the phase comparator at TP10 and ensure that the frequency is 1 MHz. If incorrect, check that a divided 20 MHz reference signal of 5 MHz is present at TP5. If the signal is present at the clock input of the synthesiser control device and not at its clock output, first check the supplies on pins 42 and 43 of the device before suspecting it as being faulty.

VCO

35 Ensure that the VCO oscillates and that the drive level to the programmable divider at TP15 is adequate (i.e. ECL levels). The tuning of the VCO may be checked by connecting a variable DC power supply between the R83 side LK1 (remove link first) and 0V. Connect a frequency counter to SK1 and tune the receiver frequency to each frequency range in Table 8.1. As the tuning voltage is varied over the range 5 V to 20 V it should be possible to tune the VCO over the frequencies shown in Table 8.1.

Programmable divider

36 An indication that the programmable divider is functioning in basic terms may be obtained by checking that a waveform is present at the output of the divider re-clocking stage (TP11). If absent, check that the clock input is present on TP15 and is divided by the prescaler, producing a lower frequency at ML2 pin 7. The division ratio of the prescaler is continuously being changed by the output of gate ML9(a). If this output is always high or low, check that the presettable binary counters are being loaded with preset data from ML14 by a negative-going pulse on the carry out (ML10 pin 15).

37 The preset data may be checked by setting the receiver to 1.6MHz (giving an LO frequency of 43 MHz) and monitoring the following logic levels:

(Note: Before checking the logic levels connect TP7 momentarily to 0 V).

ML10	pin 3	high	ML11	pin 3	low
	4	high		4	low
	5	high		5	high
	6	low		6	low

If these levels are incorrect, carry out the synthesiser control checks contained in the overall loop check procedure.

Phase comparator and loop integrator

38 An initial check of the phase comparator operation may be carried out by tuning the VCO with a DC voltage applied to LK1 as before. Set the receiver to 1.6 MHz (to set the LO frequency nominally to 43 MHz) and the DC voltage to approximately 16V. Adjust to give a VCO frequency of greater or less than 43 MHz as described below.

39 When the frequency at TP11 is greater than at TP10 (i.e. VCO frequency high) the phase comparator outputs should be similar to Fig.8.4(a) (short pulses at ML16 pin 9, longer pulses at ML12 pin 5) and the loop integrator output at ML1 pin 6 should be driven low (less than 2V). When the frequency at TP11 is less than that at TP10 (i.e. VCO frequency low) the phase comparator outputs should be similar to Fig.8.4(b) and the loop integrator output at TP14 should be driven high (greater than 20 V).

Overall loop

40 With the DC power supply removed and the link replaced the loop should lock with the phase comparator waveforms similar to Fig.8.4(c). The loop integrator should produce a steady DC output voltage at TP14. If there is any instability (an AC waveform at TP14) check the components around the integrator, and the fast lock circuit.

41 If the output frequency does not respond to changes in the setting of the main tuning knob, check ML14 divide outputs. The signal levels on ML14 pins 11 to 14 should be changing as the receiver is tuned across its entire frequency range.

42 To determine if the fault is in ML14, the input data to the device should be checked next. This can be carried out by checking that the write strobe on pin 19 and the levels on data lines D0 to D4 toggle as the synthesiser frequency is tuned. Also the levels on pins 15 and 37 (TP7) should be both high.

Signature Analysis Routine

43 This routine checks that the module control signals are interfaced and decoded correctly from the module bus.

Processor module DIL switch settings: SW1,4,7 OFF
SW2,3,5,6,8 ON

Signature analyser connections and settings:

Start: 9A Extender assembly, negative trigger
Stop: 9A Extender assembly, negative trigger
Clock: 8A Extender assembly, positive trigger
Earth: 1A Extender assembly

Signal	Signature	Test Node					Remarks
+5V	H9A0						
OV	0000						
		DATA BUS INTERFACES					
M-D0	654F	PL1/7A	ML20/2	ML21/3	ML26/3	ML23/18	Module bus
M-D1	7214	PL1/7B	ML20/4	ML21/4	ML26/4	ML23/16	Module bus
M-D2	H670	PL1/6A	ML20/6	ML21/7	ML26/7	ML23/14	Module bus
M-D3	1PUA	PL1/6B	ML20/8	ML21/8	ML26/8	ML23/12	Module bus
M-D4	UACU	PL1/5A	ML20/11	ML21/13	ML26/13	ML23/9	Module bus
M-D5	089H	PL1/5B	ML20/13	ML21/14	ML26/14	ML23/7	Module bus
M-D6	718F	PL1/4A	ML20/15	ML21/17	ML26/17	ML23/5	Module bus
M-D7	4H04	PL1/4B	ML20/17	ML21/18	ML26/18	ML23/3	Module bus

Signature Analysis Routine (continued)

Signal	Signature	Test Node						Remarks
		ADDRESS DECODER						
+5V	H9A0	ML28/2	ML28/3	ML28/4				Supply
M-A0	UF4A	PL1/12A	R139	ML19/6	ML27/6	ML27/9	ML27/10	Module bus
M-A1	0CH4	PL1/12B	R138	ML19/2	ML19/3	ML19/5		Module bus
M-A4	0000	PL1/10A	R137	ML28/10				Module bus
M-A5	0001	PL1/10B	R136	ML28/12				Module bus
M-A6	0001	PL1/9A	R135	ML28/13				Module bus
M-A7	H9A0	PL1/9B	R134	ML28/15				Module bus
0	0000	PL1/14A	R148	ML28/9				Module address
1	0000	PL1/14B	R144	ML28/11				Module address
2	0000	PL1/13A	R141	ML28/14				Module address
3	H9A0	PL1/13B	R140	ML28/1				Module address
M-R/W	3571	PL1/8B	R132	ML27/1	ML27/2	ML27/4		Module bus
M-STB	0000F	PL1/8A	R133	ML24/2				Module bus
ML27/3	PFH1	ML27/3	ML24/1					Address decoder
ML27/6	PFH0	ML27/6	ML23/1	ML23/19				Address decoder
ML24/12	0000F	ML24/12	ML22/2	ML22/4	ML22/10			Module ID
ML19/1	H274	ML19/1	ML19/8					Address decoder
ML19/10	29F4	ML19/10	ML22/1					Address decoder
ML22/3	0000F	ML22/3	ML21/11					PORT 2 strobe
ML19/4	0F2P	ML19/4	ML22/5					Address decoder
ML22/6	0000F	ML22/6	ML26/11					PORT 0 strobe
ML27/8	25PA	ML27/8	ML19/12					Address decoder
ML19/13	HP5A	ML19/13	ML22/9					Address decoder
ML22/8	0000F	ML22/8	ML14/19					Synth. Control
		MODULE IDENT AND 3-STATE BUFFER (ML23)						
ML23/2	0000	ML23/2						ID
ML23/4	H9A0	ML23/4						ID
ML23/6	0000	ML23/6						ID
ML23/8	0000	ML23/8						ID
ML23/11	0000	ML23/11						ID
0V	0000	ML23/13	ML23/15	ML23/17				Buffer
		DATA LATCH (BITE Multiplexer) (ML26)						
ML26/2	96C5	ML26/2	ML29/10					CONTROL A
ML26/5	A070	ML26/5	ML29/11					CONTROL B
ML26/6	CC12	ML26/6	ML29/14					CONTROL C
ML26/9	C6A3	ML26/9	ML29/13					CONTROL D
		DATA LATCH (Range Switching) (ML21)						
C	474U	ML21/2	ML6/1					Gain Control
D	35P7	ML21/5	ML6/8					Gain Control
E	8FC3	ML21/6	ML6/9					Gain Control
F	3P4F	ML21/12	R47					VCO Control
G	0966	ML21/15	R48					VCO Control
H	12U3	ML21/16	R49					VCO Control
ML21/19	527C	ML21/19	ML20/1	ML20/19				Synth. Control
		3-STATE BUFFER (Synthesiser Control) (ML20)						
S	1HF5	ML20/9	ML14/20					D4
R	2683	ML20/12	ML14/21					D3
Q	500P	ML20/14	ML14/22					D2
P	8864	ML20/16	ML14/23					D1
O	6721	ML20/18	ML14/24					D0

ALIGNMENT

44 This procedure details the adjustments required for aligning the 1st LO Synth. Module.

Test Equipment

45 The following items of test equipment, as detailed in Chapter 2, are required for aligning the 1st LO Synth. Module.

(1) Digital Multimeter.
(2) BITE Kit.
(3) Frequency Counter.
(4) DC Power Supply (0-20 V).

Preliminary

46 Remove the 1st LO Synth. Module from the receiver and place it on the bench next to the receiver. Remove the top cover from the module to gain access to the preset components (leave the bottom cover fitted). Reconnect the module to the receiver using the extender assembly and coaxial leads provided with the BITE Kit. Adjust the preset components according to the procedure below.

VCO Frequency Adjustment

47 Remove LK1 and tune the receiver to 0MHz. Connect the DC power supply between TP14 and 0V, set for a voltage of +19V on the varactor line. Connect the frequency counter to the LO output (SK1) and adjust L8 for a frequency of between 43.1 and 43.3 MHz.

PARTS LIST

48 The Racal part number for a complete 1st LO Synthesiser Module is ST86487.

49 Information on the identification and handling of SMDs is provided in Chapter 2. The parts list for the 1st LO Synthesiser Module is as follows:

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R1		220m	Metal Film	0.25	5	943997P	
R2		33k	Thick Film Network			934507U	
R3		33k	Thick Film Network			934507U	
R4			Not Used				
R5	A9	27R	Thick Film Chip	0.125	2	943870H	270
R6	A8	15R	Thick Film Chip	0.125	2	943867V	150
R7	A7	10R	Thick Film Chip	0.125	2	943865X	100
R8	A4	22R	Thick Film Chip	0.125	2	943869T	220
R9	B3	100R	Thick Film Chip	0.125	2	943878J	101
R10	B3	100R	Thick Film Chip	0.125	2	943878J	101
R11	B5	22R	Thick Film Chip	0.125	2	943869T	220
R12	B6	1k	Thick Film Chip	0.125	2	943890L	102
R13	B0	47R	Thick Film Chip	0.125	2	943873W	470
R14	B8	390R	Thick Film Chip	0.125	2	943885B	391
R15	B8	820R	Thick Film Chip	0.125	2	943889X	821
R16	B5	220R	Thick Film Chip	0.125	2	943882M	221
R17	B2	5k6	Thick Film Chip	0.125	2	943899E	562
R18	B1	1k5	Thick Film Chip	0.125	2	943892J	152
R19	B9	390R	Thick Film Chip	0.125	2	943885B	391
R20	B7	220R	Thick Film Chip	0.125	2	943882M	221
R21	B6	100R	Thick Film Chip	0.125	2	943878J	101
R22	C2	270R	Thick Film Chip	0.125	2	943883T	271
R23	C1	5k6	Thick Film Chip	0.125	2	943899E	562
R24	C6	560R	Thick Film Chip	0.125	2	943887Z	561
R25	C4	220R	Thick Film Chip	0.125	2	943882M	221
R26	C1	1k5	Thick Film Chip	0.125	2	943892J	152
R27	C4	1k8	Thick Film Chip	0.125	2	943893A	182
R28	C9	180R	Thick Film Chip	0.125	2	943881V	181
R29	C1	270R	Thick Film Chip	0.125	2	943883T	271
R30	C4	47k	Thick Film Chip	0.125	2	943910E	472
R31	C3	47k	Thick Film Chip	0.125	2	943910E	473
R32	C3	47k	Thick Film Chip	0.125	2	943910E	473
R33	C0	100R	Thick Film Chip	0.125	2	943878J	101
R34	D6	22R	Thick Film Chip	0.125	2	943869T	220
R35	D7	10k	Thick Film Chip	0.125	2	943902F	103
R36	D2	22k	Thick Film Chip	0.125	2	943906B	223
R37	D2	22k	Thick Film Chip	0.125	2	943906B	223
R38	D4	1k	Thick Film Chip	0.125	2	943890L	102
R39	D4	1k	Thick Film Chip	0.125	2	943890L	102
R40	D8	10k	Thick Film Chip	0.125	2	943902F	103
R41	D4	1k	Thick Film Chip	0.125	2	943890L	102
R42	D2	22k	Thick Film Chip	0.125	2	943906B	223
R43	E9	680R	Thick Film Chip	0.125	2	943888G	681
R44	E8	10k	Thick Film Chip	0.125	2	943902F	103
R45	E3	100R	Thick Film Chip	0.125	2	943878J	101
R46	E1	10R	Thick Film Chip	0.125	2	943865X	100
R47	E1	100R	Thick Film Chip	0.125	2	943878J	101
R48	E1	100R	Thick Film Chip	0.125	2	943878J	101
R49	E0	100R	Thick Film Chip	0.125	2	943878J	101
R50	F6	680R	Thick Film Chip	0.125	2	943888G	681
R51	F6	47k	Thick Film Chip	0.125	2	943910E	103
R52	F5	6k8	Thick Film Chip	0.125	2	943900H	682
R53	F5	1k	Thick Film Chip	0.125	2	943890L	102

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R54	F4	150k	Thick Film Chip	0.125	2	943916I	154
R55	F8	470R	Thick Film Chip	0.125	2	943886I	471
R56	F8	470R	Thick Film Chip	0.125	2	943886I	471
R57	F8	470R	Thick Film Chip	0.125	2	943886I	471
R58	F7	100R	Thick Film Chip	0.125	2	943878J	101
R59	F5	47k	Thick Film Chip	0.125	2	943910E	473
R60	F4	220k	Thick Film Chip	0.125	2	943918G	224
R61	F6	10R	Thick Film Chip	0.125	2	943865X	100
R62	F1	10R	Thick Film Chip	0.125	2	943865X	100
R63	G4	22k	Thick Film Chip	0.125	2	943906B	223
R64	G6	10R	Thick Film Chip	0.125	2	943865X	100
R65	G4	15k	Thick Film Chip	0.125	2	943904D	153
R66	G7	470R	Thick Film Chip	0.125	2	943886I	471
R67	G3	22R	Thick Film Chip	0.125	2	943869T	220
R68	G6	12k	Thick Film Chip	0.125	2	943903M	123
R69	G4	15k	Thick Film Chip	0.125	2	943904D	153
R70	G1	47k	Thick Film Chip	0.125	2	943910E	473
R71	G7	470R	Thick Film Chip	0.125	2	943886I	471
R72	H4	33k	Thick Film Chip	0.125	2	943908Z	333
R73	H3	33k	Thick Film Chip	0.125	2	943908Z	333
R74	H6	22k	Thick Film Chip	0.125	2	943906B	223
R75	H6	220k	Thick Film Chip	0.125	2	943918G	224
R76	H5	47k	Thick Film Chip	0.125	2	943910E	473
R77	H2	220R	Thick Film Chip	0.125	2	943882M	221
R78	H6	10R	Thick Film Chip	0.125	2	943865X	100
R79	H4	10k	Thick Film Chip	0.125	2	943902F	103
R80	H3	820R	Thick Film Chip	0.125	2	943889X	821
R81	H4	100R	Thick Film Chip	0.125	2	943878J	101
R82	H3	47k	Thick Film Chip	0.125	2	943910E	473
R83	H3	220k	Thick Film Chip	0.125	2	943918G	224
R84	H3	10R	Thick Film Chip	0.125	2	943865X	100
R85	H2	820R	Thick Film Chip	0.125	2	943889X	821
R86	J9	10R	Thick Film Chip	0.125	2	943865X	100
R87	J5	10k	Thick Film Chip	0.125	2	943902F	103
R88	J5	10k	Thick Film Chip	0.125	2	943902F	103
R89	J5	4k7	Thick Film Chip	0.125	2	943898N	472
R90	J6	1k	Thick Film Chip	0.125	2	943890L	102
R91	J6	22k	Thick Film Chip	0.125	2	943906B	223
R92	J4	10R	Thick Film Chip	0.125	2	943865X	100
R93	J1	10R	Thick Film Chip	0.125	2	943865X	100
R94	J3	2k2	Thick Film Chip	0.125	2	943894R	222
R95	J6	270R	Thick Film Chip	0.125	2	943883T	271
R96	J4	100R	Thick Film Chip	0.125	2	943878J	101
R97	J3	39k	Thick Film Chip	0.125	2	943909Q	393
R98	K6	1k	Thick Film Chip	0.125	2	943890L	102
R99	K5	1k	Thick Film Chip	0.125	2	943890L	102
R100	K1	10R	Thick Film Chip	0.125	2	943865X	100
R101	K3	22R	Thick Film Chip	0.125	2	943869T	220
R102	K2	1k5	Thick Film Chip	0.125	2	943892J	152

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R103	K2	12k	Thick Film Chip	0.125	2	943903M	123
R104	K2	8k2	Thick Film Chip	0.125	2	943901O	822
R105	K1	5k6	Thick Film Chip	0.125	2	943899E	562
R106	K1	22k	Thick Film Chip	0.125	2	943906B	223
R107	K9	10R	Thick Film Chip	0.125	2	943865X	100
R108	L3	4k7	Thick Film Chip	0.125	2	943898N	472
R109	L3	10R	Thick Film Chip	0.125	2	943865X	100
R110	L2	4k7	Thick Film Chip	0.125	2	943898N	472
R111	L1	4k7	Thick Film Chip	0.125	2	943898N	472
R112	L1	4k7	Thick Film Chip	0.125	2	943898N	472
R113	L3	10R	Thick Film Chip	0.125	2	943865X	100
R114	M3	10R	Thick Film Chip	0.125	2	943865X	100
R115	M9	2k2	Thick Film Chip	0.125	2	943894R	222
R116	M7	10k	Thick Film Chip	0.125	2	943902F	103
R117	N9	10R	Thick Film Chip	0.125	2	943865X	100
R118	P7	10R	Thick Film Chip	0.125	2	943865X	100
R119	P6	1k	Thick Film Chip	0.125	2	943890L	102
R120	P6	10R	Thick Film Chip	0.125	2	943865X	100
R121	P9	10R	Thick Film Chip	0.125	2	943865X	100
R122	P9	1k2	Thick Film Chip	0.125	2	943891C	122
R123	P7	150R	Thick Film Chip	0.125	2	943880O	151
R124	P8	10k	Thick Film Chip	0.125	2	943902F	103
R125	P6	1k	Thick Film Chip	0.125	2	943890L	102
R126	R8	1k	Thick Film Chip	0.125	2	943890L	102
R127	R6	47R	Thick Film Chip	0.125	2	943873W	470
R128	P1	10k	Thick Film Chip	0.125	2	943902F	103
R129	S9	10R	Thick Film Chip	0.125	2	943865X	100
R130	T8	10k	Thick Film Chip	0.125	2	943902F	103
R131	T9	100k	Thick Film Chip	0.125	2	943914A	104
R132	S2	22k	Thick Film Chip	0.125	2	943906B	223
R133	T1	22k	Thick Film Chip	0.125	2	943906B	223
R134	T2	22k	Thick Film Chip	0.125	2	943906B	223
R135	T1	22k	Thick Film Chip	0.125	2	943906B	223
R136	T2	22k	Thick Film Chip	0.125	2	943906B	223
R137	T1	22k	Thick Film Chip	0.125	2	943906B	223
R138	T2	22k	Thick Film Chip	0.125	2	943906B	223
R139	T1	22k	Thick Film Chip	0.125	2	943906B	223
R140	T2	22k	Thick Film Chip	0.125	2	943906B	223
R141	T1	22k	Thick Film Chip	0.125	2	943906B	223
R142	T3	47k	Thick Film Chip	0.125	2	943910E	473
R143	T2	47k	Thick Film Chip	0.125	2	943910E	473
R144	T1	22k	Thick Film Chip	0.125	2	943906B	223
R145	V4	10k	Thick Film Chip	0.125	2	943902F	103
R146	V3	22k	Thick Film Chip	0.125	2	943906B	223
R147	V2	22k	Thick Film Chip	0.125	2	943906B	223
R148	V1	22k	Thick Film Chip	0.125	2	943906B	223
R149	V1	33k	Thick Film Chip	0.125	2	943908Z	333
R150	V0	33k	Thick Film Chip	0.125	2	943908Z	333
R151	V4	82k	Thick Film Chip	0.125	2	943913T	823
R152	V4	82k	Thick Film Chip	0.125	2	943913T	823
R153	V4	10k	Thick Film Chip	0.125	2	943902F	103
R154	W4	10k	Thick Film Chip	0.125	2	943902F	103

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R155	W4	15k	Thick Film Chip	0.125	2	943904D	153
R156	W3	10k	Thick Film Chip	0.125	2	943902F	103
R157	W1	33k	Thick Film Chip	0.125	2	943908Z	333
R158	W1	10k	Thick Film Chip	0.125	2	943902F	103
R159	W4	120k	Thick Film Chip	0.125	2	943915R	124
R160	W3	18k	Thick Film Chip	0.125	2	943905K	183
R161	W4	100k	Thick Film Chip	0.125	2	943914A	104
R162	W3	10k	Thick Film Chip	0.125	2	943902F	103
R163	W3	1k	Thick Film Chip	0.125	2	943890L	102
R164	W2	1k	Thick Film Chip	0.125	2	943890L	102
R165	W2	270k	Thick Film Chip	0.125	2	943919N	274
R166	W2	1k	Thick Film Chip	0.125	2	943890L	102
R167	W4	18k	Thick Film Chip	0.125	2	943905K	183
R168	W3	100k	Thick Film Chip	0.125	2	943914A	104
R169	X4	180R	Thick Film Chip	0.125	2	943881V	181
R170	X4	4k7	Thick Film Chip	0.125	2	943898N	472
R171	X3	22k	Thick Film Chip	0.125	2	943906B	223
R172	X1	15k	Thick Film Chip	0.125	2	943904D	153
R173	X4	2k2	Thick Film Chip	0.125	2	943894R	222
R174	Y2	220R	Thick Film Chip	0.125	2	943882M	221
R175	Y4	220R	Thick Film Chip	0.125	2	943882M	221
R176	Y4	220R	Thick Film Chip	0.125	2	943882M	221
R177	Z3	4k7	Thick Film Chip	0.125	2	943898N	472
Capacitors				V			
C1		220µ	Electrolytic	16	-10 +50	941843N	
C2		15µ	Electrolytic	63	-10 +50	926397M	
C3		2µ2	Polycarbonate	100	10	931134H	
C4		68n	Polycarbonate	100	10	945009R	
C5		220µ	Electrolytic	25	-10 +50	945178C	
C6		220µ	Electrolytic	25	-10 +50	945178C	
C7	A8	10p	Ceramic Chip	50	5	941787I	
C8	A6	1µ	Tantalum Chip	35	20	945049Z	
C9	B5	10n	Ceramic Chip	50	10	941775D	
C10	B5	1n	Ceramic Chip	50	10	941772O	
C11	B4	1n	Ceramic Chip	50	10	941772O	
C12	B0	10n	Ceramic Chip	50	10	941775D	
C13	B8	1n	Ceramic Chip	50	10	941772O	
C14	B7	1n	Ceramic Chip	50	10	941772O	
C15	B2	1n	Ceramic Chip	50	10	941772O	
C16	B7	10n	Ceramic Chip	50	10	941775D	
C17	B9	1n	Ceramic Chip	50	10	941772O	
C18	B2	10n	Ceramic Chip	50	10	941775D	
C19	B1	1µ	Tantalum Chip	35	20	945049Z	
C20	B5	10n	Ceramic Chip	50	10	941775D	
C21	B6	10n	Ceramic Chip	50	10	941775D	
C22	B8	1n	Ceramic Chip	50	10	941772O	

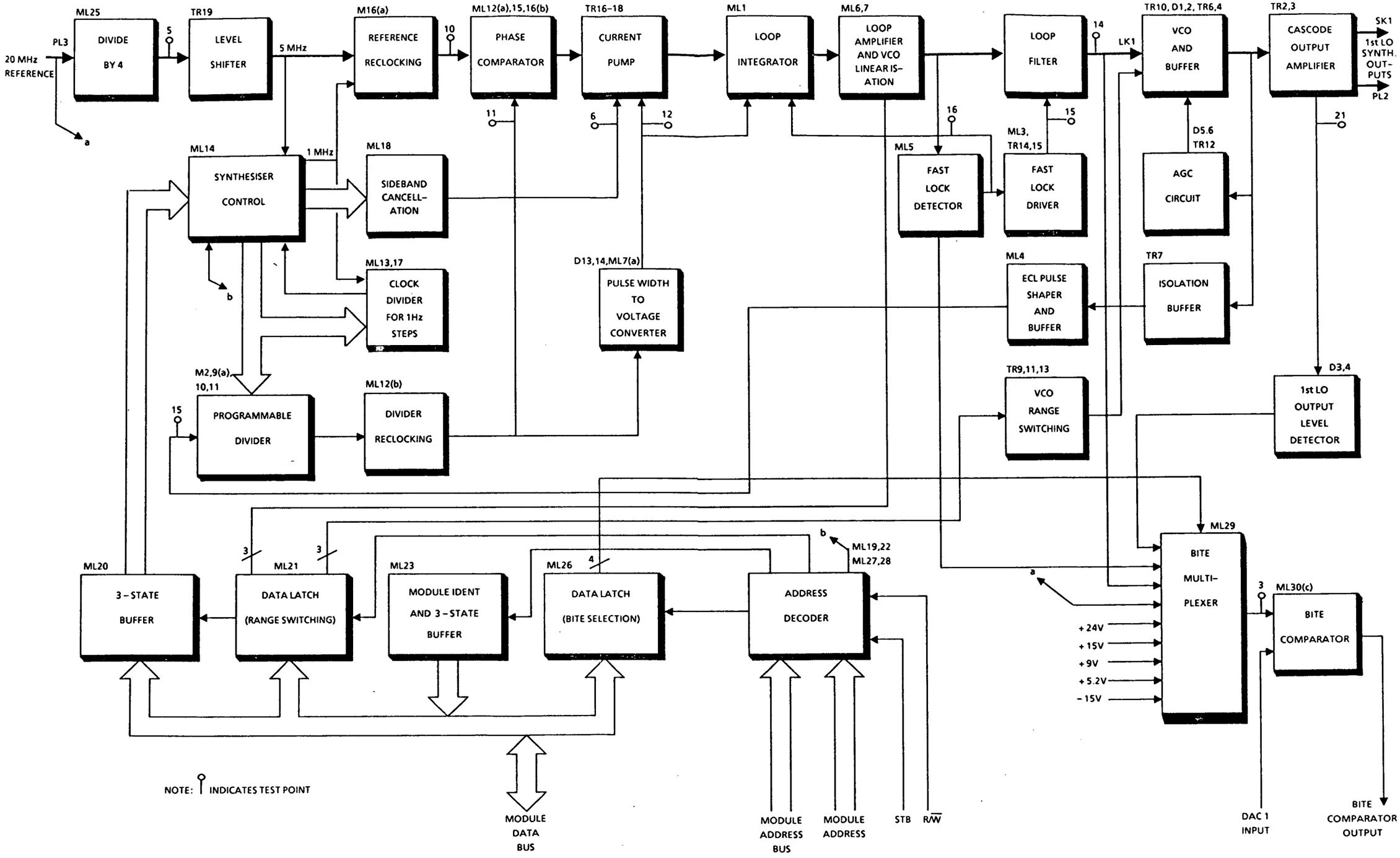
Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C23	B1	10n	Ceramic Chip	50	10	941775D	
C24	B0	10n	Ceramic Chip	50	10	941775D	
C25	C5	100n	Ceramic Chip	50	20	945146T	
C26	C6	1n	Ceramic Chip	50	10	941772O	
C27	C2	10n	Ceramic Chip	50	10	941775D	
C28	C8	1n	Ceramic Chip	50	10	941772O	
C29	C8	1µ	Tantalum Chip	35	20	945049Z	
C30	C8	1n	Ceramic Chip	50	10	941772O	
C31	C4	1n	Ceramic Chip	50	10	941772O	
C32	C5	10n	Ceramic Chip	50	10	941775D	
C33	C8	1n	Ceramic Chip	50	10	941772O	
C34	C3	10n	Ceramic Chip	50	10	941775D	
C35	C7	100p	Ceramic Chip	50	5	941799N	
C36	D5	1n	Ceramic Chip	50	10	941772O	
C37	D9	1n	Ceramic Chip	50	10	941772O	
C38	D8	100n	Ceramic Chip	50	20	945146T	
C39	D4	6µ8	Tantalum Chip	35	20	945052L	
C40	D1	1µ	Tantalum Chip	35	20	945049Z	
C41	D0	10n	Ceramic Chip	50	10	941775D	
C42	D2	10n	Ceramic Chip	50	10	941775D	
C43	D8	1n	Ceramic Chip	50	10	941772O	
C44	D7	100p	Ceramic Chip	50	5	941799N	
C45	D6	12p	Mica Chip	500	2	945133H	
C46	D5	10n	Ceramic Chip	50	10	941775D	
C47	D2	10n	Ceramic Chip	50	10	941775D	
C48	D5	10n	Ceramic Chip	50	10	941775D	
C49	D2	10n	Ceramic Chip	50	10	941775D	
C50	E6	27p	Mica Chip	500	2	945134Y	
C51	E6	47p	Mica Chip	500	2	945135F	
C52	E5	10n	Ceramic Chip	50	10	941775D	
C53	E3	100n	Ceramic Chip	50	20	945146T	
C54	E2	1n	Ceramic Chip	50	10	941772O	
C55	E1	10n	Ceramic Chip	50	10	941775D	
C56	E0	1n	Ceramic Chip	50	10	941772O	
C57	F8	10n	Ceramic Chip	50	10	941772O	
C58	F4	10n	Ceramic Chip	50	10	941775D	
C59	F7	1n	Ceramic Chip	50	10	941772O	
C60	F3	10n	Ceramic Chip	50	10	941775D	
C61	F3	1n	Ceramic Chip	50	10	941772O	
C62	F6	10n	Ceramic Chip	50	10	941775D	
C63	G8	1n	Ceramic Chip	50	10	941772O	
C64	G7	10n	Ceramic Chip	50	10	941775D	
C65	G2	10n	Ceramic Chip	50	10	941775D	
C66	G1	1µ	Tantalum Chip	35	20	945049Z	
C67	G6	10n	Ceramic Chip	50	10	941775D	
C68	H5	1n	Ceramic Chip	50	10	941772O	
C69	H2	10n	Ceramic Chip	50	10	941775D	
C70	H1	10n	Ceramic Chip	50	10	941775D	
C71	H7	33µ	Tantalum Chip	10	20	945054T	
C72	H7	1n	Ceramic Chip	50	10	941772O	
C73	H4	1µ	Tantalum Chip	35	20	945049Z	
C74	H4	10n	Ceramic Chip	50	10	941775D	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C75	J8	1n	Ceramic Chip	50	10	941772O	
C76	J6	1µ	Tantalum Chip	35	20	945049Z	
C77	J5	10n	Ceramic Chip	50	10	941775D	
C78	J4	100n	Ceramic Chip	50	20	945146T	
C79	J6	1µ	Tantalum Chip	35	20	945049Z	
C80	J7	10n	Ceramic Chip	50	10	941775D	
C81	J9	33µ	Tantalum Chip	10	20	945054T	
C82	K8	10n	Ceramic Chip	50	10	941775D	
C83	K6	10n	Ceramic Chip	50	10	941775D	
C84	K3	47n	Ceramic Chip	50	10	945145M	
C85	K3	1n5	Ceramic Chip	50	5	5945148B	
C86	K2	10n	Ceramic Chip	50	10	941775D	
C87	J1	10n	Ceramic Chip	50	10	941775D	
C88	K1	1µ	Tantalum Chip	35	20	945049Z	
C89	K5	10n	Ceramic Chip	50	10	941775D	
C90	K2	10n	Ceramic Chip	50	10	941775D	
C91	K1	10n	Ceramic Chip	50	10	941775D	
C92	K3	33p	Ceramic Chip	50	5	941793J	
C93	L6	33µ	Tantalum Chip	10	20	945054T	
C94	L9	10n	Ceramic Chip	50	10	941775D	
C95	L4	10n	Ceramic Chip	50	10	941775D	
C96	L3	100n	Ceramic Chip	50	20	945146T	
C97	L2	100p	Ceramic Chip	50	5	941799N	
C98	L2	10n	Ceramic Chip	50	10	941775D	
C99	L1	10p	Ceramic Chip	50	5	941787I	
C100	L5	33µ	Tantalum Chip	10	20	945054T	
C101	M8	10n	Ceramic Chip	50	10	941775D	
C102	M8	10n	Ceramic Chip	50	10	941775D	
C103	M3	10n	Ceramic Chip	50	10	941775D	
C104	M9	10n	Ceramic Chip	50	10	941775D	
C105	M2	10n	Ceramic Chip	50	10	941775D	
C106	M2	1n	Ceramic Chip	50	10	941772O	
C107	M1	1n	Ceramic Chip	50	10	941772O	
C108	M1	1n	Ceramic Chip	50	10	941772O	
C109	M1	10n	Ceramic Chip	50	10	941775D	
C110	M0	1n	Ceramic Chip	50	10	941772O	
C111	M0	1n	Ceramic Chip	50	10	941772O	
C112	M0	1n	Ceramic Chip	50	10	941772O	
C113	M0	10n	Ceramic Chip	50	10	941775D	
C114	N8	33µ	Tantalum Chip	10	20	945054T	
C115	N7	10n	Ceramic Chip	50	10	941775D	
C116	N3	1n	Ceramic Chip	50	10	941772O	
C117	N3	1n	Ceramic Chip	50	10	941772O	
C118	N2	1n	Ceramic Chip	50	10	941772O	
C119	N2	1n	Ceramic Chip	50	10	941772O	
C120	N2	1n	Ceramic Chip	50	10	941772O	
C121	P9	1µ	Tantalum Chip	35	20	945049Z	
C122	P7	100n	Ceramic Chip	50	20	945146T	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C123	P6	10n	Ceramic Chip	50	10	941775D	
C124	P8	1n	Ceramic Chip	50	10	941772O	
C125	C6	1µ	Tantalum Chip	35	20	945049Z	
C126	P8	10n	Ceramic Chip	50	10	941775D	
C127	S9	10n	Ceramic Chip	50	10	941775D	
C128	T8	10n	Ceramic Chip	50	10	941775D	
C129	T5	10n	Ceramic Chip	50	10	941775D	
C130	W0	10n	Ceramic Chip	50	10	941775D	
C131	W5	10n	Ceramic Chip	50	10	941775D	
C132	X3	10n	Ceramic Chip	50	10	941775D	
C133	W1	33µ	Tantalum Chip	10	20	945054T	
C134	X0	10n	Ceramic Chip	50	10	941775D	
C135	Y5	10n	Ceramic Chip	50	10	941775D	
C136	Y3	10n	Ceramic Chip	50	10	941775D	
C137	Y2	10n	Ceramic Chip	50	10	941775D	
C138	Y1	10n	Ceramic Chip	50	10	941775D	
C139	Y0	10n	Ceramic Chip	50	10	941775D	
C140	Y3	100n	Ceramic Chip	50	20	945146T	
C141	Y3	1µ	Tantalum Chip	35	20	945049Z	
C142	Y3	10n	Ceramic Chip	50	10	941775D	
C143	Y2	10n	Ceramic Chip	50	10	941775D	
C144	Y1	10n	Ceramic Chip	50	10	941775D	
C145	Z1	1µ	Tantalum Chip	35	20	945049Z	
C146	Z0	100n	Ceramic Chip	50	20	945146T	
C147	Y5	10n	Ceramic Chip	50	10	941775D	
C148	Z5	10n	Ceramic Chip	50	10	941775D	
C149	Z5	10n	Ceramic Chip	50	10	941775D	
C150	Z2	10n	Ceramic Chip	50	10	941775D	
Inductors				W			
L1		1µH	Choke	0.2	10	938966Z	
L2		2µH2	Choke	0.2	10	2922459F	
L3		2µH2	Choke	0.2	10	922459F	
L4		330µH	Choke	0.2	10	939163N	
L5		4µH7	Choke	0.2	10	939887S	
L6		4µH7	Choke	0.2	10	939887S	
L7		4µH7	Choke	0.2	10	939887S	
L8			Coil Assembly			ST87457	
L9	D8	4µH7	Choke		10	945031A	
L10	D7	10µH	Choke		10	945032H	
L11	E8	470µH	Choke		10	945039S	
L12	E1	100µH	Choke		10	945037U	
L13	P9	47µH	Choke		10	945137D	
Transformers							
T1			Transformer Assembly			ST87474	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Diodes							
D1			ZC 714, Varicap			920267O	
D2			ZC 714, Varicap			920267O	
D3	B2		BAT 17, Schottky			943953B	
D4	B1		BAT 17, Schottky			943953B	
D5	C7		BAT 17, Schottky			943953B	
D6	C7		BAT 17, Schottky			943953B	
D7	D5		BAT 18			943955Z	
D8	D5		BAT 18			943955Z	
D9	E5		BAT 18			943955Z	
D10	G4		BAS 16			943951D	
D11	J2		BAS 16			943951D	
D12	J1		BAS 16			943951D	
D13	J5		BAT 17, Schottky			943953B	
D14	J4		BAT 17, Schottky			943953B	
D15	P9		ZC2811E, Schottky			943954S	
D16	P7		BAS 16			943951D	
D17	W2		BAS 16			943951D	
D18	W2		BAS 16			943951D	
D19	X3		BAS 16			943951D	
Transistors							
TR1			BD 140, PNP			941548P	
TR2			2N3866, NPN			917219H	
TR3			2N3866, NPN			917219H	
TR4	B8		BFQ 19, NPN			943944L	
TR5	C2		BCX 55, NPN			945136W	
TR6	C6		BFQ 19, NPN			943944L	
TR7	C8		MMBFU310, FET			943945C	
TR8	D1		BCX 52, PNP			943948H	
TR9	D3		BC 859, PNP			943942N	
TR10	D6		MMBFU310, FET			943945C	
TR11	D3		BC 859, PNP			943942N	
TR12	D8		BC 849, NPN			943941W	
TR13	E3		BC 859, PNP			943942N	
TR14	G2		MMBT2369, FET			943946J	
TR15	G1		BCX 71J, PNP			943950M	
TR16	L2		BCX 71J, PNP			943950M	
TR17	L1		MMBT2369, FET			943946J	
TR18	L2		MMBT2369, FET			943946J	
TR19	P8		MMBT2369, FET			943946J	
TR20	X4		BC 849, NPN			943941W	
TR21	X1		BC 849, NPN			943941W	
TR22	Y4		BCX 55, NPN			945136W	
TR23	Y4		BC 849, NPN			943941W	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Integrated Circuits		CAUTION: *SSD - STATIC SENSITIVE DEVICES					
ML1		*SSD	3140, Operational Amplifier			932204W	
ML2		*SSD	12009, ECL Dual 5/6 Prescaler			945016Z	
ML3		*SSD	3140, Operational Amplifier			932204W	
ML4		*SSD	10115, ECL Qual Line Receiver			935262J	
ML5	F5		339, Quad Voltage Comparator			945023R	
ML6	G5	*SSD	211, Quad Analogue Switch (SPST)			945024I	
ML7	H5		324, Quad Operational Amplifier			945026G	
ML8	J3		211, Quad Analogue Switch (SPST)			945024I	
ML9	J7		74LS27, Triple 3-Input NOR Gate			945013U	
ML10	K9		74LS169, Binary Up/Down Counter			945014B	
ML11	K7		74LS169, Binary Up/Down Counter			945014B	
ML12	K4	*SSD	74HC74, Dual D-Type Flip-Flop			943977L	
ML13	L9	*SSD	4527, BCD Rate Multiplier			945048I	
ML14	L7	*SSD	RMSL 019/A, Digiphase			AD86724 or AD87894	
ML15	L4	*SSD	74HC00, Quad 2-Input NAND Gate			943968V	
ML16	M4	*SSD	74HC74, Dual D-Type Flip-Flop			943977L	
ML17	N9	*SSD	74HC74, Dual D-Type Flip-Flop			943977L	
ML18	N7		08, 8-Bit D/A Converter			945019O	
ML19	N4	*SSD	74HC02, Quad 2-Input NOR Gate			943969C	
ML20	P2	*SSD	74HC244, Octal Line Driver			943987I	
ML21	P1	*SSD	74HC273, D-Type Flip-Flop			943989G	
ML22	P4	*SSD	74HC08, Quad 2-Input AND Gate			943972Y	
ML23	R2	*SSD	74HC244, Octal Line Driver			943987I	
ML24	R4	*SSD	74HC11, Triple 3-Input AND Gate			943974W	
ML25	R9	*SSD	74HC71, Dual D-Type Flip-Flop			943977L	
ML26	S2	*SSD	74HC273, D-Type Flip-Flop			943989G	
ML27	S4	*SSD	74HC00, Quad 2-Input NAND Gate			943968V	
ML28	T3	*SSD	74HC85, 4-Bit Magnitude Comparator			943978S	
ML29	V3	*SSD	4067, 16-Channel Multiplexer			945044M	
ML30	V1		339, Quad Voltage Comparator			945023R	
ML31	X2		324, Quad Op Amp			945026G	
Connectors							
PL1			Plug, 64-way			940339G	
Miscellaneous							
W1			Cable Assembly (complete with PL3)			BA87136	
W2			Cable Assembly (complete with SK1)			BA87135	
W3			Cable Assembly (complete with PL2)			BA87136	
LK1			Comprising:				
			Plug, 4-way			945062S	
			Shorting Link			943684I	
TP1 to TP21			Terminal, Assembly (test points)			936148X	



1st Lo Synthesiser Module: Block Diagram **Fig.8.5**

CHAPTER 9

REFERENCE/BFO MODULE

CONTENTS

ILLUSTRATIONS

CHAPTER 9

REFERENCE/BFO MODULE

INTRODUCTION

1 The Reference/BFO Module may be functionally divided into two distinct sections:

(1) A phase-locked loop (PLL) circuit producing reference outputs at the following frequencies:

(a) 20 MHz to the 1st LO Synthesiser Module.
(b) 40 MHz to the Front End Module.
(c) 2.5 MHz to the BFO section in this module.

The outputs can either be phase locked to an internal 5 MHz reference signal from the Frequency Standard Module or to an external reference source of 1, 5 or 10 MHz, as selected by switches mounted on top of the module. If the internal standard is selected, these switches may be used to select the frequency of the output made available at the rear panel REF IN/OUT socket (SK1) giving a choice of 1, 5 or 10 MHz.

(2) A PLL circuit producing a BFO output signal that may be tuned over the range 1.4 MHz plus or minus 9.99 kHz in 10 Hz steps. This signal is passed to the IF/AF Module to provide the BFO tuning facility.

Fig.9.1 Receiver Block Diagram

MODULE DESCRIPTION

2 The following description should be read in conjunction with the Reference/BFO Block Module and Circuit Diagrams included in this chapter. Component references shown on the Block Diagram allow it to be related to the Circuit Diagram.

REFERENCE CIRCUIT

Reference Oscillator

3 The reference oscillator consists of a crystal voltage controlled oscillator (VCO), its nominal frequency of 20 MHz being controlled by the DC voltage applied to a varactor diode connected in series with the crystal. An increase in varactor voltage causes a decrease in varactor capacitance and hence an increase in oscillator frequency, and vice-versa.

4 The VCO output is amplified, shaped and buffered in order to provide the subsequent stages with squared pulses of sufficient drive level.

1st LO Reference Output

5 A 20 MHz OUTPUT BUFFER accepts the 20 MHz VCO output to provide a buffered 20 MHz reference signal to the 1st LO Synthesiser Module with the required drive level.

2nd LO Output

6 The 40 MHz 2nd LO output to the 2nd Mixer stage in the Front End Module is derived from the 20 MHz signal using a FREQUENCY DOUBLER. This consists of an amplifier operating in Class C to generate many harmonics and a tuned circuit to select the second harmonic, i.e. 40 MHz. A level detector is also included to allow the receiver BITE to monitor the output level.

Dividers

7 A divider chain with a combined division ratio of 20 takes the 20 MHz square wave from the VCO and produces a 1 MHz feedback signal for the PHASE COMPARATOR. The last divider stage restores the signal to a square wave. The 1, 5 and 10 MHz outputs and the 2.5 MHz reference for the BFO PLL are derived using additional divider stages.

5 MHz Output

8 A 5 MHz OUTPUT BUFFER feeds the 5 MHz square wave output from the dividers to a LOW PASS FILTER. This filter converts the square wave into a 5 MHz sine wave which may be used as a reference for optional modules.

Internal/External Standard Amplification

9 In order to buffer and amplify both the internal and external frequency standard inputs to the reference PLL, two similar input amplifiers are used, each consisting of two high gain transistor stages. Only one amplifier is allowed to operate at a time. This is achieved using the INT/EXT switch (SA1) which causes the first stage of the unused amplifier to be switched off. Both amplifier outputs are fed to selection circuitry and the average DC level of either signal is also detected for BITE purposes.

10 The internal frequency standard is powered from a DC voltage applied to PL6.

Frequency Standard Selection

11 Depending on the setting of the INT/EXT switch (SA1), either the internal or external frequency standard input signal is selected by the INTERNAL/EXTERNAL STANDARD SELECT circuit. The selected signal is squared and then passed through a divider, which is set to the appropriate division ratio for providing a 1 MHz reference signal to one input of the PHASE COMPARATOR.

Reference Divider

12 A programmable divider formed by ML7 and ML8 can be set to divide by 5 or 10. Decoded outputs from the frequency selection switches (SA3 and 4) provide preset inputs to the divider to determine its division ratio and also select the signal path. When operating from a 5 MHz internal standard, the division ratio is automatically set to 5 and the switches have no effect. If a 1 MHz external frequency standard is used, the divider is bypassed and the signal is fed via ML13.

External Reference Output

13 When the internal standard is selected, a reference signal is made available at the REF IN/OUT socket (SK1) for external use and is derived from the 20 MHz VCO output dividers using a REFERENCE OUTPUT FREQUENCY SELECT circuit. This circuit is controlled by switches SA3 and 4 to select either a 1, 5 or 10 MHz output which is fed via a REFERENCE OUTPUT AMPLIFIER to obtain the necessary isolation, impedance and drive level for the external output.

Phase Comparator

14 The PHASE COMPARATOR produces negative-going output pulses of length proportional to the phase difference between the 1 MHz reference and feedback signals. If the VCO frequency is too high, ML15(b) is clocked before ML15(a), placing a logic low on ML12 Pin 4. This has no effect until ML15(a) is clocked and puts a logic low on ML12 Pin 5, causing both latches to be cleared. Hence the output consists of very short negative pulses. In the case of a low VCO frequency, ML15(a) is clocked before ML15(b) and its output remains low until ML15(a) is clocked, thus clearing both latches as before. However, this time a longer negative-going output pulse is produced.

15 The nature and timing relationship of these input and output pulses is shown in Fig.9.2. Waveforms are given for the in-lock condition and the out-of-lock condition, when the VCO frequency can be either too high or too low.

Loop Integrator

16 The output pulses from the PHASE COMPARATOR are fed to the LOOP INTEGRATOR which produces a DC voltage at its output. This voltage controls the frequency of the 20 MHz VCO in order to lock the loop.

17 ML17 and ML18 form a FAST LOCK DETECTOR. If the loop goes out-of-lock, ML17 output closes ML18 to reduce the integrator time constant, allowing the loop to lock quickly. A peak detector provides a DC voltage to the BITE to indicate an out-of-lock condition.

BFO CIRCUIT

BFO Oscillator

18 The BFO oscillator consists of a 5.6 MHz VCO running at four times the BFO frequency, its output being squared and buffered before being fed back to the PROGRAMMABLE DIVIDER in the feedback loop. A DIVIDE-BY-4 circuit provides the final BFO frequency of 1.4 MHz.

BFO Output

19 The required drive level for the BFO output is produced by the BFO OUTPUT AMPLIFIER, which incorporates a peak level detector for BITE monitoring purposes. Filtering of the BFO output is performed by a LOW PASS FILTER.

Phase Locked Loop

20 The VCO is connected into a phase-locked loop circuit comprising a PROGRAMMABLE DIVIDER, a PHASE COMPARATOR and a LOOP INTEGRATOR. The operation of this loop is similar to that of the reference circuit except that the division ratio of the divider, and hence the VCO frequency, is controlled by the SYNTHESISER CONTROL.

Synthesiser Control

21 The SYNTHESISER CONTROL employs an LSI device which allows the VCO output frequency to be incrementally adjusted in steps which are much less in size than the 500 kHz reference frequency using a single phase-lock loop. The SYNTHESISER CONTROL is loaded with frequency setting data from the Processor data bus and operates on this information to control the division ratio of the PROGRAMMABLE DIVIDER. The divided VCO frequency is applied to one input of the PHASE COMPARATOR.

22 The actual division ratio is constantly varied between integer values to give the required non-integer division ratio. This effectively gives the PROGRAMMABLE DIVIDER the fractional division capability necessary to achieve the required resolution for the BFO frequency.

23 A 2.5 MHz reference signal from the reference synthesiser circuit is first shifted in level and converted to a 500 kHz reference in the SYNTHESISER CONTROL for application as the second input to the PHASE COMPARATOR. The PHASE COMPARATOR output pulses are integrated by the LOOP INTEGRATOR to produce a DC voltage which controls the VCO frequency. Phase lock is achieved when the divided VCO frequency is equal to the 500 kHz reference frequency. Waveforms at the inputs and outputs of the PHASE COMPARATOR are given in Fig. 9.3 for both in-lock and out-of-lock conditions.

24 D8 and D9 form a fast lock circuit which reduces the loop time constant to allow the loop to regain phase lock quickly after a large frequency change.

25 As with the reference circuit, an in-lock monitor and peak detector is incorporated in the PHASE COMPARATOR to provide monitoring by the BITE.

GENERAL

Bus Interface

26 A unique hardwired code is received on the Module Address input to the Reference/BFO Module via the motherboard. This code is used by the ADDRESS DECODER to detect addresses on the Module Address Bus from the Processor Module and then produce read or write pulses according to the status of the R/W input. These pulses allow the Processor to read data from the 3-STATE BUFFER or write data to either the DATA LATCH or SYNTHESISER CONTROL, using the Module Data Bus. Pulses on the strobe input ensure correct timing of write pulses. The 3-STATE BUFFER gives the Processor access to the Reference/BFO identification code and also the switch status. The DATA LATCH outputs are used to disable the BFO divider, thus muting the BFO output, and to control the BITE MULTIPLEXER.

BITE Measurement System

27 The BITE measurement system, comprising the BITE MULTIPLEXER operating in conjunction with a BITE COMPARATOR, allows the Processor Module to measure various voltages and operating levels in the Reference/BFO Module. The voltage to be measured is selected by the BITE MULTIPLEXER and compared in the BITE COMPARATOR with a voltage generated by a digital to analogue converter (DAC) in the Processor Module. The Processor measures the level of the selected voltage by applying voltages representing upper and lower limits to the comparator and then monitoring the resulting output.

FAULT FINDING

General

28 Fault finding techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the Reference/BFO Module is contained in the following sections.

BITE Tests

29 The following BITE tests for the Reference/BFO Module are arranged in the order in which they are performed or presented for selection.

TEST NUMBER : 201

TITLE : BITE hardware

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : DAC 1 line is set to 2.55 volts (i.e. max). BITE multiplexer input X1 (+5 volts) is selected and the BITE multiplexer output is checked to ensure that it is low.

LIMITS : Less than 0.5V at TP8.

FAULT DIRECTORY : Fault No. 2

TEST NUMBER : 202, 203

TITLE : +5V rail, +15V rail

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : The appropriate BITE multiplexer input is selected and the supply voltage is checked.

LIMITS :

Test No.	Supply	Mux. Input	Mux Limits (TP8)	
			Lower	Upper
202	+ 5 V	X2	1.8 V	2.2 V
203	+15 V	X3	1.7 V	2.2 V

FAULT DIRECTORY : Fault No. 4

TEST NUMBER : 204

TITLE : BFO Ref level

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : BITE multiplexer input X13 is selected when using the internal reference. If an external reference is in use, BITE multiplexer input X15 is selected. The test checks that the frequency standard reference signal is present.

LIMITS : Internal standard; lower limit 0.7 V at TP8
External standard; lower limit 0.25 V at TP8.

FAULT DIRECTORY : Fault No. 5

TEST NUMBER : 205

TITLE : BFO Ref lock

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : BITE multiplexer input X12 is selected. The output of the out-of-lock detector is measured to ensure that the reference loop is in lock.

LIMITS : Upper limit 0.2V at TP8.

FAULT DIRECTORY : Fault No. 6

TEST NUMBER : 206

TITLE : Ref Osc. varac V

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : BITE multiplexer input X10 is selected. The varactor voltage is measured at the operating frequency.

LIMITS :

Mux. Limits (TP8)		Varactor Line	
Lower	Upper	Lower	Upper
0.32 V	1.74V	2 V	12 V

FAULT DIRECTORY : Fault No. 7

TEST NUMBER : 207

TITLE : 40 MHz o/p level

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : BITE multiplexer input X14 is selected, and the 40 MHz detector output is measured.

LIMITS

Mux. Limits (TP8)		Output Level	
Lower	Upper	Lower	Upper
0.5V	—	-2 dBm	—

FAULT DIRECTORY : Fault No. 8

TEST NUMBER	:	208
TITLE	:	BFO lock
PERFORMED	:	Continous, unit confidence test, select test.
DESCRIPTION	:	BITE multiplexer input X9 is selected. The output of the in-lock detector is measured to ensure that the loop is in lock.
LIMITS	:	Upper limit 0.06 V at TP8.
FAULT DIRECTORY	:	Fault No. 11

TEST NUMBER	:	209
TITLE	:	BFO Osc. varac V
PERFORMED	:	Continuous, unit confidence test, select test.
DESCRIPTION	:	BITE multiplexer input X7 is selected. The varactor voltage is measured at the operating frequency.
LIMITS	:	

Mux. Limits (TP8)		Varactor Line	
Lower	Upper	Lower	Upper
0.44 V	1.4 V	3 V	9 V

FAULT DIRECTORY	:	Fault No. 11

TEST NUMBER : 210

TITLE : BFO sweep

PERFORMED : Unit confidence test, select test.

DESCRIPTION : BITE multiplexer input X7 is selected. The BFO frequency is swept from 1.37 MHz to 1.43 MHz in 200 Hz steps and the varactor line is measured at each step.

LIMITS :

Mux. Limits (TP8)		Varactor Line	
Lower	Upper	Lower	Upper
0.44 V	1.4 V	3 V	9 V

FAULT DIRECTORY : Fault No. 11

TEST NUMBER : 211

TITLE : BFO o/p level

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : BITE multiplexer input X8 is selected and the BFO output level is measured.

LIMITS : Lower limit 0.6 V at TP8.

FAULT DIRECTORY : Fault No. 12

Fault Directory

30 Use the following fault directory to identify the fault condition and take the necessary corrective action. Note that all inputs to the module are assumed to be correct.

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
1	Fails to run BITE tests for Ref/BFO Module.	Address decoding/module ident, not responding	Check address decoding/module ident logic operation using signature analysis routine if necessary.
2	BITE hardware fault.	Comparator/multiplexer inoperative.	Use BITE test 201 to check comparator operation. Select all BITE tests for this module to check multiplexer operation for all analogue inputs. Use signature analysis routine to check multiplexer addressing.
3	BITE indicates failure but manual check shows no fault.	(a) BITE hardware fault. (b) Faulty BITE detector.	(a) As above. (b) Check operation of suspect BITE detector.
4	Power supply fault within module.	Faulty component drawing excess current or open circuit choke L1 or L2.	Locate and replace faulty component.
5	Internal/external reference level fault.	(a) Internal/external reference not present at input. (b) Input amplifier failure.	(a) Check connected to module. Check switch settings. (b) Check signal levels.
6	5 MHz, 20 MHz, 40 MHz outputs all incorrect.	No 1 MHz reference to 20 MHz PLL, or 20 MHz PLL out of lock.	Follow 20 MHz loop check procedure.
7	20 MHz level (PL5) low.	VCO or output buffer failure.	Check signal levels for VCO and output buffer.
8	40 MHz level (PL3) low.	Frequency doubler fault.	Check doubler operation and alignment (see circuit diagram).
9	5 MHz level (PL2) low.	5 MHz output circuit fault.	Check divider, 5 MHz output buffer and low pass filter operation.
10	Reference output (SK1) low or absent.	(a) Module not set for operation from internal reference. (b) Reference output select circuit or amplifier fault.	(a) Check switch settings. (b) Check circuit operation, and signal levels.
11	BFO output incorrect frequency.	(a) 20 MHz PLL out of lock. (b) BFO PLL out of lock.	(a) See Fault No.6. (b) Follow BFO loop check procedure.
12	BFO level (PL4) low.	VCO, output divider/buffer or low pass filter faulty.	Check signal levels for these circuits.

20 MHz Loop Check Procedure

1 MHz reference for phase comparator

31 Check the switch settings on top of the module and position of LK3. Ensure that if internal standard is selected, a 5 MHz signal from the frequency standard is present at PL6. If external standard is selected, ensure that a signal at the correct frequency and level (greater than 70 mV rms) is applied to SK1.

32 Check the reference input to the phase comparator at TP20 and ensure that the frequency is 1 MHz. When the loop is locked the VCO frequency is 20 times the frequency at TP20. The loop will not lock if the frequency at TP20 differs from 1 MHz by more than 85 Hz.

20 MHz VCO

33 Ensure that the VCO oscillates and that the drive to the divide by 2 stage is adequate. Check the frequency of oscillation by connecting a frequency counter to TP17. The VCO tuning may be checked by removing LK3 and connecting a variable DC power supply between the R50 side of LK3 and ground to provide a tuning voltage. As the tuning voltage is adjusted in the range 2V – 8V it should be possible to tune the VCO over the range at least 20 MHz $\pm$1500 Hz.

Dividers

34 Check that the dividers in the loop are working correctly and that the frequency at TP18 is the VCO frequency divided by 20.

Phase comparator and loop integrator

35 The operation of the phase comparator may be checked initially by manually tuning the VCO as described above. When the frequency at TP18 is greater than the frequency at TP20 the phase comparator outputs should be similar to Fig. 9.2 (a) (short pulses at ML15 pin 8, longer pulses at ML15 pin 6) and the loop integrator output should be driven high (greater than 12V). When the frequency at TP18 is less than the frequency at TP20 the above situation should be reversed, with the phase comparator output similar to Fig.9.2 (b).

Overall loop

36 Remove the DC power supply and replace LK3. The loop should lock with the phase comparator waveforms being similar to Fig. 9.2 (c). The loop integrator should produce a steady DC output at TP15 to set the VCO frequency to 20 MHz (20 times the frequency at TP20). If there is any instabilty (an AC waveform at TP15) check the components in the loop integrator and the fast lock circuit. In the latter circuit ML18 should be switched off (0 V at ML18 pin 12).

BFO Loop Check Procedure

500 kHz reference for phase comparator

37 Check the reference input to phase comparator at TP4 and ensure that the frequency is 500 kHz. If incorrect, ensure that the 2.5 MHz signal from the reference oscillator is present on TP2 and TP14. If the signal is present on TP2, check the supplies on pins 42 and 43 of the Synthesiser Control device (ML31) before suspecting it as being faulty.

5.6 MHz VCO

38 Ensure that the VCO oscillates and that the drive level to the programmable divider is adequate. The tuning of the VCO may be checked by connecting a variable DC power supply between the R78 side of link LK1 (remove link first) and ground. Connect a frequency counter to TP12. As the tuning voltage is varied over the range 4V to 8V it should be possible to tune the VCO over the range 5.48 MHz to 5.72 MHz.

Programmable divider

39 The operation of the programmable divider may be checked in basic terms by monitoring TP7 with an oscilloscope for the presence of a waveform (frequency unimportant at this stage).

Phase comparator and loop integrator

40 An initial check of the phase comparator operation may be carried out by tuning the VCO with a DC voltage applied to LK1 as described previously.

41 When the frequency at TP7 is greater than that at TP4, the phase comparator outputs should be similar to Fig. 9.3 (a) (short pulses at ML25 pin 8, longer pulses at ML25 pin 5), and the loop integrator output at TP11 should be driven high (greater than 12 V). When the frequency at TP7 is less than at TP4, the phase comparator outputs should be similar to Fig. 9.3 (b) and the loop integrator output at TP11 should be driven low (less than 2 V).

Overall loop

42 With the DC power supply removed and link LK1 replaced the loop should lock with the phase comparator waveforms similar to Fig. 9.3 (c). The loop integrator should produce a steady DC output voltage at TP11. If there is any instability (an AC waveform at TP11), check the components around the integrator.

43 If the BFO frequency does not respond to changes in the BFO tuning, check the Synthesiser Control divide outputs. The signal levels on ML31 pins 13 and 14 should be changing and pins 11 and 12 should be high and low respectively.

44 Further checks of the Synthesiser Control device can be carried out by checking that the write strobe on pin 19 and the levels on data lines D0 to D4 toggle as the BFO is tuned. Also the levels on pins 15 and 37 should be both high (9 V).

Signature Analysis Routine

45 This routine checks that the module control signals are interfaced and decoded correctly from the module bus.

Ensure all the DIL switches on the REF/BFO module under test are set to OFF.

Plug the extender card into the motherboard slot adjacent to theProcessor Module.

Processor Module DIL switch settings: SW1,4,7 OFF
SW2,3,5,6,8 ON

Signature Analyser connection and settings:

Start: 9A Extender assembly, negative trigger
Stop: 9A Extender assembly, negative trigger
Clock: 8A Extender assembly, positive trigger
Earth: 1A Extender assembly

Note : Signatures xxxxF signify a flashing probe indicator.

Signal	Signature	Test Node				Remarks
+5v	H9A0					
OV	0000					
		DATA BUS INTERFACES				
M-DO	503F	PL1/7A	ML30/18	ML24/3	ML31/24	Module bus
M-D1	7214	PL1/7B	ML30/16	ML24/4	ML31/23	Module bus
M-D2	H670	PL1/6A	ML30/14	ML24/7	ML31/22	Module bus
M-D3	1PUA	PL1/6B	ML30/12	ML24/8	ML31/21	Module bus
M-D4	UACU	PL1/5A	ML30/9	ML24/13	ML31/20	Module bus
M-D5	089H	PL1/5B	ML30/7	ML24/14		Module bus
M-D6	718F	PL1/4A	ML30/5	ML24/17		Module bus
M-D7	4H04	PL1/4B	ML30/3	ML24/18		Module bus
		ADDRESS DECODER				
M-A0	UF4A	PL1/12A	R117	ML32/1		Module bus
M-A1	0CH4	PL1/12B	R116	ML32/2		Module bus
M-A2	PU8U	PL1/11A	R115	ML32/3		Module bus
M-A4	0000	PL1/10A	R113	ML33/10		Module bus
M-A5	0001	PL1/10B	R114	ML33/12		Module bus
M-A6	0001	PL1/9A	R111	ML33/13		Module bus
M-A7	H9A0	PL1/9B	R112	ML33/15		Module bus
0	0000	PL1/14A	R124	ML33/9		Module address
1	0000	PL1/14B	R123	ML33/11		Module address
2	0000	PL1/13A	R122	ML33/14		Module address
3	H9A0	PL1/13B	R121	ML33/1		Module address
M-R/W	3571	PL1/8B	ML29/12	ML29/13	ML29/10	Module bus
M-STB	0000F	PL1/8A	ML29/4			Module bus
ML33/3	H9A0	ML33/3	ML33/4	ML33/2		

Signature Analysis Routine (continued)

Signal	Signature	Test Node			Remarks
		ADDRESS DECODER			
ML29/11	PFH1	ML29/11	ML29/5		Address decoder
ML29/6	H9A0	ML29/6	ML32/4		Address decoder
A=B	H9A1	ML33/6	ML32/6	ML29/9	Address decoder
ML29/8	PFH0	ML29/8	ML30/1	ML30/19	Address decoder
ML32/15	H9A0	ML32/15	ML24/11		Address decoder
ML32/14	H9A0	ML32/14	ML29/2	ML29/1	Address decoder
ML29/3	0000F	ML29/3	ML31/19		Address decoder
		MODULE IDENT AND 3-STATE BUFFER			
ML30/2	H9A0	ML30/2			ID
ML30/4	H9A0	ML30/4			ID
ML30/6	0000	ML30/6			ID
ML30/8	0000	ML30/8			ID
ML30/11	0000	ML30/11			ID
		DATA LATCH (BITE Multiplexer)			
Q0	59FP	ML24/2	ML23/10		
Q1	HUC3	ML24/5	ML23/11		
Q2	9F8H	ML24/6	ML23/14		
Q3	3H12	ML24/9	ML23/13		
J	1PUA	ML24/12	ML19/13		Divide 4 clear
CLR	H9A0	ML24/1			
		SWITCHES AND DECODING			
		SW1-4 OFF			
R	0000	ML30/13	ML3/10	ML3/12 ML3/13	Switch decode
T	0000	ML30/15	ML11/3	ML6/1	Switch decode
S	0000	ML30/17	ML11/6	ML6/4	Switch decode
		SW1-4 ON			
RH	9A0	ML30/13	ML3/10	ML3/12 ML3/13	Switch decode
TH	9A0	ML30/15	ML11/3	ML6/1	Switch decode
SH	9A0	ML30/17	ML11/6	ML6/4	Switch decode

ALIGNMENT

46 This procedure details the adjustments available for aligning the Reference/BFO Module.

Test Equipment

47 The following items of test equipment, as detailed in Chapter 2, are required for aligning the Reference/BFO Module.

(1) RF Millivoltmeter.
(2) BITE Kit.ssembly and coaxial leads provided with the BITE Kit. Adjust the preset components according to the procedure below.

Preliminary

48 Remove the Reference/BFO Module from the receiver and place it on the bench next to the receiver. Remove the top cover from the module to gain access to the preset components (leave the bottom cover fitted). Reconnect the module to the receiver using the extender assembly and coaxial leads provided with the BITE Kit. Adjust the preset components according to the procedure below.

Frequency Doubler Adjustment

49 Connect the RF Millivoltmeter, using the 50 ohm impedance input, to PL3. Adjust L3 and L4 for a peak output of greater than -2 dBm.

PARTS LIST

50 The Racal part number for a complete Reference/BFO Module is ST86488.

51 Information on the identification and handling of SMDs is provided in Chapter 2. The parts list for the Reference/BFO Module is as follows:

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R1		33k	Thick Film Network			939281C	
R2		33k	Thick Film Network			934507U	
R3		33k	Thick Film Network			934507U	
R4	B9	10k	Thick Film Chip	0.125	2	943902F	103
R5	B7	10k	Thick Film Chip	0.125	2	943902F	103
R6	B3	180R	Thick Film Chip	0.125	2	943881V	181
R7	B5	100R	Thick Film Chip	0.125	2	943878J	101
R8	B3	1k2	Thick Film Chip	0.125	2	943891C	122
R9	B8	1k	Thick Film Chip	0.125	2	943890L	102
R10	B6	1k	Thick Film Chip	0.125	2	943890L	102
R11	B5	100R	Thick Film Chip	0.125	2	943878J	101
R12	B9	6k8	Thick Film Chip	0.125	2	943900H	682
R13	B7	6k	Thick Film Chip	0.125	2	943900H	682
R14	B9	10k	Thick Film Chip	0.125	2	943902F	103
R15	B7	10k	Thick Film Chip	0.125	2	943902F	103
R16	C9	820R	Thick Film Chip	0.125	2	943889X	821
R17	C7	820R	Thick Film Chip	0.125	2	943889X	821
R18	C0	330k	Thick Film Chip	0.125	2	943920L	331
R19	C5	1k	Thick Film Chip	0.125	2	943890L	102
R20			Not Used				
R21	C2	100R	Thick Film Chip	0.125	2	943878J	101
R22	C9	1k	Thick Film Chip	0.125	2	943890L	102
R23	C7	1k	Thick Film Chip	0.125	2	943890L	102
R24	C4	22R	Thick Film Chip	0.125	2	943869T	220
R25	C3	10R	Thick Film Chip	0.125	2	943865X	100
R26	D9	10k	Thick Film Chip	0.125	2	943902F	103
R27	D7	10k	Thick Film Chip	0.125	2	943902F	103
R28	D2	330R	Thick Film Chip	0.125	2	943884K	331
R29	D9	1k	Thick Film Chip	0.125	2	943890L	102
R30	D7	470R	Thick Film Chip	0.125	2	943886I	471
R31	D9	10k	Thick Film Chip	0.125	2	943902F	103
R32	D8	22R	Thick Film Chip	0.125	2	943869T	220
R33	D7	10k	Thick Film Chip	0.125	2	943902F	103
R34	D6	22R	Thick Film Chip	0.125	2	943869T	220
R35	D1	100R	Thick Film Chip	0.125	2	943878J	101
R36	D9	100k	Thick Film Chip	0.125	2	943914A	104
R37	D7	100k	Thick Film Chip	0.125	2	943914A	104
R38	D5	10R	Thick Film Chip	0.125	2	943865X	100
R39	C0	10R	Thick Film Chip	0.125	2	943865X	100
R40	G1	4k7	Thick Film Chip	0.125	2	943898N	472
R41	G1	330R	Thick Film Chip	0.125	2	943884K	331
R42	H3	1k	Thick Film Chip	0.125	2	943890L	102
R43	H2	100R	Thick Film Chip	0.125	2	943878J	101
R44	H1	820R	Thick Film Chip	0.125	2	943889X	821
R45	H1	10k	Thick Film Chip	0.125	2	943902F	103
R46	H4	10R	Thick Film Chip	0.125	2	943865X	100
R47	H6	2k2	Thick Film Chip	0.125	2	943894R	222
R48	H6	270k	Thick Film Chip	0.125	2	943919N	274
R49	H4	2k2	Thick Film Chip	0.125	2	943894R	222
R50	H4	10k	Thick Film Chip	0.125	2	943902F	103
R51	H3	47k	Thick Film Chip	0.125	2	943910E	473
R52	H2	3k3	Thick Film Chip	0.125	2	943896P	332

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R53	H1	6k8	Thick Film Chip	0.125	2	943900H	682
R54	H7	10k	Thick Film Chip	0.125	2	943902F	103
R55	H6	10k	Thick Film Chip	0.125	2	943902F	103
R56	H4	100k	Thick Film Chip	0.125	2	943914A	104
R57	J4	1k	Thick Film Chip	0.125	2	943890L	102
R58	J1	100R	Thick Film Chip	0.125	2	943878J	101
R59	J2	22k	Thick Film Chip	0.125	2	943906B	223
R60	J2	10k	Thick Film Chip	0.125	2	943902F	103
R61	J1	10k	Thick Film Chip	0.125	2	943902F	103
R62	J9	10R	Thick Film Chip	0.125	2	943865X	100
R63	J4	100k	Thick Film Chip	0.125	2	943914A	104
R64	J4	220k	Thick Film Chip	0.125	2	943918G	224
R65	K8	150k	Thick Film Chip	0.125	2	943916I	154
R66	K4	10R	Thick Film Chip	0.125	2	943865X	100
R67	K4	3k3	Thick Film Chip	0.125	2	943896P	332
R68	L4	5k6	Thick Film Chip	0.125	2	943899E	562
R69	L8	10k	Thick Film Chip	0.125	2	943902F	103
R70	L4	220k	Thick Film Chip	0.125	2	943918G	224
R71	M7	100k	Thick Film Chip	0.125	2	943914A	104
R72	M3	10k	Thick Film Chip	0.125	2	943902F	103
R73	M7	10R	Thick Film Chip	0.125	2	943865X	100
R74	M4	39k	Thick Film Chip	0.125	2	943909Q	393
R75	M2	100k	Thick Film Chip	0.125	2	943914A	104
R76	M6	56k	Thick Film Chip	0.125	2	943911V	563
R77	M6	100k	Thick Film Chip	0.125	2	943914A	104
R78	M5	3k3	Thick Film Chip	0.125	2	943896P	332
R79	N9	10R	Thick Film Chip	0.125	2	943865X	100
R80	N7	100k	Thick Film Chip	0.125	2	943914A	104
R81	N4	100k	Thick Film Chip	0.125	2	943914A	104
R82	N3	100k	Thick Film Chip	0.125	2	943914A	104
R83	N3	150k	Thick Film Chip	0.125	2	943916I	154
R84			Not Used				
R85	N3	18k	Thick Film Chip	0.125	2	943905K	183
R86	N2	100k	Thick Film Chip	0.125	2	943914A	104
R87	N2	100k	Thick Film Chip	0.125	2	943914A	104
R88	N9	100k	Thick Film Chip	0.125	2	943914A	104
R89	N9	100k	Thick Film Chip	0.125	2	943914A	104
R90	P8	100k	Thick Film Chip	0.125	2	943914A	104
R91	P7	150k	Thick Film Chip	0.125	2	943916I	154
R92	P7	22k	Thick Film Chip	0.125	2	943906B	223
R93	P9	100k	Thick Film Chip	0.125	2	943914A	104
R94	R4	10k	Thick Film Chip	0.125	2	943902F	103
R95	R4	15k	Thick Film Chip	0.125	2	943904D	153
R96	R3	10k	Thick Film Chip	0.125	2	943902F	103
R97	R3	18k	Thick Film Chip	0.125	2	943905K	183
R98	R3	120k	Thick Film Chip	0.125	2	943915R	124
R99	R2	100k	Thick Film Chip	0.125	2	943914A	104
R100	R2	18k	Thick Film Chip	0.125	2	943905K	183

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R101	R2	100k	Thick Film Chip	0.125	2	943914A	104
R102	R8	100R	Thick Film Chip	0.125	2	943878J	101
R103	S7	10R	Thick Film Chip	0.125	2	943865X	100
R104	S7	2k2	Thick Film Chip	0.125	2	943894R	222
R105	S9	10R	Thick Film Chip	0.125	2	943865X	100
R106	S9	220R	Thick Film Chip	0.125	2	943882M	221
R107	S8	2k2	Thick Film Chip	0.125	2	943894R	222
R108	S8	4k7	Thick Film Chip	0.125	2	943898N	472
R109	T1	22k	Thick Film Chip	0.125	2	943906B	223
R110	T2	22k	Thick Film Chip	0.125	2	943906B	223
R111	T1	22k	Thick Film Chip	0.125	2	943906B	223
R112	T2	22k	Thick Film Chip	0.125	2	943906B	223
R113	T1	22k	Thick Film Chip	0.125	2	943906B	223
R114	T2	22k	Thick Film Chip	0.125	2	943906B	223
R115	T1	22k	Thick Film Chip	0.125	2	943906B	223
R116	T2	22k	Thick Film Chip	0.125	2	943906B	223
R117	T1	22k	Thick Film Chip	0.125	2	943906B	223
R118	V8	1k2	Thick Film Chip	0.125	2	943891C	122
R119	V9	1k	Thick Film Chip	0.125	2	943890L	102
R120	V6	10k	Thick Film Chip	0.125	2	943902F	103
R121	V1	22k	Thick Film Chip	0.125	2	943906B	223
R122	V1	22k	Thick Film Chip	0.125	2	943906B	223
R123	V1	22k	Thick Film Chip	0.125	2	943906B	223
R124	V1	22k	Thick Film Chip	0.125	2	943906B	223
Capacitors				V			
C1		1µ	Polycarbonate	100	10	931133Q	
C2		1µ	Polycarbonate	100	10	931133Q	
C3	A6	100n	Ceramic Chip	50	20	945146T	
C4	B5	10n	Ceramic Chip	50	10	941775D	
C5			Not Used				
C6	B2	270p	Ceramic Chip	50	5	941804M	
C7	B1	82p	Ceramic Chip	50	5	941798W	
C8	B0	10n	Ceramic Chip	50	10	941775D	
C9	B9	10n	Ceramic Chip	50	10	941775D	
C10	B7	10n	Ceramic Chip	50	10	941775D	
C11	B3	33p	Ceramic Chip	50	5	941793J	
C12	B8	10n	Ceramic Chip	50	10	941775D	
C13	B6	10n	Ceramic Chip	50	10	941775D	
C14	C2	10n	Ceramic Chip	50	10	941775D	
C15	C1	68p	Ceramic Chip	50	5	941797F	
C16	B2	47p	Ceramic Chip	50	5	941795H	
C17	C5	10n	Ceramic Chip	50	10	941775D	
C18			Not Used				
C19	C0	10n	Ceramic Chip	50	10	941775D	
C20	C9	10n	Ceramic Chip	50	10	941775D	
C21	C8	10n	Ceramic Chip	50	10	941775D	
C22	C7	10n	Ceramic Chip	50	10	941775D	

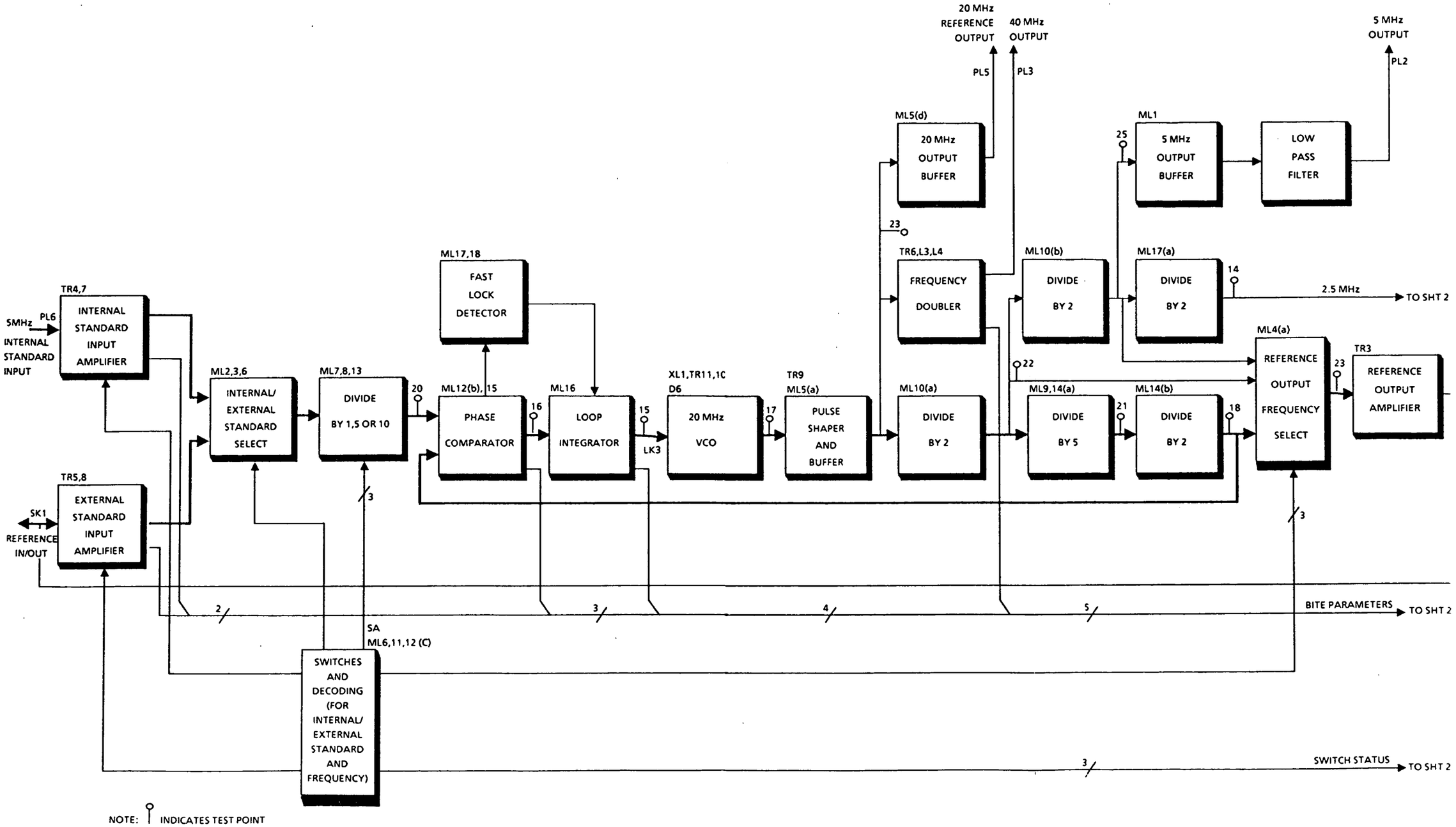
Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C23	C6	10n	Ceramic Chip	50	10	941775D	
C24	C8	1µ	Tantalum Chip	35	20	945049Z	
C25	C6	1µ	Tantalum Chip	35	20	945049Z	
C26	C4	1µ	Tantalum Chip	35	20	945049Z	
C27	C3	33p	Ceramic Chip	50	5	941793J	
C28	C3	10n	Ceramic Chip	50	10	941775D	
C29	D1	6µ8	Tantalum Chip	35	20	945052L	
C30	D8	33µ	Tantalum Chip	10	20	945054T	
C31	D6	33µ	Tantalum Chip	10	20	945054T	
C32	D2	10n	Ceramic Chip	50	10	941775D	
C33	D3	10n	Ceramic Chip	50	10	941775D	
C34	D0	150p	Ceramic Chip	50	5	941801X	
C35	D8	10n	Ceramic Chip	50	10	941775D	
C36	D6	10n	Ceramic Chip	50	10	941775D	
C37	D8	10n	Ceramic Chip	50	10	941775D	
C38	D6	10n	Ceramic Chip	50	10	941775D	
C39	E8	10n	Ceramic Chip	50	10	941775D	
C40	E2	10n	Ceramic Chip	50	10	941775D	
C41	E5	10n	Ceramic Chip	50	10	941775D	
C42	E5	33µ	Tantalum Chip	10	20	945054T	
C43	E0	10n	Ceramic Chip	50	10	941775D	
C44	F1	10n	Ceramic Chip	50	10	941775D	
C45	F8	10n	Ceramic Chip	50	10	941775D	
C46	F6	10n	Ceramic Chip	50	10	941775D	
C47	F4	10n	Ceramic Chip	50	10	941775D	
C48	F2	10n	Ceramic Chip	50	10	941775D	
C49	G8	10n	Ceramic Chip	50	10	941775D	
C50	G6	10n	Ceramic Chip	50	10	941775D	
C51	G4	10n	Ceramic Chip	50	10	941775D	
C52	G3	10n	Ceramic Chip	50	10	941775D	
C53	G2	10n	Ceramic Chip	50	10	941775D	
C54	G1	1µ	Tantalum Chip	35	20	945049Z	
C55	G1	10n	Ceramic Chip	50	10	941775D	
C56	H3	33µ	Tantalum Chip	10	20	945054T	
C57	H2	10n	Ceramic Chip	50	10	941775D	
C58	H7	10n	Ceramic Chip	50	10	941775D	
C59	H6	10n	Ceramic Chip	50	10	941775D	
C60	H4	10n	Ceramic Chip	50	10	941775D	
C61	H3	10n	Ceramic Chip	50	10	941775D	
C62	H3	100p	Ceramic Chip	50	5	941799N	
C63	H9	100p	Ceramic Chip	50	20	945146T	
C64	H1	10n	Ceramic Chip	50	10	941775D	
C65	H2	10n	Ceramic Chip	50	10	941775D	
C66	H2	330p	Ceramic Chip	50	5	941805D	
C67	H1	10n	Ceramic Chip	50	10	941775D	
C68	J4	33µ	Tantalum Chip	10	20	945054T	
C69	J6	10n	Ceramic Chip	50	10	941775D	
C70	J7	10n	Ceramic Chip	50	10	941775D	
C71	J2	6µ8	Tantalum Chip	35	20	945052L	
C72	J1	1µ	Tantalum Chip	35	20	945049Z	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C73	J5	47n	Ceramic Chip	50	10	945145M	
C74	K8	68p	Ceramic Chip	50	5	941797F	
C75	L8	220p	Ceramic Chip	50	5	941803V	
C76	L3	33µ	Tantalum Chip	10	20	945054T	
C77	L3	10n	Ceramic Chip	50	10	941775D	
C78	L4	10n	Ceramic Chip	50	10	941775D	
C79	L8	10n	Ceramic Chip	50	10	941775D	
C80	L7	10n	Ceramic Chip	50	10	941775D	
C81	L3	1n	Ceramic Chip	50	10	941772O	
C82	M5	22n	Ceramic Chip	50	10	941776U	
C83	M4	1n	Ceramic Chip	50	10	941772O	
C84	M7	10n	Ceramic Chip	50	10	941775D	
C85	M2	10n	Ceramic Chip	50	10	941775D	
C86	M1	10n	Ceramic Chip	50	10	941775D	
C87	M1	10n	Ceramic Chip	50	10	941775D	
C88	M1	10n	Ceramic Chip	50	10	941775D	
C89	M0	10n	Ceramic Chip	50	10	941775D	
C90	M0	10n	Ceramic Chip	50	10	941775D	
C91			Not Used				
C92	M3	39p	Ceramic Chip	50	5	941794A	
C93	M8	10n	Ceramic Chip	50	10	941775D	
C94	N7	33µ	Tantalum Chip	10	20	945054T	
C95	N2	10n	Ceramic Chip	50	10	941775D	
C96	N7	470p	Ceramic Chip	50	5	941807B	
C97	P8	22n	Ceramic Chip	50	10	941776U	
C98	P2	10n	Ceramic Chip	50	10	941775D	
C99	P0	10n	Ceramic Chip	50	10	941775D	
C100	P7	10n	Ceramic Chip	50	10	941775D	
C101	P8	10n	Ceramic Chip	50	10	941775D	
C102	P5	10n	Ceramic Chip	50	10	941775D	
C103	R5	10n	Ceramic Chip	50	10	941775D	
C104	R7	10n	Ceramic Chip	50	10	941775D	
C105	R8	33µ	Tantalum Chip	10	20	945054T	
C106	R2	10n	Ceramic Chip	50	10	941775D	
C107	S3	10n	Ceramic Chip	50	10	941775D	
C108	S8	1µ	Tantalum Chip	35	20	945049Z	
C109	T8	10n	Ceramic Chip	50	10	941775D	
C110	T9	100n	Ceramic Chip	50	20	945146T	
C111	T8	10n	Ceramic Chip	50	10	941775D	
C112	V3	10n	Ceramic Chip	50	10	941775D	
C113	W4	10n	Ceramic Chip	50	10	941775D	
C114	Y1	10n	Ceramic Chip	50	10	941775D	
C115	Y1	10n	Ceramic Chip	50	10	941775D	
C116	Y1	10n	Ceramic Chip	50	10	941775D	
C117	Y1	10n	Ceramic Chip	50	10	941775D	
C118	B3	10n	Ceramic Chip	50	10	941775D	

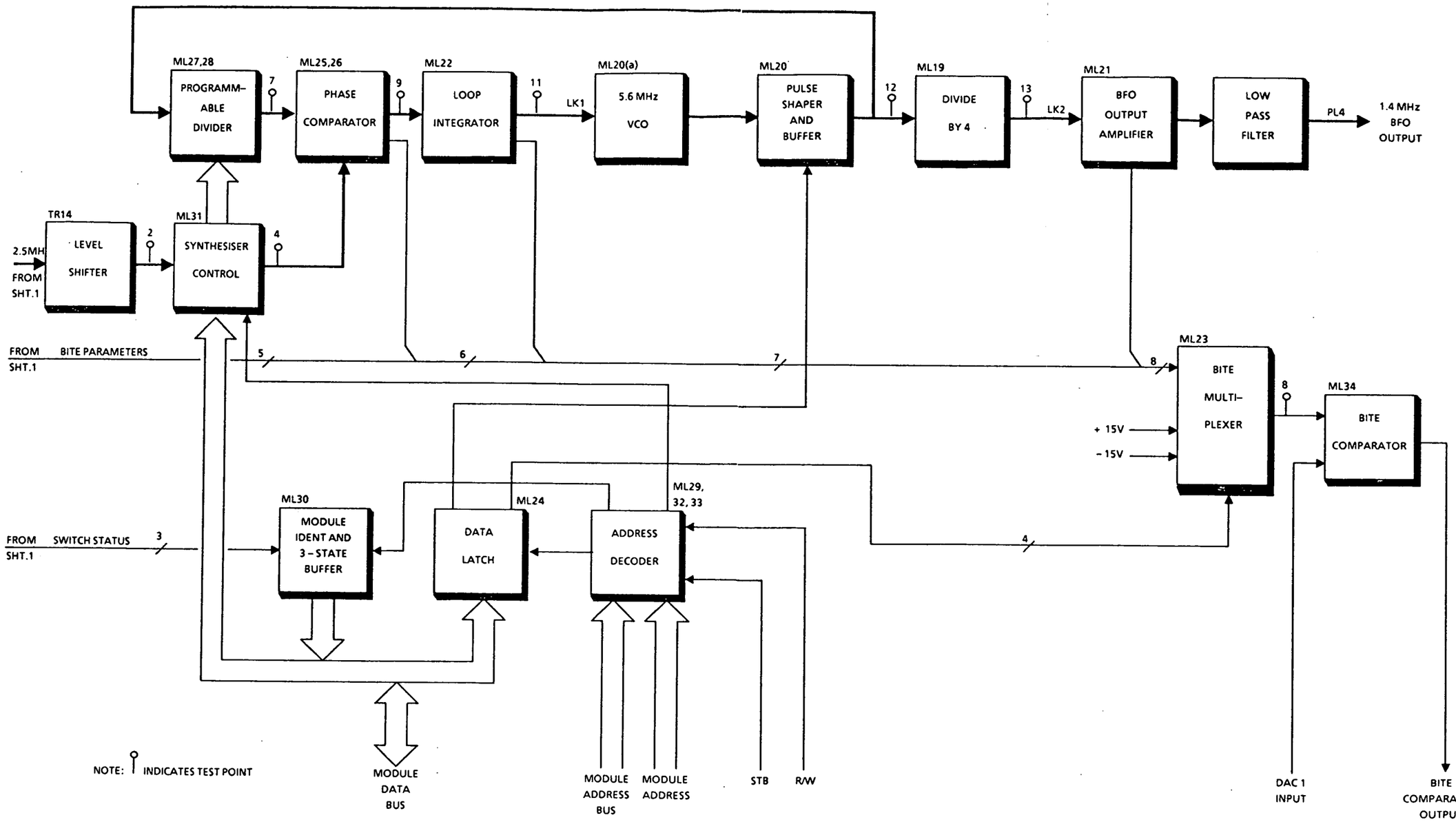
Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Inductors							
L1		10µH	Choke		10	922364Q	
L2		10µH	Choke		10	922364Q	
L3			Choke, Variable			945061B	
L4			Choke, Variable			945061B	
L5		6µH8	Choke		10	939694S	
L6		6µH8	Choke		10	939694S	
L7	B3	47µH	Choke		10	945036N	
L8	C3	47µH	Choke		10	945036N	
L9	C2	10µH	Choke		10	945032H	
L10	C8	10µH	Choke		10	945032H	
L11	C7	10µH	Choke		10	945032H	
L12	C0	470nH	Choke		10	945029V	
L13	G0	10µH	Choke		10	945032H	
L14	J1	10µH	Choke		10	945032H	
L15	K8	33µH	Choke		10	945035W	
L16	L8	100µH	Choke		10	945037U	
L17	M3	33µH	Choke		10	945035W	
L18	T9	47µH	Choke		10	945036N	
Diodes							
D1	B4		Not Used				
D2	B0		BAS 16			943951D	
D3	B4		Not Used				
D4	B0		BAS 16			943951D	
D5	H9		BAS 16			943951D	
D6	J3		ZC 834A, Varicap			945204W	
D7	L8		BAS 16			943951D	
D8	M5		BAS 16			943951D	
D9	M5		BAS 16			943951D	
D10	M4		ZC 836A, Varicap			943956Q	
D11	R8		BAS 16			943951D	
D12	T9		BAS 16			943951D	
D13	T8		ZC2811E, Schottky			943954S	
Transistors							
TR1	B8		BC 849 NPN			943941W	
TR2	B6		BC 849 NPN			943941W	
TR3	B5		MMBT2369 NPN			943946J	
TR4	C8		MMBT2369 NPN			943946J	
TR5	C6		MMBT2369 NPN			943946J	
TR6	C0		BCX 55 NPN			945136W	
TR7	D9		MMBT2369 NPN			943946J	
TR8	D7		MMBT2369 NPN			943946J	
TR9	G1		MMBT2369 NPN			943946J	
TR10	H2		MMBT2369 NPN			943946J	
TR11	J1		MMBT2369 NPN			943946J	
TR12	L4		BC 849 NPN			943941W	
TR13	T8		BC 849 NPN			943941W	
TR14	V8		MMBT2369 NPN			943946J	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Integrated Circuits		CAUTION:	*SSD - STATIC SENSTITVE DEVICES				
ML1	D3	*SSD	74HC00, QUAD 2-Input NAND Gate			943968V	
ML2	E8	*SSD	74HC00, QUAD 2-Input NAND Gate			943968V	
ML3	E6	*SSD	74HC00, QUAD 2-Input NAND Gate			943968V	
ML4	E3	*SSD	74HC153, Dual 4-Channel Multiplexer			943983M	
ML5	E1	*SSD	74HC00, QUAD 2-Input NAND Gate			943968V	
ML6	F8	*SSD	74HC08, Quad 2-Input AND Gate			943972Y	
ML7	F6	*SSD	74HC191, Up/Down Binary Counter			943985K	
ML8	F5	*SSD	74HC74, Dual D-Type Flip/Flop			943977L	
ML9	F3	*SSD	74HC191, Up/Down Binary Counter			943985K	
ML10	F1	*SSD	F174HC74, Dual D-Type Flip/Flop			943977L	
ML11	G8	*SSD	74HC02, Quad 2-Input NOR Gate			943969C	
ML12	G6	*SSD	74HC32, Quad 2-Input OR Gate			943975D	
ML13	G5	*SSD	74HC153, Dual 4-Channel Multiplexer			943983M	
ML14	G3	*SSD	74HC74, Dual D-Type Flip/Flop			943977L	
ML15	H8	*SSD	74HC74, Dual D-Type Flip/Flop			943977L	
ML16	H5		081, Operational Amplifier			945085L	
ML17	J8	*SSD	74HC74, Dual D-Type Flip/Flop			943977L	
ML18	J6	*SSD	4066, Qual Bilateral Switch			945043V	
ML19	L5	*SSD	74HC74, Dual D-Type Flip/Flop			943977L	
ML20	L3	*SSD	74HC00, QUAD 2-Input NAND Gate			943968V	
ML21	M8	*SSD	74HC00, QUAD 2-Input NAND Gate			943968V	
ML22	N8		081, Operational Amplifier			945085L	
ML23	P3	*SSD	4067, 16-Channel Multiplexer			945044M	
ML24	P1	*SSD	74HC273, Octal D-Type Flip-Flop			943989G	
ML25	P7	*SSD	74HC74, Dual D-Type Flip/Flop			943977L	
ML26	P6	*SSD	74HC00, QUAD 2-Input NAND Gate			943968V	
ML27	R7	*SSD	74HC74, Dual D-Type Flip/Flop			943977L	
ML28	R6	*SSD	74HC191, Up/Down Binary Counter			943985K	
ML29	S4	*SSD	74HC00, QUAD 2-Input NAND Gate			943968V	
ML30	S2	*SSD	74HC244, Octal Line Driver			943987I	
ML31	T6	*SSD	RMSL 019/A, Digiphase			AD86724	
ML32	T4	*SSD	74HC138, 3 to 8 Line Decoder			943980X	
ML33	V4	*SSD	74HC85, 4-Bit Magnitude Comparator			943978S	
ML34	W4		339, Quad Voltage Comparator			945023R	
Connectors							
PL1			Plug, 64 way, Pin Contacts			940339G	
Switches							
SA			Slide, DIL			945028E	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Miscellaneous							
W1			Cable Assembly			BA87135	
W2			Cable Assembly			BA87136	
W3			Cable Assembly			BA87136	
W4			Cable Assembly			BA87136	
W5			Cable Assembly			BA87136	
W6			Cable Assembly			BA87136	
TP1 to TP25			Terminal, Assembly (test points)			936148X	
LK1			Shorting Link			943684I	
LK3			Shorting Link			943684I	
XL1			Crystal, Quartz 20 MHz			AD80547	



Reference/BFO Module:
Block Diagram (Sht 1) **Fig.9.4**



Reference/BFO Module: Block Diagaram (Sht 2) **Fig.9.5**

CHAPTER 10

PROCESSOR MODULE (SERIAL)

CONTENTS

TABLE

ILLUSTRATIONS

CHAPTER 10

PROCESSOR MODULE (SERIAL)

INTRODUCTION

1 The Processor Module communicates with all modules connected to a module bus carried by the motherboard. It processes operational control settings to provide the necessary command signals for controlling various functions within these modules. The control settings may be received either from the Front Panel Assembly or via the RS423 remote interface at the rear of the module in serial ASCII format.

Fig. 10.1 Receiver Block Diagram

2 The processing is performed by a 16-bit 68000 microprocessor supported by 256 kbytes of EPROM, 64 kbytes of RAM and 8 kbytes of EEPROM. Communication is via parallel interface/timers (PI/T), serial RS423 ports and digital to analogue converters (DACs).

3 BITE programs stored in the EPROM allow the Processor to perform comprehensive tests of the receiver's performance. A signature analysis facility is also provided as a further aid to locating faults in the digital circuits to component level

MODULE DESCRIPTION

4 The following description should be read in conjunction with the Processor Module Block and Circuit Diagrams included with this chapter. Component references shown on the Block Diagram allow it to be related to the Circuit Diagram.

Processor

5 The PROCESSOR fetches data either from the input or memory devices, processes the information according to program code stored in the EPROM, and then sends the results of these computations to an output or memory device. The PROCESSOR is driven from an 8 MHz CRYSTAL OSCILLATOR by means of which all its actions and those of the supporting devices are synchronised.

6 If desired, the internal clock for the PROCESSOR may be disabled by connecting ML16 pin 4 to 0 V via link LK2. This link may also be removed to permit the connection of an external clock source for test purposes.

Address Decoding

7 According to the status of address lines A18-22, the ADDRESS DECODER asserts the appropriate select line to allow the various on-board devices to communicate with the PROCESSOR, thereby ensuring that only the relevant data is routed to and from these devices. The ADDRESS DECODER is disabled by the 3-bit function code (FC0-3) during interrupts.

Internal Bus Structure

8 Address lines A1-17 form the ADDRESS BUS. This is used by the PROCESSOR to address the memory and interface devices to allow data transfer via a 16-bit bidirectional DATA BUS. This bus is split into two bytes (D0-7 and D8-15) and is interfaced to the PROCESSOR via a bidirectional DATA BUFFER. Data transfers are handled by control signals on the CONTROL BUS.

9 During data transactions, acknowledgement to the PROCESSOR that data transfer is completed is produced by the DTACK COUNTER to terminate the bus cycle.

Memory Devices

10 As well as providing storage for the main program, the EPROM contains the BITE program which is initiated at power-up, returning to the normal program on completion of testing. Included with the main program are the continuous BITE tests which are performed automatically without operator intervention. Signature analysis routines are also held in this memory.

11 Non-volatile storage of operational settings for up to 100 channels and power-down information containing the current front panel settings and receiver configuration is provided by the EEPROM, which requires no back-up battery supply. Data can be written into this memory when bit 7 of port B of PARALLEL I/O INTERFACE TIMER 2 is driven to active low. The current operational settings are updated if a change has occurred since they were last copied to the EEPROM, but only if they remain at these settings for more than one minute.

12 Two 32k by 8 static RAM devices form the RAM store. In addition to storing the front panel settings, it also serves as a working memory for storing intermediate results and computations during program execution. A back-up supply is provided by the charge held in C1 to provide short term data retention while the power is switched off.

13 If, for example, the power is momentarily interrupted, the front panel settings stored in the RAM are recalled when power is restored. The data is checked using a checksum and if it is uncorrupted, it is used as the receiver's operational settings. If the data in the RAM is corrupted, for example, because the supply has been switched off for some time, the data is taken from the EEPROM. A reset pulse generated in the Power Supply Regulator Module at power- up is used to disable the RAM until the supplies reach their rated values, thus avoiding data corruption.

Interface Devices

14 The PROCESSOR is interfaced to other modules in the equipment through the use of PARALLEL I/O INTERFACE TIMER 1. This bidirectional parallel interface provides a module bus for internal communication with all modules connected to it. It consists of an 8-bit address bus, an 8-bit data bus, read/write and strobe control lines, 3 interrupt lines, plus a BITE line for BITE measurements. A programmable event timer is also contained in this device for timing periodic events such as servicing the front panel shaft encoder or push buttons or updating the displays.

15 A second bidirectional parallel interface, PARALLEL I/O INTERFACE TIMER 2, mainly interfaces signals for the rear panel PARALLEL I/O 25-way connector (SK1) to allow the connection of external equipment. It is also used to read the status of seven DIL TEST SWITCHES. As before, a programmable timer is contained in this device. This acts as a 'watchdog timer' which applies a hardware reset unless it is serviced by the software at defined regular intervals

16 Parallel data is also latched from the DATA BUS by DATA LATCH 1 and presented via OUTPUT DRIVERS as control signals for external equipment connected to SK1.

17 Interfacing with remotely-controlled equipment is performed by two SERIAL I/O INTERFACE ports conforming to Standard RS423-A and V10. Each port consists of an Enhanced Programmable Communication Interface (EPCI) operating as a universal asynchronous data communication controller. It is driven by an external 4.9152 MHz OSCILLATOR which it divides to provide the baud rate clock. The EPCI converts the parallel information on its 8-bit DATA BUS input into a serial data stream and vice-versa. Two data control (handshake) lines (CTS and RTS) are also provided to synchronise data transfer with equipments, such as modems.

18 The two ports, termed Master and Tributary, are routed via separate DUAL DIFFERENTIAL DRIVERS AND RECEIVERS to a common 25-way REMOTE connector (PL2) on the rear panel. Connections are made according to the application. For example, a basic RS423-A configuration for each port consists of a data output line, a data input line and a common line for each data line.

19 All serial link parameters can be programmed either locally from the front panel, via the menu system, or externally from a remote (controlling) equipment. To perform the latter method, the CONFIG pin on the REMOTE connector (PL2) must be grounded. This is taken as an input to PI/T 2. Serial data with default parameters can then be received from the controller at a pre-defined baud rate by the Master and Tributary ports in turn, thereby allowing communication to be established. The programmed serial link parameters are then adopted once the CONFIG pin is released. Details of remote control operation are contained in Chapter 5 of the RA3700 Series Operators Manual. Chapter 6 of the Operators Manual gives pin connections and typical system configurations. Details of programming the remote interface for operation with computer controlled systems are provided in Chapter 5 of this maintenance manual.

20 Three analogue control lines are derived by the digital to analogue conversion of parallel data presented to DAC 1 and DAC 2. Each DAC has a latched 8-bit digital input and an output range between 0 and 2.55 V in 10 mV steps. The DAC outputs are buffered by voltage followers.

21 The DAC 1 output is used for BITE metering while the DAC 2 output is used for setting the manual gain level. The DAC 3 output is derived from the DAC 1 output, which is strobed through a DAC 3 SAMPLE AND HOLD CIRCUIT by bit 3 of port B of PI/T 2 to provide a periodic refresh. The DAC 3 output is only used in the dual receiver versions to provide the manual gain setting for the second receiver.

22 Two internal interrupt lines (IPL0 and IPL1) are also provided on the Processor Module. The IPL1 line has the higher priority and is connected to the EPCI devices. The IPL0 line is connected to both PI/T devices and deals with general purpose timer interrupts and external interrupts from the scan inhibit inputs at the PARALLEL I/O connector.

Test Facilities

23 The seven DIL TEST SWITCHES provide access to various test facilities including manually initiated BITE tests and signature analysis. According to the desired operating mode, the switches are set to the positions shown in Table 10.1 and their status read via PI/T 2 at power-up.

TABLE 10.1

Test Switch Positions

Function Selected	Switch No.			
	5	6	7	8
Normal Operation	ON	ON	ON	ON
Receiver Default Set-up	OFF	ON	ON	ON
Unit Confidence Test	ON	OFF	ON	ON
Signature Analysis	ON *	ON *	OFF	ON
Processor Free-Run (Signature Analysis)	OFF	OFF	OFF	OFF

* Dependent on selected signature analysis routine

24 On a slave receiver (RA3703/RA3704) the DIL TEST SWITCHES allow the unit confidence test to be run locally. This facility may also be used on a receiver where a fault prevents the unit confidence test being run from the front panel via the menu system.

25 The DIL TEST SWITCHES also allow the PROCESSOR to operate in a free-run mode. With switch 8 set to OFF, the PROCESSOR data bus is isolated from the rest of the circuit and a test data word is injected into the PROCESSOR causing it to execute a one-word instruction. This instruction is continually stepped through the entire address range to create a repetitive data pattern and allow signature analysis to be performed on the Processor and associated circuitry within the Processor Module.

26 Normally in the initial power-up mode, switches 1 to 4 have no significance. However if signature analysis has been entered, switches 1 to 7 are then used to enter and execute the various signature analysis routines stored in the EPROM. In addition to checking the Processor Module, these routines check the module bus on the motherboard and the digital circuitry of any other module connected to it. Further details of signature analysis are contained in Chapter 3.

27 A 3-digit, 7-segment LED DISPLAY is used for test purposes. It is driven by parallel data latched into DATA LATCH 2 and controlled by three lines taken from the data output of DATA LATCH 1. The display is primarily used to show BITE test faults as some faults may prevent the front panel displays from being used. If a failure occurs the LED DISPLAY flashes its BITE test number.

BITE Measurement System

28 The BITE Measurement System enables the PROCESSOR to measure the supply voltages and check the analogue outputs of DAC 2 and DAC 3 by comparing them with the output of DAC 1.

29 It comprises of an ANALOGUE MULTIPLEXER operating in conjunction with a BITE COMPARATOR. The voltage to be measured is selected by the ANALOGUE MULTIPLEXER which is controlled by three lines taken from Port C of PI/T 1. This selected voltage is then compared in the BITE COMPARATOR with a test voltage established on the DAC 1 line. The resulting output is read by the PROCESSOR via PI/T 1.

30 To enable BITE measurements to be performed in the other modules of the receiver, the DAC 1 line is taken to a BITE comparator in each of these modules. All comparator outputs are connected to an open- collector BITE return line whose status is also read by the PROCESSOR via PI/T 1.

SOFTWARE PROGRAM IDENTIFICATION

31 Using the menu system, the issue of the software program residing in the EPROM may be identified as follows:

(1) Press MENU until the following level 6 options are presented on the right-hand display:

BW	SERIAL PORTS	FREQ RES	S/W ID

(2) Press M4 to select the S/W ID option and the security code prompt appears.

(3) Enter the receiver security code and the following menu is presented:

SERIAL NUMBER	S/W ISSUE

(4) Press M3 to select S/W ISSUE and display the software issue number.

(5) Press M4 to exit back to level 6 options or press RCL to revert back to the receiver operating conditions.

RECEIVER SERIAL NUMBER IDENTIFICATION

32 Using the menu system, the serial number of the receiver is programmed into the EPROM so that it may be identified from the front panel. This facility would be of use in a rack-mounted receiver where the internally-mounted serial number plate is not visible. In the event of the Processor Module being replaced, this facility allows the serial number to be re-entered into the new module. The procedure is as follows:

(1) Carry out the previous procedure for identifying the software issue until the following menu is presented:

SERIAL NUMBER S/W ISSUE

(2) Press M1 to select the SERIAL NUMBER option and the current serial number, if any, is displayed.

(3) Key in the receiver serial number required and press ENTER. The display reverts back to the level 6 options.

(4) Press RCL to revert back to the receiver operating conditions.

FAULT FINDING

General

33 Fault finding techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the Processor Module is contained in the following sections.

BITE Tests

34 The following BITE tests for the Processor Module are arranged in the order in which they are performed or presented for selection.

TEST NUMBER	:	001
TITLE	:	Checksum PD1
PERFORMED	:	Power-up
DESCRIPTION	:	Performs a 16-bit checksum on the EPROM fitted to the PD1 position on the Processor Module. PD1 is indicated as being faulty if the result does not agree with the expected checksum.
FAULT DIRECTORY	:	Fault No. 5

TEST NUMBER	:	002
TITLE	:	Checksum PD2
PERFORMED	:	Power-up
DESCRIPTION	:	As previous BITE test but checks the EPROM fitted to the PD2 position.
FAULT DIRECTORY	:	Fault No. 5

TEST NUMBER	:	003
TITLE	:	RAM test ML17
PERFORMED	:	Power-up
DESCRIPTION	:	Checks the RAM fitted to position ML17 on the Processor Module by writing and reading the following data patterns into the first 32K bytes: all 0's all 1's, walking 0's walking 1's and (except at power-up) a test of the independence of the address lines.
FAULT DIRECTORY	:	Fault No. 5

TEST NUMBER	:	004
TITLE	:	RAM test ML15
PERFORMED	:	Power-up
DESCRIPTION	:	As previous BITE test but checks the RAM fitted to the ML15 position, which provides the second 32K bytes.
FAULT DIRECTORY	:	Fault No. 5

TEST NUMBER	:	005
TITLE	:	EEPROM test
PERFORMED	:	Power-up
DESCRIPTION	:	Checks the data residing in the EEPROM at power-up against the corresponding checksums. A failure to program the EEPROM during normal operation also causes the test number to be displayed on the Processor Module displays.
FAULT DIRECTORY	:	Fault No. 8

TEST NUMBER : 006, 007, 008, 009, 010

TITLE : +5V rail, +15V rail, -15V rail, +24V rail, -5V rail.

PERFORMED : Power-up, unit confidence test, select test.

DESCRIPTION : The appropriate power supply test voltage is selected at the Processor Module and checked.

LIMITS :

Test No.	Supply	Mux I/P	Mux Limits	
			Lower	Upper
006	+5 V	X2	1.78 V	2.22 V
007	+15 V	X4	1.70 V	2.21 V
008	-15 V	X7	1.65 V	2.24 V
009	+24 V	X5	1.73 V	2.45 V
010	-5 V	X6	1.44 V	2.31 V

FAULT DIRECTORY : Fault No. 7

TEST NUMBER : 011

TITLE : DAC test

PERFORMED : Power-up, unit confidence test, select test.

DESCRIPTION : This test checks that the DAC 1 (BITE measurement system) and DAC 2 (IF gain) analogue outputs track to 1 bit across their operating ranges.

FAULT DIRECTORY : Fault No. 10

TEST NUMBER : 012

TITLE : Processor I/O

PERFORMED : Select test.

DESCRIPTION : This test causes the 4-bit antenna output on SK1 and the DAC 1 and DAC 2 outputs to ramp continuously, thus exercising every value. The test will always pass as it is intended for fault finding with the use of additional test equipment.

TEST NUMBER	:	013
TITLE	:	Parallel I/O 1
PERFORMED	:	Select test.
DESCRIPTION	:	The test partially checks the parallel I/O signal lines to the 25-way connector (SK1) on the Processor Module. It requires the use of the external parallel loopback 1 connector to interconnect the following: ANT 0 to AUX 0 ANT 1 to AUX 1 ANT 2 to AUX 2 ANT 3 to AUX 3 COR 1 to MUTE 1 All combinations of bits are tested to ensure that all lines can be driven and read correctly without any crosstalk.
FAULT DIRECTORY	:	Fault No. 12

TEST NUMBER	:	013
TITLE	:	Parallel I/O 2
PERFORMED	:	Select test.
DESCRIPTION	:	Similar to previous test but checks the remainder of the parallel I/O signal lines to SK1 using the parallel loopback 2 connector to interconnect the following: ANT 0 to SCAN INHIBIT 1 ANT 1 to SCAN INHIBIT 2 ANT 2 to DUMP 1 ANT 3 to DUMP 2 COR 2 to MUTE 2
FAULT DIRECTORY	:	Fault No. 12

TEST NUMBER	:	051
TITLE	:	Master port INT.
PERFORMED	:	Select test.
DESCRIPTION	:	Performs an internal loopback test on the Master port using a test pattern consisting of all characters that may be transmitted. Checks that the transmitted pattern is read back correctly.
FAULT DIRECTORY	:	Fault No. 11

TEST NUMBER	:	052
TITLE	:	Master port EXT.
PERFORMED	:	Select test.
DESCRIPTION	:	This test is similiar to test 051 but the internal loopback mode is not used. It requires the use of the external serial loopback connector to interconnect the following: Data output to data input. CTR/RTS to CTS. Receive common to Transmit common. (All connections refer to Master port pins).
FAULT DIRECTORY :		Fault No. 11

TEST NUMBER	:	053
TITLE	:	Trib. port INT.
PERFORMED	:	Select test.
DESCRIPTION	:	As test 051, but for the Tributary port.
FAULT DIRECTORY	:	Fault No. 11

TEST NUMBER	:	054
TITLE	:	Trib. port INT.
PERFORMED	:	Select test.
DESCRIPTION	:	As test 052, but for the Tributary port. (All connections refer to Tributary port pins).
FAULT DIRECTORY	:	Fault No. 11

TEST NUMBER	:	101
TITLE	:	RX data bus.
PERFORMED	:	Power-up.
DESCRIPTION	:	Checks that the parallel interface (PI/T 1) to the receiver modules can drive the data bus. A walking '1' pattern is placed on the data bus and read back into the PI/T such that instantaneous levels are obtained. Short circuits on the data bus are detected by this method.
FAULT DIRECTORY	:	Fault No. 2

TEST NUMBER	:	102
TITLE	:	RX address bus.
PERFORMED	:	Power-up.
DESCRIPTION	:	Checks the receiver address bus as in test 101.
FAULT DIRECTORY	:	Fault No. 2

TEST NUMBER	:	103
TITLE	:	RX bus control.
PERFORMED	:	Power-up.
DESCRIPTION	:	Checks the signals used to control the flow of data on the RX bus. The RX bus strobe line is checked by reading it at the RX bus R/W line and vice versa.
FAULT DIRECTORY	:	Fault No. 2

TEST NUMBER	:	104
TITLE	:	RX BITE line.
PERFORMED	:	Power-up.
DESCRIPTION	:	Checks that no module's BITE circuit asserts the BITE line when their multiplexers are all deselected. DAC1 line is set to 160 mV to allow even a low voltage at a module's multiplexer output to be detected.
FAULT DIRECTORY	:	Fault No. 4

Fault Directory

35 Use the following fault directory to identify the fault condition and take the necessary corrective action. The Processor Module relies heavily on signature analysis as a means of tracing faults to component level. Note that all inputs to the module are assumed to be correct, including the power supplies.

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
1	No response to any control setting, displays blank, and no number displayed on Processor Module LED's	(a) Master clock inoperative.	(a) Check TP2 for 8 MHz. square wave (CMOS levels).
		(b) Reset permanently activated.	(b) Check status of Processor reset line.
		(c) Processor, address decode or address bus fault.	(c) Check supplies to Processor and carry out free-run signature analysis routine.
		(d) Data bus or EPROM fault.	(d) Carry out signature analysis routine 0.
2	As above but LED's display a number (see Table 3.1 , Chap.3).	Module bus parallel I/O interface faulty.	Use signature analysis routine 3 to locate fault around PI/T 1.
3	Unable to update displayed operational settings.	(a) Parallel I/O event timer or processor interrupts faulty.	(a) Use signature analysis routine 5 to locate fault.
		(b) Faulty RAM.	(b) See Fault No. 1.
		(c) Faulty EPROM.	(c) See Fault No. 5.
4	Receiver responds to controls but BITE indicates multiple faults.	(a) BITE hardware fault.	(a) Check action of BITE comparator/ multiplexer using signature analysis routine 4.
		(b) DAC 1 inoperative.	(b) See Fault No. 11.
5	Incorrect response to control settings.	(a) EPROM faulty.	(a) Select BITE tests 001 and 002 to confirm whether PD1 or PD2 is faulty.
		(b) Faulty PI/T 1.	(b) See Fault No. 2.
		(c) RAM faulty.	(c) Check ML15 and ML17 using BITE tests 003 and 004. Use signature analysis routine 0.
6	No indication on Processor Module LEDs but receiver appears to operate normally.	LED display or data latches faulty.	Use signature analysis routine 6 to locate fault.
7	Power supply rails fail BITE test (Power Supply Regulator Module assumed serviceable).	BITE hardware fault.	Check inputs to analogue multiplexer and refer to Fault No. 4.
8	Unable to program channels or retain operating settings when receiver is switched off for a long period.	EEPROM or address decode faulty.	Check ML6 using BITE test 005 and signature analysis routine 2.
9	If power is momentarily interrupted, changes to operating settings made within the last minute are not stored.	(a) RAM back-up supply faulty.	(a) Check C1 is being charged via TR8.
		(b)RAM faulty.	(b) Check ML15 and ML17 using BITE tests 003 and 004. Use signature analysis routine 0.
10	No manual gain control.	DAC 2 inoperative.	Select BITE test 012 and check for a sawtooth waveform of between 0 V and 2.55 V on DAC output. Use signature analysis routine 4 to check digital inputs.

Fault Directory (continued)

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
11	No remote control.	Serial I/O interface faulty.	Select BITE tests 051 to 054 to check both ports. If both ports faulty, check baud rate clock on TP7 and -5 V supply from ML1. Carry out signature analysis routine 6 using serial loopback connector.
12	No response to one or more signal I/O connections to SK1 (parallel I/O).	Parallel I/O interface (PI/T 2) faulty.	Select BITE tests 013 and 014 to check all I/O lines. Check chip enable on TP4.
13	No response to scan inhibit inputs.	(a) Parallel I/O interface faulty (b) Processor interrupts absent.	(a) See Fault No. 12. (b) Use signature analysis routine 6 to check SCAN INHIBIT inputs.

Signature Analsysis Routines

ROUTINE FREE RUN

36 This routine checks the fundamental operation of the Processor,address bus and address decoding.

Processor Module DIL switch settings: SW8 OFF
SW1-7 ON

Signature Analyser connection and settings:

Start : A23 (ML2/52) Processor Module, negative trigger
Stop : A23 (ML2/52) Processor Module, negative trigger
Clock : TP2 Processor Module, positive trigger
Earth: TP1 Processor Module

Note : Signatures xxxxF signify a flashing probe indicator.

Signal	Signature	Test Node						Remarks
+5V	5382	ML2/49	ML2/14					
0V	0000	TP1	ML2/16	ML2/53				
CLK	0000F	XL1/8	LK2/1	LK2/2	ML16/4	ML19/2		
AS	0C7H	ML2/6	TP6	ML16/6	ML29/4	ML27/1		
UDS	0C7H	ML2/7	ML27/10	ML18/9				
LDS	0C7H	ML2/8	ML27/4	ML18/1	ML18/13			
R/(W)	5382	ML2/9	ML16/17	ML18/5	ML5/43	ML31/1	ML30/1	
		ML3/43	ML18/12	ML18/10				
(R)/W	0000	ML16/3	ML8/13	ML7/13	PD1/20	PD2/20	ML6/22	
		ML15/22	ML17/22					

Signature Analysis Routines (continued)

Signal	Signature	Test Node						Remarks
RESET	5382	ML14/8	ML16/15	ML19/1	ML2/18	ML2/17	ML3/39	
IPL0	5382	ML26/8	ML2/25					
IPL1	5382	ML8/14	ML8/15	ML7/14	ML7/15	ML26/11	ML2/24	
FC0	0000	ML2/28	ML26/1					
FC1	5382	ML2/27	ML26/2					
FC2	5382	ML2/26	ML26/13					
ML26/12	5382	ML26/12	ML29/6	ML27/2				
VPA	5382	ML27/3	ML2/21	ML19/7				
A1	FA19	ML2/29	ML7/12	ML8/12	ML5/29	ML15/10	ML17/10	
		ML3/29	PD2/21	ML6/10	PD1/21			
A2	U7UU	ML2/30	ML7/10	ML8/10	ML5/28	ML15/9	ML17/9	
		ML3/28	PD2/22	PD1/22	ML6/9			
A3	P8AC	ML2/31	ML5/27	ML15/8	ML17/8	ML6/8	ML3/27	
		PD1/23	PD2/23					
A4	17CF	ML2/32	ML5/26	ML15/7	ML17/7	ML6/7	ML3/26	
		PD1/24	PD2/24					
A5	IP81	ML2/33	ML5/25	ML15/6	ML17/6	ML6/6	ML3/25	
		PD1/25	PD2/25					
A6	FU6C	ML2/34	ML15/5	ML17/5	ML6/5	PD1/26	PD2/26	
A7	7668	ML2/35	ML15/4	ML17/4	ML6/4	PD1/27	PD2/27	
A8	76U2	ML2/36	ML15/3	ML17/3	ML6/3	PD1/28	PD2/28	
A9	F35C	ML2/37	ML15/25	ML17/25	ML6/25	PD1/29	PD2/29	
A10	A35A	ML2/38	ML15/24	ML17/24	ML6/24	PD1/31	PD2/31	
A11	C0C7	ML2/39	ML15/21	ML17/21	ML6/21	PD1/32	PD2/32	
A12	0317	ML2/40	ML15/23	ML17/23	ML6/23	PD1/33	PD2/33	
A13	4951	ML2/41	ML15/2	ML17/2	ML6/2	PD1/34	PD2/34	
A14	24H8	ML2/42	ML15/26	ML17/26	ML6/26	PD1/35	PD2/35	
A15	C0CC	ML2/43	ML15/1	ML17/1	PD1/36	PD2/36		
A16	FF7P	ML2/44	PD1/37	PD2/37				
A17	FA19	ML2/45	PD1/38	PD2/38				
A18	U7UU	ML2/46	ML23/2	ML23/14				
A19	P8AC	ML2/47	ML23/3	ML23/13				
A20	17CF	ML2/48	ML29/1					
A21	1P81	ML2/50	ML29/2					
A22	FU6C	ML2/51	ML29/3					
A23	7668	ML2/52	ML19/3					
DTACK	F951	ML16/12	ML2/10					
ML16/14	58UU	ML16/14	ML19/9					
RAM R/(W)	5382	ML18/11	ML15/27					
RAM (R)/W	5382	ML18/8	ML17/27					
E^2 R/W	5382	ML18/3	ML6/27					
PD1 CE	P291	ML29/15	PD1/2					
PD2 CE	9PHC	ML29/14	PD2/2					
E^2 CE	C5CA	ML29/13	ML6/20					
RAM CE	A2C4	ML29/12	ML25/1	ML25/2	ML15/20	ML17/20		
ML29/11	22AU	ML29/11	ML27/5	ML27/9				
ML27/6	22AU	ML27/6	ML23/1					
ML27/8	22AU	ML27/8	ML23/15					
A	3FC2	ML23/4	TP4	ML5/41				
B	HC90	ML23/5	ML8/11					
C	7H83	ML23/6	ML28/11					
D	PC8F	ML23/7	ML24/4					
E	3FC2	ML23/12	ML3/41					
F	HC90	ML23/11	ML7/11					
G	7H83	ML23/10	ML12/11					
H	PC8F	ML23/9	ML21/4					

Signature Analysis Routines (continued)

ROUTINE 0

37 This routine checks the RAM and the data read into the Processor via the Data Buffer.

Processor Module DIL switch settings: SW7 OFF
SW1-6,8 ON

Signature Analyser connection and settings:

Start: TP4 Processor Module, negative trigger
Stop: TP4 Processor Module, negative trigger
Clock: TP6 Processor Module, positive trigger
Earth: TP1 Processor Module

Note: The gating period is approximately 5 seconds for this test, therefore allow sufficent time for signatures to settle before taking result.

Signal	Signature	Test Node					Remarks
RAM 5V	5883	ML15/28	ML17/28	ML25/14			
RAM 0V	0000	ML15/14	ML17/14				
CE	05PP	ML15/20	ML17/20	ML25/2	ML25/1	ML29/12	
OE	34PF	ML15/22	ML17/22	ML16/3			
WE(L)	6F6U	ML15/27	ML18/11				
WE(U)	6F6U	ML17/27	ML18/3				
DO	836F	ML2/5 PD2/19	ML31/18	ML31/2	ML15/11	PD1/19	
D1	515A	ML2/4	ML31/17	ML31/3	ML15/12		
D2	A976	ML2/3	ML31/16	ML31/4	ML15/13		
D3	C0A6	ML2/2	ML31/15	ML31/5	ML15/15		
D4	P381	ML2/1	ML31/14	ML31/6	ML15/16		
D5	1C09	ML2/64	ML31/13	ML31/7	ML15/17		
D6	580P	ML2/63	ML31/12	ML31/8	ML15/18		
D7	65U8	ML2/62	ML31/11	ML31/9	ML15/19		
D8	HP96	ML2/61	ML30/18	ML30/2	ML17/11		
D9	9HOF	ML2/60	ML30/17	ML30/3	ML17/12		
D10	U42A	ML2/59	ML30/16	ML30/4	ML17/13		
D11	1FC2	ML2/58	ML30/15	ML30/5	ML17/15		
D12	PCFC	ML2/57	ML30/14	ML30/6	ML17/16		
D13	P371	ML2/56	ML30/13	ML30/7	ML17/17		
D14	H253	ML2/55	ML30/12	ML30/8	ML17/18		
D15	4712	ML2/54	ML30/11	ML30/9	ML17/19		

Signature Analysis Routines (continued)

ROUTINE 1

38 This routine checks the LED Display and associated data latches.

Processor Module DIL switch settings: SW7,1 OFF
SW2-6,8 ON

Signature Analyser connection and settings:

Start: TP4 Processor Module, negative trigger
Stop: TP4 Processor Module, negative trigger
Clock: TP6 Processor Module, positive trigger
Earth: TP1 Processor Module

Signal	Signature	Test Node				Remarks
+5V	63A3	ML28/20	ML12/20			
OE/OV	0000	ML28/1	ML28/10	ML12/1	ML12/10	
LDS	5P5H	ML2/8	ML27/4			
ML27/6	C213	ML27/6	ML23/1			
C	P061	ML23/6	ML28/11			
G	3HUP	ML23/10	ML12/11			
UDS	H1C0	ML2/9	ML27/10			
ML27/8	3HUP	ML27/8	ML23/15			
a	U10P	ML28/2	R64			
b	6825	ML28/5	R61			
c	96P3	ML28/6	R60			
d	9F9U	ML28/9	R58			
e	5P42	ML28/12	R65			
f	4P8U	ML28/15	R63			
g	53F0	ML28/16	R59			
dp	5139	ML28/19	R57			
C3	U314	ML12/15	ML4/1			
C2	89FU	ML12/16	ML4/4			
C1	7AHC	ML12/19	ML4/11			

ROUTINE 2

39 This routine checks the EEPROM.

WARNING:The contents of the EEPROM will be corrupted when this routine is run.

Processor Module DIL switch settings: SW7,2 OFF
SW1,3-6,8 ON

Signature Analyser connection and settings:

Start: TP4 Processor Module, negative trigger
Stop: TP4 Processor Module, negative trigger
Clock: TP6 Processor Module, positive trigger
Earth: TP1 Processor Module

Signal	Signature	Test Node	Remarks
+5V	481P	ML6/28	
0V	0000	ML6/14	
CE	2P2F	ML29/13 ML6/20	
DO	HP27	ML6/11	
D1	8PP4	ML6/12	
D2	8A11	ML6/13	
D3	159F	ML6/15	
D4	U49U	ML6/16	
D5	1354	ML6/17	
D6	3UH2	ML6/18	
D7	85FH	ML6/19	

ROUTINE 3

40 This routine checks that the Processor can communicate with the receiver module bus via PI/T.

Processor Module DIL switch settings: SW7,1,2 OFF
SW3-6,8 ON

Signature Analyser connection and settings:

Start: TP4 Processor Module, negative trigger
Stop: TP4 Processor Module, negative trigger
Clock: TP6 Processor Module, positive trigger
Earth: TP1 Processor Module

Signal	Signature	Test Node		Remarks
+5V	5HHC	ML3/12		
0V	0000	ML3/38		
CE	U61P	ML23/12	ML3/41	
RESET	5HHC	ML3/39		
R/W	936A	ML3/43		
PIRQ	5HHC	ML3/35	ML3/33	
D8	07A7	ML3/44		
D9	7H75	ML3/45		
D10	4697	ML3/46		
D11	P3U0	ML3/47		
D12	49C9	ML3/48		
D13	323P	ML3/1		
D14	2952	ML3/2		
D15	14AP	ML3/3		
A1	1P3H	ML3/29		
A2	H0UO	ML3/28		
A3	07UF	ML3/27		
A4	7P56	ML3/26		
A5	P04H	ML3/25		
PC1	314F	ML3/31	ML16/11	
PC2	P0C2	ML3/30	ML16/13	
PC4	3UPP	ML3/34		
PC6	P9UU	ML3/36		
PC7	28H4	ML3/37		
M-WR	C224	ML16/9	PL1/8B	
M-STB	H905	ML16/7	PL1/8A	
M-A0	019H	ML3/4	PL1/12A	
M-A1	A3C9	ML3/5	PL1/12B	
M-A2	UPA8	ML3/6	PL1/11A	
M-A3	UF40	ML3/7	PL1/11B	
M-A4	C6FF	ML3/8	PL1/10A	
M-A5	1757	ML3/9	PL1/10B	
M-A6	4C0U	ML3/10	PL1/9A	
M-A7	1783	ML3/11	PL1/9B	
M-D0	19AU	ML3/17	PL1/7A	
M-D1	P22C	ML3/18	PL1/7B	
M-D2	6HU7	ML3/19	PL1/6A	
M-D3	91H3	ML3/20	PL1/6B	
M-D4	P668	ML3/21	PL1/5A	
M-D5	AP85	ML3/22	PL1/5B	
M-D6	HUF8	ML3/23	PL1/4A	
M-D7	3HAP	ML3/24	PL1/4B	

Signature Analysis Routines (continued)

ROUTINE 4

41 This routine checks the data lines to the DACs and EPCIs.

Processor Module DIL switch settings: SW7,3 OFF
SW1,2,4-6,8 ON

Signature Analyser connection and settings:

Start: TP4 Processor Module, negative trigger
Stop: TP4 Processor Module, negative trigger
Clock: TP6 Processor Module, positive trigger
Earth: TP1 Processor Module

Signal	Signature	Test Node				Remarks
+5V	PU58	ML21/10	ML24/10	ML7/26	ML8/26	
0V	0000	ML21/9	ML24/9			
D0	HA74	ML24/2	ML8/27			
D1	P039	ML24/1	ML8/28			
D2	1H74	ML24/16	ML8/1			
D3	H117	ML24/15	ML8/2			
D4	P92C	ML24/14	ML8/5			
D5	CP7H	ML24/13	ML8/6			
D6	PHF5	ML24/12	ML8/7			
D7	3185	ML24/11	ML8/8			
D8	U867	ML21/2	ML7/27			
D9	90H4	ML21/1	ML7/28			
D10	2567	ML21/16	ML7/1			
D11	9C26	ML21/15	ML7/2			
D12	6HU0	ML21/14	ML7/5			
D13	9432	ML21/13	ML7/6			
D14	2UPP	ML21/12	ML7/7			
D15	H9UU	ML21/11	ML7/8			

Signature Analysis Routines (continued)

ROUTINE 5

42 This routine checks PI/T 2 watchdog timer/reset and the PI/T 1 event timer.

Processor Module DIL switch settings: SW7,1,3 OFF
SW2,4-6,8 ON

Signature Analyser connection and settings:

Start: ML2/17, Processor Module, negative trigger
Stop: ML2/18, Processor Module, negative trigger
Clock: TP6 Processor Module, positive trigger
Earth: TP1 Processor Module

Signal	Signature	Test Node						Remarks
+5V	A544	ML5/12						
0V	0000	ML5/30						
D0	P11C	ML5/44	ML31/2					
D1	P0H2	ML5/45	ML31/3					
D2	CF20	ML5/46	ML31/4					
D3	4654	ML5/47	ML31/5					
D4	F0H8	ML5/48	ML31/6					
D5	9H63	ML5/1	ML31/7					
D6	5C08	ML5/2	ML31/8					
D7	FF71	ML5/3	ML31/9					
A1	U88A	ML5/29	ML2/29					
A2	24UA	ML5/28	ML2/30					
A3	730C	ML5/27	ML2/31					
A4	4FAF	ML5/26	ML2/32					
A5	4A70	ML5/25	ML2/33					
IPLO(PIT)	2FP3	ML5/35	ML3/33	ML3/35	ML13/11 R36			
ML13/10	89A7	ML13/10	ML26/10					
ML26/9	A544	ML26/9						
IPL1	A544	ML8/14	ML8/15	ML7/14	ML7/15	ML2/24	ML26/11	
IPLO	2FP3	ML26/8	ML2/25					
TOUT	H2A2	ML5/33	ML14/10					
R	H2A2	ML14/8	ML16/15	ML3/39	ML19/1	ML2/18	ML2/17	
SA1	A544	ML5/4						
SA2	0000	ML5/5						
SA3	A544	ML5/6						
SA4	0000	ML5/7						
SA5	0000	ML5/8						
SA6	0000	ML5/9						
SA7	A544	ML5/1						

Signature Analysis Routines (continued)

ROUTINE 6

43 This routine checks the Processor parallel I/O data latch.

Processor Module DIL switch settings: SW7,3,2 OFF
SW1,4,5,6,8 ON

Signature Analyser connection and settings:

Start: ML3/41 Processor Module, negative trigger
Stop: ML3/41 Processor Module, negative trigger
Clock: TP6 Processor Module, positive trigger
Earth: TP1 Processor Module

Signal	Signature	Test Node	Remarks
+5V	848F	ML5/12	
0V	0000		
ML12/2	465U	ML12/2	
ML12/5	PUPC	ML12/5	
ML12/6	9HCU	ML12/6	
ML12/9	6A08	ML12/9	
ML12/12	1PUF	ML12/12	

PARTS LIST

44 The Racal part number for a complete serial ASCII Processor Module is ST87707.

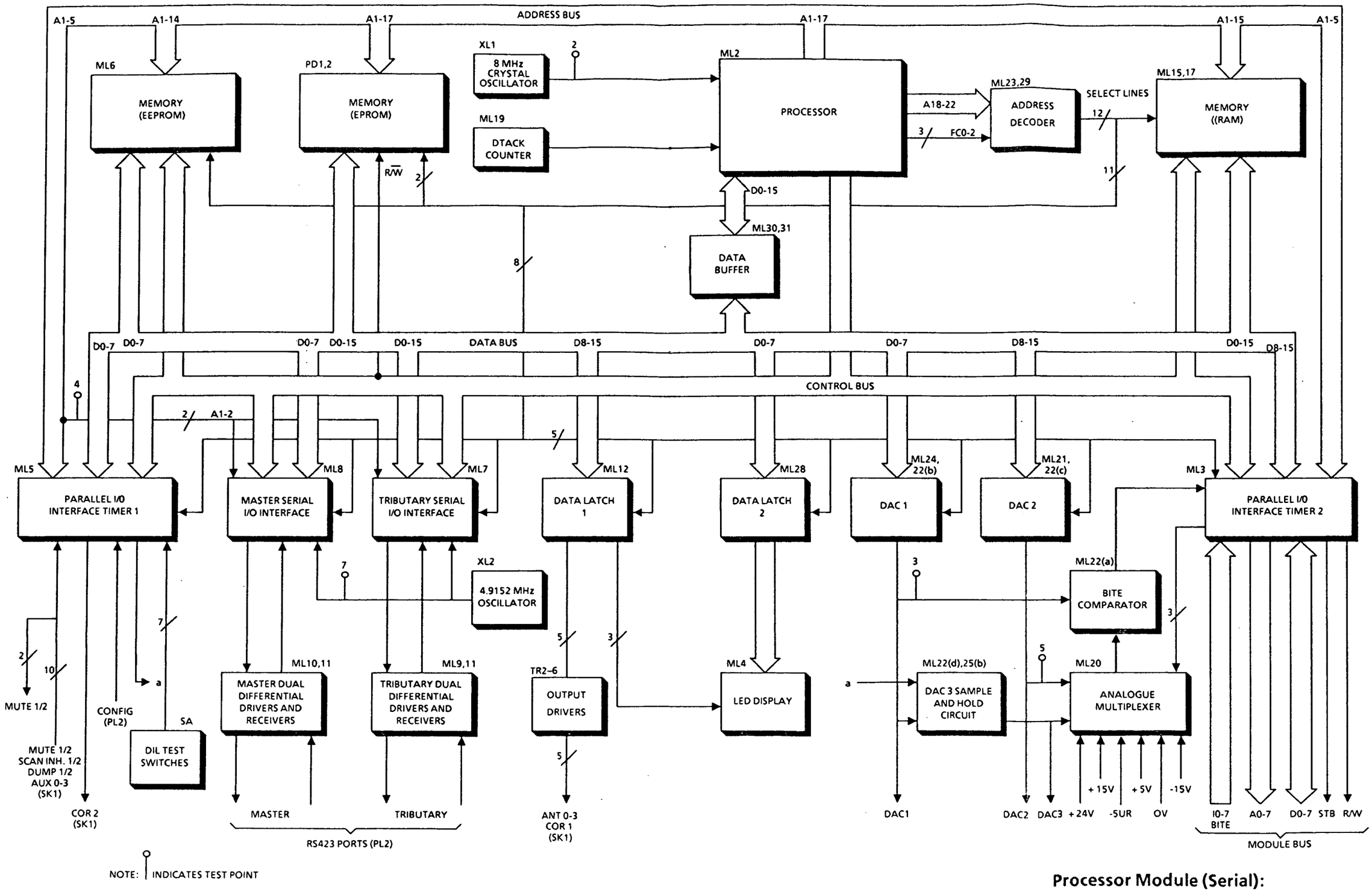
45 Information on the identification and handling of SMDs is provided in Chapter 2. The parts list for the Processor Module is as follows:

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R1		10k	Thick Film Network			934506N	
R2		10k	Thick Film Network			934506N	
R3		10k	Thick Film Network			934506N	
R4		3k3	Thick Film Network			939677T	
R5		10k	Thick Film Network			934506N	
R6		1k	Thick Film Network			940019R	
R7		1k	Thick Film Network			940019R	
R8		47R		0.5	2	918744Z	
R9	C5	270k	Thick Film Chip	0.125	2	943919N	274
R10	C4	2k2	Thick Film Chip	0.125	2	943894R	222
R11	C5	270k	Thick Film Chip	0.125	2	943919N	274
R12	D3	2k2	Thick Film Chip	0.125	2	943894R	222
R13	D3	2k2	Thick Film Chip	0.125	2	943894R	222
R14	D3	2k2	Thick Film Chip	0.125	2	943894R	222
R15	D3	2k2	Thick Film Chip	0.125	2	943894R	222
R16	D2	2k2	Thick Film Chip	0.125	2	943894R	222
R17	D2	2k2	Thick Film Chip	0.125	2	943894R	222
R18	D1	2k2	Thick Film Chip	0.125	2	943894R	222
R19	D1	2k2	Thick Film Chip	0.125	2	943894R	222
R20	D0	2k2	Thick Film Chip	0.125	2	943894R	222
R21	D0	2k2	Thick Film Chip	0.125	2	943894R	222
R22	D4	1k	Thick Film Chip	0.125	2	943890L	102
R23	D4	1k	Thick Film Chip	0.125	2	943890L	102
R24	E4	1k	Thick Film Chip	0.125	2	943890L	102
R25	E4	1k	Thick Film Chip	0.125	2	943890L	102
R26	F0	2k2	Thick Film Chip	0.125	2	943894R	222
R27	F0	2k2	Thick Film Chip	0.125	2	943894R	222
R28	F0	2k2	Thick Film Chip	0.125	2	943894R	222
R29	F0	2k2	Thick Film Chip	0.125	2	943894R	222
R30	F0	2k2	Thick Film Chip	0.125	2	943894R	222
R31	G4	1M	Thick Film Chip	0.125	2	945100R	105
R32	G0	2k2	Thick Film Chip	0.125	2	943894R	222
R33	G4	220R	Thick Film Chip	0.125	2	943882M	221
R34	H1	10k	Thick Film Chip	0.125	2	943902F	103
R35	J1	5k6	Thick Film Chip	0.125	2	943899E	562
R36	J1	5k6	Thick Film Chip	0.125	2	943899E	562
R37	N0	22k	Thick Film Chip	0.125	2	943906B	223
R38	N0	22k	Thick Film Chip	0.125	2	943906B	223
R39	N1	120k	Thick Film Chip	0.125	2	943915R	124
R40	N3	15k	Thick Film Chip	0.125	2	943904D	153
R41	N1	18k	Thick Film Chip	0.125	2	943905K	183
R42	N3	10k	Thick Film Chip	0.125	2	943902F	103
R43	N1	10k	Thick Film Chip	0.125	2	943902F	103
R44	P3	27k	Thick Film Chip	0.125	2	943907S	273
R45	P1	22k	Thick Film Chip	0.125	2	943906B	223
R46	P9	100k	Thick Film Chip	0.125	2	943914A	104
R47	P3	10k	Thick Film Chip	0.125	2	943902F	103
R48	P1	18k	Thick Film Chip	0.125	2	943905K	183
R49	P1	100k	Thick Film Chip	0.125	2	943914A	104
R50	P1	10k	Thick Film Chip	0.125	2	943902F	103
R51	P1	100k	Thick Film Chip	0.125	2	943914A	104
R52	R1	3k3	Thick Film Chip	0.125	2	943896P	332
R53	R2	3k3	Thick Film Chip	0.125	2	943896P	332
R54	R2	3k3	Thick Film Chip	0.125	2	943896P	332
R55	S3	390R	Thick Film Chip	0.125	2	943885B	391
R56	T1	10k	Thick Film Chip	0.125	2	943902F	103
R57	T9	2k2	Thick Film Chip	0.125	2	943894R	222
R58	T8	2k2	Thick Film Chip	0.125	2	943894R	222

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R59	T9	2k2	Thick Film Chip	0.125	2	943894R	222
R60	T8	2k2	Thick Film Chip	0.125	2	943894R	222
R61	V8	2k2	Thick Film Chip	0.125	2	943894R	222
R62	V1	10k	Thick Film Chip	0.125	2	943902F	103
R63	V9	2k2	Thick Film Chip	0.125	2	943894R	222
R64	V8	2k2	Thick Film Chip	0.125	2	943894R	222
R65	V9	2k2	Thick Film Chip	0.125	2	943894R	222
R66	Y3	4k7	Thick Film Chip	0.125	2	943898N	472
R67	Z3	100k	Thick Film Chip	0.125	2	943914A	104
R68	Z3	100k	Thick Film Chip	0.125	2	943914A	104
Capacitors				V			
C1		47m	Electrolytic, Aluminium Tubular	5V5	-20 +80	945002G	
C2	B8	82p	Ceramic Chip	50	5	941798W	
C3	B7	82p	Ceramic Chip	50	5	941798W	
C4	C8	82p	Ceramic Chip	50	5	941798W	
C5	C7	82p	Ceramic Chip	50	5	941798W	
C6	C8	82p	Ceramic Chip	50	5	941798W	
C7	C7	82p	Ceramic Chip	50	5	941798W	
C8	D9	100n	Ceramic Chip	50	20	945146T	
C9	D7	100n	Ceramic Chip	50	20	945146T	
C10	D5	100n	Ceramic Chip	50	20	945146T	
C11	G4	180p	Ceramic Chip	50	5	941802O	
C12	G4	180p	Ceramic Chip	50	5	941802O	
C13	G8	100n	Ceramic Chip	50	20	945146T	
C14	G6	100n	Ceramic Chip	50	20	945146T	
C15	H1	100n	Ceramic Chip	50	20	945146T	
C16	H8	100n	Ceramic Chip	50	20	945146T	
C17	M1	100n	Ceramic Chip	50	20	945146T	
C18	M4	100n	Ceramic Chip	50	20	945146T	
C19	M6	100n	Ceramic Chip	50	20	945146T	
C20	M6	100n	Ceramic Chip	50	20	945146T	
C21	N1	100n	Ceramic Chip	50	20	945146T	
C22	N6	100n	Ceramic Chip	50	20	945146T	
C23	P5	100n	Ceramic Chip	50	20	945146T	
C24	R3	470n	Ceramic Chip	50	20	941767E	
C25	R1	100n	Ceramic Chip	50	20	945146T	
C26	R7	100n	Ceramic Chip	50	20	945146T	
C27	R5	100n	Ceramic Chip	50	20	945146T	
C28	R3	1µ	Tantalum Chip	35	20	945049Z	
C29	X9	100n	Ceramic Chip	50	20	945146T	
C30	X2	100n	Ceramic Chip	50	20	945146T	
C31	X2	100n	Ceramic Chip	50	20	945146T	
C32	Y6	100n	Ceramic Chip	50	20	945146T	
C33	Y2	1µ	Tantalum Chip	35	20	945049Z	
C34	Y0	1µ	Tantalum Chip	35	20	945049Z	
C35	Z5	100n	Ceramic Chip	50	20	945146T	
C36	Z3	33µ	Tantalum Chip	10	20	945054T	
Inductors				W			
L1		150nH	Choke	0.2	10	940392R	
L2		150nH	Choke	0.2	10	940392R	
L3		150nH	Choke	0.2	10	940392R	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Diodes							
D1	C4		BAS 16			943951D	
D2	C3		BAS 16			943951D	
D3	C3		BAS 16			943951D	
D4	C2		BAS 16			943951D	
D5	C1		BAS 16			943951D	
D6	C0		BAS 16			943951D	
D7	D3		BAS 16			943951D	
D8	D3		BAS 16			943951D	
D9	D2		BAS 16			943951D	
D10	D1		BAS 16			943951D	
D11	D0		BAS 16			943951D	
Transistors							
TR1	C3		MMBT2222A NPN			943949Y	
TR2	C3		MMBT2222A NPN			943949Y	
TR3	C2		MMBT2222A NPN			943949Y	
TR4	C1		MMBT2222A NPN			943949Y	
TR5	C0		MMBT2222A NPN			943949Y	
TR6	C0		MMBT2222A NPN			943949Y	
TR7	Z3		MMBT2222A NPN			943949Y	
TR8	Z3		BCX 71J PNP			943950M	
Integrated Circuits		CAUTION: *SSD - STATIC SENSITIVE DEVICES					
ML1			7905, -5V Regulator			945150G	
ML2		*SSD	68000, 16-Bit Microprocessor			945154C	
ML3		*SSD	68230, Parallel Interface Timer			945153L	
ML4			Display, Triple 7-Segment, Red			945175X	
ML5		*SSD	68230, Parallel Interface Timer			945153L	
ML6		*SSD	28C64, 8k x 8-Bit EEPROM			945350Y	
ML7		*SSD	68661, Programmable Communication Interface			943548N	
ML8		*SSD	68661, Programmable Communication Interface			943548N	
ML9			26LS30			938684U	
ML10			26LS30			938684U	
ML11			26LS32, Dual Differential Line Receiver			938683N	
ML12	F2	*SSD	74HC377, D-Type Flip-Flop			943990E	
ML13	G6	*SSD	74HCT04, Hex Inverter			945152E	
ML14	G1		74LS09, Quad 2-Input AND Gate			945155J	
ML15	L8	*SSD	62256, 32k x 8-Bit Static RAM			945471C	
ML16	M1	*SSD	74HCT240, Octal Inverter Buffer			943986B	
ML17	N8	*SSD	62256, 32k x 8-Bit Static RAM			945471C	
ML18	N6	*SSD	74HCT32, Quad 2-Input OR Gate			943976U	
ML19	M4	*SSD	74HCT161, Synchronous 4-Bit Binary Counter			943984T	
ML20	P2	*SSD	4051, 8-Channel Multiplexer			943993J	
ML21	P4		428, 8-Bit D/A Converter			945158Y	
ML22	R2		324, Quad Operational Amplifier			945026G	
ML23	R7	*SSD	74HCT139, 2 to 4 Line Decoder/Demultiplexer			945157R	
ML24	R4		428, 8-Bit D/A Converter			945158Y	
ML25	S2	*SSD	74HC4066, Quad Analogue Switch			945151N	
ML26	T6	*SSD	74HCT10, Triple 3-Input NAND Gate			943973F	
ML27	V6	*SSD	74HCT32, Quad 2-Input OR Gate			943976U	
ML28	W8	*SSD	74HC377, D-Type Flip-Flop			943990E	
ML29	W6	*SSD	74HCT138, 3 to 8 Line Decoder/Latch			943981O	
ML30	X6	*SSD	74HCT245, Octal Bus Transceiver			943988Z	
ML31	Z6	*SSD	74HCT245, Octal Bus Transceiver			943988Z	
PD1		*SSD	27210, 64k x 16-Bit EPROM			945364B	
PD2		*SSD	27210, 64k x 16-Bit EPROM			945364B	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Connectors							
PL1			Plug, 64-Way			940339G	
Switches							
SA			Slide, DIL			945176E	
Miscellaneous							
W1			Cable Assembly			BA87138	
W2			Cable Assembly			BA87157	
LK2			Comprising:				
			Plug, 4-Way			943168X	
			Shorting Link			943684I	
TP1 to TP7			Terminal, Assembly (test points)			936148X	
XL1			Crystal Oscillator 8 MHz			945170K	
XL2			Crystal Oscillator 4.9152 MHz			945174G	



Processor Module (Serial): Block Diagram **Fig 10.2**

CHAPTER 11

FRONT PANEL ASSEMBLY

(RA3701/RA3702/MA3700)

CONTENTS

ILLUSTRATIONS

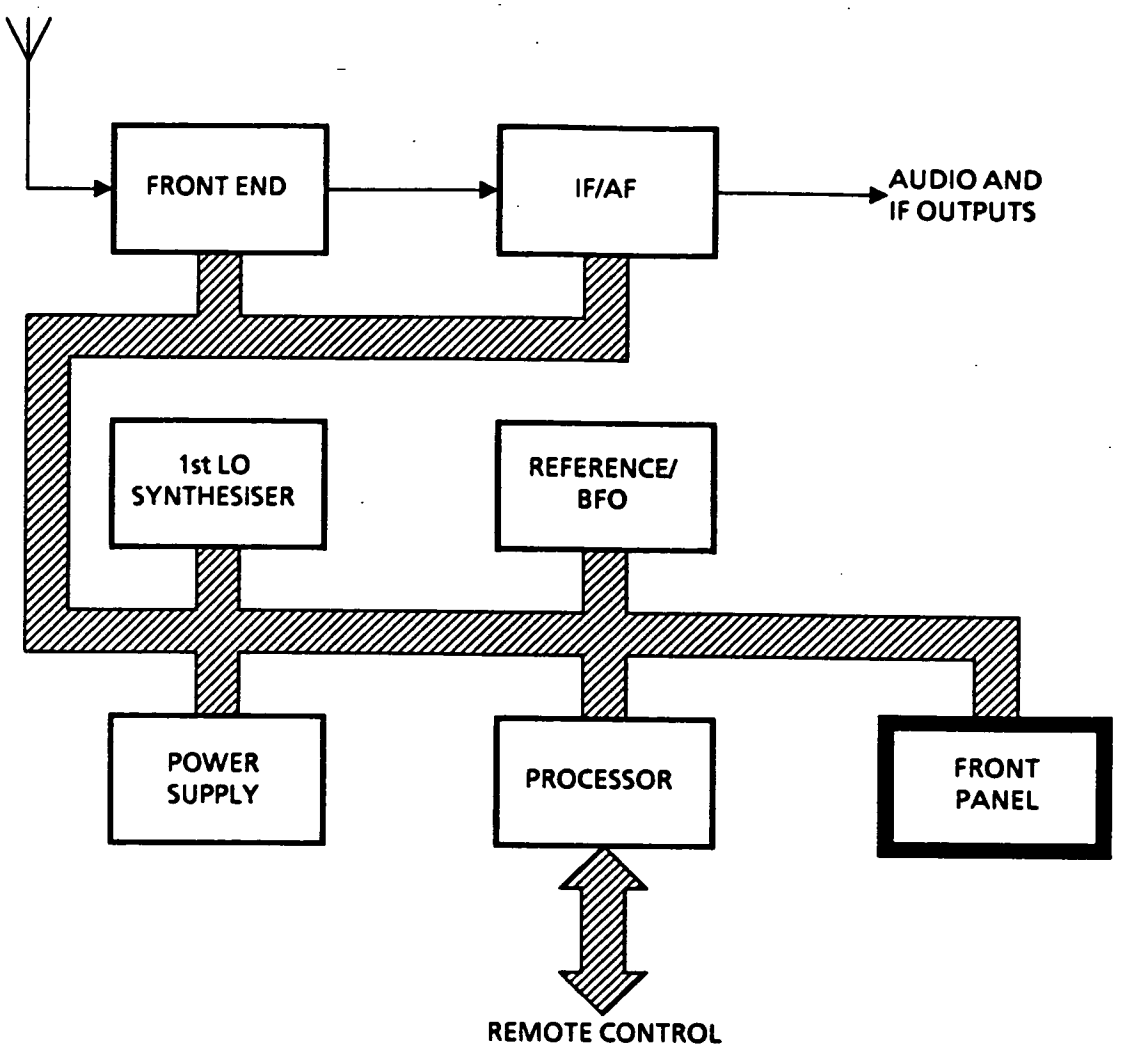


Fig. 11.1 Receiver Block Diagram

CHAPTER 11

FRONT PANEL ASSEMBLY

(RA3701/RA3702/MA3700)

INTRODUCTION

1 The Front Panel Assembly contains all the necessary controls and displays, together with the interfaces to the Processor Module, to allow operator control of the equipment. Audio amplifiers for driving loudspeaker and phone outlets are also provided as well as the means for adjusting the backlighting intensity of the displays. The electronic components are carried on a printed circuit board mounted behind the front panel.

Fig.11.1 Receiver Block Diagram

ASSEMBLY DESCRIPTION

2 The following description should be read in conjunction with the Front Panel Assembly Block and Circuit Diagrams included in this chapter. Component references shown on the Block Diagram allow it to be related to the Circuit Diagram.

Tuning Control

3 The front panel tuning control is mechanically linked to a SHAFT ENCODER comprising a disc with a series of apertures cut out around its circumference. The disc passes through two optical switches, each consisting of a light emitting diode and a photo transistor. As the disc is rotated, the light path through the switch is interrupted, producing a series of pulses at the switch output.

4 The optical switches are physically displaced such that as the disc rotates, two pulse trains are produced which are offset in phase, one leading the other according to the direction of rotation (see Fig. 11.2). An INTERFACE CIRCUIT uses this phase relationship to detect the direction of pulse count and translates the pulses into a form suitable to be read by the Processor via the Module Data Bus.

5 In the INTERFACE CIRCUIT, 100 pulses per revolution of the disc together with up/down information are produced for driving an 8-bit counter. When the Processor requires frequency tuning data it momentarily stops the counters and enables buffer ML16 to read the count value in the counters onto the Module Data Bus.

6 The timing diagrams in Fig. 11.2 illustrate how the INTERFACE CIRCUIT produces the clock and up/down inputs for the counters for both clockwise and anticlockwise rotation of the SHAFT ENCODER.

7 ML7(a) and (b), R48 and C28 generate a clock pulse for a change in state of either pulse waveform from the optical switches and this is used to clock both latch ML14(b) and the counters. The D input to the latch is subjected to the same time delay as the clock to ensure the correct logic level is latched for its corresponding clock pulse.

8 The output waveform of ML14(b) is dependent upon the direction of rotation of the SHAFT ENCODER. From the timing diagrams it can be seen that the waveform is identical to that of one optical switch output (at ML7(b)) for an anticlockwise rotation and the inverse for a clockwise rotation. When either of the two waveforms from the latch is exclusive ORed with the output of ML7(b), the result is a steady low for an anticlockwise rotation and a steady high for a clockwise rotation.

Switch Interface

9 The push button switches on the front panel are connected as a six- row (X) by eight-column (Y) SWITCH MATRIX to enable the closure of any switch to be detected. In response to select data on the Module Address Bus from the Processor, a ROW SELECT DECODER causes a 0 V signal to be applied, in turn, to each row line. A depressed push button routes this 0 V signal via one of eight return lines into a SWITCH SELECT BUFFER to be read out onto the Module Data Bus when selected by the ADDRESS DECODER. Hence, a coded output is returned to the Processor to indicate which switch is pressed. Coded outputs resulting from the simultaneous closure of more than one switch are rejected by the Processor, thereby preventing invalid operation.

Displays

10 The liquid crystal display modules are connected directly to the Module Data Bus and are supplied with a low frequency square wave signal from the backlighting control circuitry; this is required by the internal driver devices to drive the LCD displays.

11 For the FREQUENCY and BARGRAPH DISPLAY MODULES, all the coded display information is sent serially in 20 bytes on the Module Data Bus whenever the display requires modification. The 2-bit bytes for the BARGRAPH DISPLAY MODULE are loaded into an internal shift register by a negative-going strobe pulse on the port 2 line from the ADDRESS DECODER (W2 pin 4). Similarly, the 6-bit wide bytes for the FREQUENCY DISPLAY MODULE are loaded by a strobe pulse on port 4 (W3 pins 5, 6 and 19). The data is latched from the internal shift registers to the displays by a write strobe pulse on W2 pin 3 and W3 pin 1 respectively.

12 In the DOT MATRIX DISPLAY MODULE the mode legends are driven by data written into the external DATA LATCH. The 2 x 20 dot matrix characters are driven by internal processing circuits incorporating a character generator. Instruction bytes on the Module Data Bus are loaded into a register in the processing circuits by a low on W1 pin 17 in order to define the display configuration. W1 pin 17 then goes high followed by a strobe pulse on W1 pin 15 which allows data now present on the Module Data Bus to set up the character generator and display the required character. Because the dot matrix displays are multiplexed, a narrower viewing angle results, but this can be adjusted using the menu system. This is achieved by means of a control voltage derived from digital to analogue conversion of data received on the Module Data Bus.

Backlighting Control

13 The backlighting control circuit allows the backlighting intensity of the displays to be adjusted from the front panel, using the menu system, and is powered from the +15 V unregulated supply. It provides an efficient way of regulating the current through the backlighting bulbs to compensate for variations in the unregulated supply and therefore maintain constant brightness. The circuit consists basically of a pulse width modulator (PWM) connected to drive circuits which control the supply to the backlighting bulbs. A feedback control loop allows the intensity to be stabilised at one of eight possible brightness settings from data received on the Module Data Bus.

Pulse width modulator

14 An OSCILLATOR generates a triangular waveform for application to a comparator operating as a PULSE WIDTH MODULATOR (PWM). When a variable DC voltage is applied to the other input of the comparator, the pulse width of the output waveform is varied accordingly, and this is used to vary the intensity of the backlighting after processing by further stages.

Delay and drive circuit

15 This circuit takes the modulated waveform from the PWM and performs a number of functions. Firstly, two non-overlapping signals are produced from the modulated waveform, suitable for driving the switched transistors in the OUTPUT STAGE. Secondly, a delay circuit modifies these non-overlapping waveforms such that a minimum acceptable brightness level can be achieved. Finally, the drive waveform of 125 Hz nominal for the display modules is derived from this circuit by dividing the waveform from the PWM.

16 The minimum pulse width provided by the PWM is too wide to achieve the required minimum brightness level. The DELAY AND DRIVE CIRCUIT effectively reduces this pulse width by gating a delay pulse of approximately 200 µs, provided by monostable ML21, with the drive waveforms to the OUTPUT STAGE as shown in Fig. 11.3.

Output stage

17 The two non-overlapping PWM signals are used to drive an OUTPUT STAGE containing a transistor switching circuit which converts the unregulated +15 V DC into a variable pulse width AC supply for the backlighting bulbs. Protection circuits are included in the drive path to prevent damage to the transistors occurring, and hence to the bulbs, if the drive waveform is absent.

Control feedback loop

18 The two non-overlapping pulse waveforms driving the bulbs are fed back to the control loop from the OUTPUT STAGE via D6 and D7. These diodes perform half wave rectification producing a feedback signal of double the frequency of the two waveforms driving the bulbs. The feedback signal is fed via a potential divider to a non-inverting FIXED DC OFFSET AMPLIFIER which is biased such that it operates linearly. Ripple on the feedback signal is filtered by R66 and C34. The resultant DC control voltage is applied via buffer ML17(c) to the inverting input of the LOOP AMPLIFIER. This gives a corresponding reduction in control voltage for an increase in output to the bulbs.

19 The LOOP AMPLIFIER compares the feedback voltage with the brightness control voltage and produces a control voltage at its output which is fed to the PWM. This determines the width of the PWM output waveform and hence enables the brightness level to be held constant at the level established by the level control.

Brightness level decoding

20 Data representing one of eight possible brightness levels is received on the Module Data Bus from the Processor by a digital to analogue converter (DAC) and a corresponding output voltage is interfaced to the control loop to control the brightness level.

Audio Outputs

21 A pair of AUDIO AMPLIFIERS receives the audio input signal via a VOLUME CONTROL on the front panel, which is adjusted for the desired audio level at the loudspeaker and phone outputs. Muting of the audio output to the loudspeaker occurs when the mute line is activated by the Processor, in response to the loudspeaker push button on the front panel being operated.

Bus Interface

22 The ADDRESS DECODER in the Front Panel Assembly detects addresses on the Module Address Bus from the Processor Module to produce control signals for various functions throughout the assembly. These signals write data into the display modules and a DATA LATCH, which provides control of a BITE MULTIPLEXER and the illumination of legends displayed on the dot matrix display. The control signals also allow data from the tuning INTERFACE CIRCUIT and SWITCH SELECT BUFFER, as well as the assembly identification code, to be read by the Processor via the Module Data Bus.

BITE Measurement System

23 The BITE measurement system, comprising the BITE MULTIPLEXER operating in conjunction with a BITE COMPARATOR, allows the Processor Module to monitor the setting of the IF GAIN CONTROL and measure various voltages in the Front Panel Assembly. The voltage to be measured is selected by the BITE MULTIPLEXER and compared in the BITE COMPARATOR with a voltage generated by a DAC in the Processor Module. The Processor Module measures the level of the selected voltage by applying voltages representing upper and lower limits to the comparator and then monitoring the resulting output.

FAULT FINDING

General

24 Fault finding techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the Front Panel Assembly is contained in the following sections.

BITE Tests

25 The following BITE tests for the Front Panel Assembly are arranged in the order in which they are performed or presented for selection.

TEST NUMBER : 151

TITLE : BITE hardware

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : DAC 1 line is set to 2.55 volts (i.e. max). BITE multiplexer input X1 (+5volts) is selected and the output of the BITE comparator is checked to ensure that it is low.

LIMITS : Less than 0.8 V at TP8.

FAULT DIRECTORY : Fault No. 2

TEST NUMBER : 152, 153, 154, 155

TITLE : +5V rail, +15V audio rail, -15V rail, +15V rail.

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : The appropriate BITE multiplexer input is selected and the supply voltage is checked.

LIMITS :

Test No.	Supply	Mux. Input	Mux Limits (TP8)	
			Lower	Upper
152	+ 5 V	X2	1.78 V	2.22 V
153	+15 V (Audio)	X3	1.7 V	2.21 V
154	- 15 V	X4	1.65 V	2.24 V
155	+15 V	X5	1.7 V	2.21 V

FAULT DIRECTORY : Fault No. 4

TEST NUMBER	:	156
TITLE	:	Displays Test.
PERFORMED	:	Unit confidence test, select test.
DESCRIPTION	:	Using test patterns, all the front panel displays are tested in the following sequence: (1) "Testing Character Display" message shown for 4 seconds to indicate display under test and all legends blanked. (2) Complete display exhibits a "checkerboard" pattern for 1 second and then turns on each legend at 1 second intervals. (3) Each legend is then turned off in the same order at 1 second intervals. (4) "Testing Frequency Display" message shown for 2 seconds and all legends blanked. (5) All address, channel and frequency displays are sequenced through their range of digits, from 0 to 9, with each set held for 2 seconds. (6) Display is then blanked and each legend is turned on, one by one, at 1 second intervals. (7) Each legend is then turned off in the same order at 1 second intervals. (8) "Testing Bargraph Display" message shown for 2 seconds, then each legend is illuminated in turn for 1 second. (9) The AF and RF meter scales are each activated to on for 1 second in turn. The bars are illuminated from left to right with a 0.25 second gap between bars, and then extinguished in reverse order.
FAULT DIRECTORY	:	Fault No. 5 or 6.

TEST NUMBER	:	157
TITLE	:	Keyboard Test.
PERFORMED	:	Select test.
DESCRIPTION	:	Each key is tested when pressed by the operator in response to the message "Press the * * * * key", where * * * * is the key to be pressed. The test fails if the wrong key is pressed.
FAULT DIRECTORY	:	Fault No. 10.

Fault Directory

26 Use the following fault directory to identify the fault condition and take the necessary corrective action. Note that all inputs to the assembly are assumed to be correct.

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
1	Fails to run BITE tests for Front Panel Assembly.	Address decoder/assembly ident. not responding.	Check address decoding/assembly ident logic operation using signature analysis routine if necessary.
2	BITE hardware fault.	Comparator/multiplexer inoperative.	Use BITE test 151 to check comparator operation. Select all BITE tests for the Front Panel to check multiplexer operation for all analogue inputs. Use signature analysis routine to check multiplexer addressing.
3	BITE indicates failure but manual check shows no fault.	BITE hardware fault.	As Fault No. 2.
4	Power supply fault within module.	Faulty component drawing excess current.	Locate and replace faulty component.
5	All displays inoperative	(a) Address decoder fault. (b) Backlighting drive waveform absent.	(a) Use signature analysis routine to trace fault. (b) See Fault No. 7.
6	Fault confined to individual display.	(a) Display module faulty. (b) Address decoder fault.	(a) Replace suspect display module. (b) As Fault No. 5.
7	No backlighting.	Backlighting control circuit faulty.	Follow backlighting control check procedure.
8	Unable to control via menu system.	Dual DAC ML4 faulty.	Using oscilloscope, check ML4 brightness level control output varies when the backlighting level is varied via the menu system.
9	No audio output	(a) Audio amplifier fault. (b) Audio input absent. (c) Faulty volume control. (d) Mute activated.	(a) Check both loudspeaker and phones outputs to establish if fault is common to both amplifiers. Check signal levels around suspect circuit. (b) Check audio is being applied to the volume control. (c) Check operation. (d) Operate L/S button and check that logic 1 can be obtained on ML8 (b) pin 14.
10	No response to pressing any key.	Faulty switch select buffer or row select decoder.	Use signature analysis routine to check circuit action.
11	Failure of individual or group of switches.	Faulty switch matrix, switch select buffer or row select decoder.	See Fault No. 10.
12	Tuning knob stiff.	Excessive tuning knob friction.	Remove knob and adjust preset screw located behind it.

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
13	No response from rotating main tuning knob.	(a) Faulty shaft encoder.	(a) Check output waveforms present on links 1 and 2.
		(b) Interface circuit inoperative.	(b) Check for pulses on TP7 and for changing level on TP9 as direction of rotation is changed. Using oscilloscope, check counter outputs toggle when tuning knob is rotated.
14	Unable to control viewing angle of dot matrix display.	(a) Faulty dual DAC	(a) Using oscilloscope, check ML4 view angle control output varies when the view angle is varied via the menu system.
		(b) Faulty display module.	(b) Replace.
15	Unable to control IF gain.	(a) Faulty potentiometer or bias circuit.	(a) Check 2.8V is applied to potentiometer. Locate and replace faulty component.
		(b) BITE multiplexer faulty.	(b) BITE hardware fault (see Fault No. 2.)

Backlighting Control Check Procedure

Oscillator output

27 The free-running triangular wave oscillator may be checked by connecting the frequency counter to TP6 and ensuring that the frequency is between 350 and 750 Hz. The amplitude of the triangular waveform should be 30 V peak-to-peak nominal, measured on an oscilloscope.

Drive circuit control

28 Remove links LK3 and 4 to break the control loop and connect the frequency counter to LK3 pin 1. The frequency of the drive circuit output should be between 175 and 375 Hz.

29 Connect TP4 to 0V and check that the voltage at TP5 is between +13 V and +15 V. Check that the counter reads between 175 and 375 Hz.

30 Using an external DC power supply, apply 27V to TP4 and check that the voltage at TP5 is between -13 V and -15 V.

31 Repeat the previous two paragraphs with the counter connected to LK4 pin 1.

Overall loop

32 Remove the counter and external DC supply. Replace links LK3 and 4 to restore the control loop. Check that the level on ML13 (a) pin 3 changes in response to different brightness settings determined via the menu system. Use the appropriate part of signature analysis routine if faulty.

33 Set the brightness level control for maximum (using the menu system) and ensure that between +9 V and +11 V rms is present on TP4. If minumum brightness is unobtainable check that the dual monostable, ML21, produces 200 µs (approx) pulses to clock the delay latches. If this fails to locate the fault, use signature analysis.

PARTS LIST

34 35 The Racal part number for a complete Front Panel Assembly (RA3701/RA3702/MA3700) is ST86482. When ordering specify equipment number.

35 36 Information on the identification and handling of SMDs is provided in Chapter 2. The parts list for the Front Panel Assembly is as follows:

SIGNATURE ANALYSIS ROUTINE

36 This routine checks that the module control signals are interfaced and decoded correctly from the module bus.

Processor Module DIL switch settings: SW7,1,2,3 OFF
SW4,5,6,8 ON

Signature Analyser connections:

Start: TP2 Front panel negative trigger
Stop: TP2 Front panel negative trigger
Clock: Test point 8A on extender assembly, negative trigger
Earth: Test point 1B on extender assembly

Note : Signatures xxxxF signify a flashing probe indicator.
Note: Before running the Front panel signature routine disconnect the loudspeaker (PL3).

Signal	Signature	Test Node						Remarks
+5V	1CAU							
OV	0000							
		DATA BUS INTERFACES						
M-DO	8C37	PL1/15	ML10/18	ML4/3	ML5/3	ML16/18		
		W3/13	W2/2	W7/16				Module bus
M-D1	2UPU	PL1/16	ML10/16	ML4/4	ML5/4	ML16/16		
		W3/4	W2/13	W7/13				Module bus
M-D2	72C5	PL1/13	ML10/14	ML4/7	ML5/7	ML16/14		
		W3/3	W7/14					Module bus
M-D3	39H1	PL1/14	ML10/12	ML4/8	ML5/8	ML16/12		
		W3/15	W7/11					Module bus
M-D4	1FU8	PL1/11	ML10/9	ML4/13	ML5/13	ML16/9		
		W3/17	W7/12					Module bus
M-D5	F5C1	PL1/12	ML10/7	ML4/14	ML5/14	ML16/7		
		W3/20	W7/9					Module bus
M-D6	1FC8	PL1/9	ML10/5	ML4/17	ML5/17	ML16/5	W7/10	Module bus
M-D7	4HUC	PL1/10	ML10/3	ML4/18	ML5/18	ML16/3	W7/7	Module bus
		ADDRESS DECODER						
M-A0	5H68	PL1/25	R14	ML18/2	ML20/1			Module bus
M-A1	7483	PL1/26	R15	ML18/13	ML20/2	ML19/11		Module bus
M-A2	1C83	PL1/23	R16	ML20/3	ML19/10			Module bus
M-A3	9A8C	PL1/24	R17	ML18/14	ML19/9	W7/17		Module bus
M-A4	0000	PL1/21	R18	ML3/10				Module bus
M-A5	0001	PL1/22	R19	ML3/9				Module bus
M-A6	0001	PL1/19	R20	ML3/2				Module bus

SIGNATURE ANALYSIS ROUTINE (continued)

Signal	Signature	Test Node						Remarks
		ADDRESS DECODER						
M-STB	0000F	PL1/17	R22	ML20/6				Module bus
ML3/3	0001	ML3/3	ML3/4					Address decoder
ML3/8	0001	ML3/8	ML3/5					Address decoder
ML3/6	0001	ML3/6	TP2	ML18/1	ML20/4			Address decoder
PORT0	1CAUF	ML20/15	ML5/11					PORT0 Select
PORT1	1CAUF	ML20/14	ML7/13					PORT1 Select
PORT2	1CAUF	ML20/13	W2/4					PORT2 Select
PORT3	1CAUF	ML20/12	ML7/11					PORT3 Select
PORT4	1CAUF	ML20/11	W7/6	W7/5	W7/19			PORT4 Select
PORT5	1CAUF	ML20/10	ML7/9					PORT5 Select
PORT6	1CAUF	ML20/9	ML4/11					PORT6 Select
ML18/7	1CH1	ML18/7	ML10/1	ML10/19				Keypad select
ML18/6	8HH7	ML18/6	ML18/15					
ML18/11	1CAU	ML18/11	ML16/1	ML16/19	ML7/5			Shaft encoder
ML7/6	0000	ML7/6	ML13/5					Shaft encoder
ML7/12	0000F	ML7/12	W7/15					
ML7/10	0000F	ML7/10	W2/3					
ML7/8	0000F	ML7/8	W3/1					
ML18/12	8HH7	ML18/12	ML8/7					ID
ML8/1	8C37	ML8/1						ID
		DATA LATCH (BITE Multiplexer) (ML6)						
Q0	H86C	ML5/2	ML6/11					CONTROL S0
Q1	9F4H	ML5/5	ML6/10					CONTROL S1
Q2	CP5P	ML5/6	ML6/9					CONTROL S2
		DOT MATRIX LCD (W7)						
BFO	A7H3	ML5/12	W7/2					BFO Legend
ANT	61C0	ML5/16	W7/1					ANT Legend
AGC	2391	ML5/15	W7/6					AGC Legend
BW	40A0	ML5/19	W7/4					BW Legend
		DUAL DAC (ML4)						
Q0	2HC6	ML4/2	R46					Level control
Q1	CACA	ML4/5	R38					Level control
Q2	U13F	ML4/6	R45					Level control
Q3	295H	ML4/9	ML8/8					Speaker mute
Q4	3CCF	ML4/12	R36					Viewing angle
Q5	F5C1	ML4/15	R35					Viewing angle
Q6	32FF	ML4/16	R34					Viewing angle
RESET	ICAU	PL1/27	ML8/10	ML9/1	ML9/13	ML21/3	ML21/11	
		ML22/10	ML4/1					

SIGNATURE ANALYSIS ROUTINE (continued)

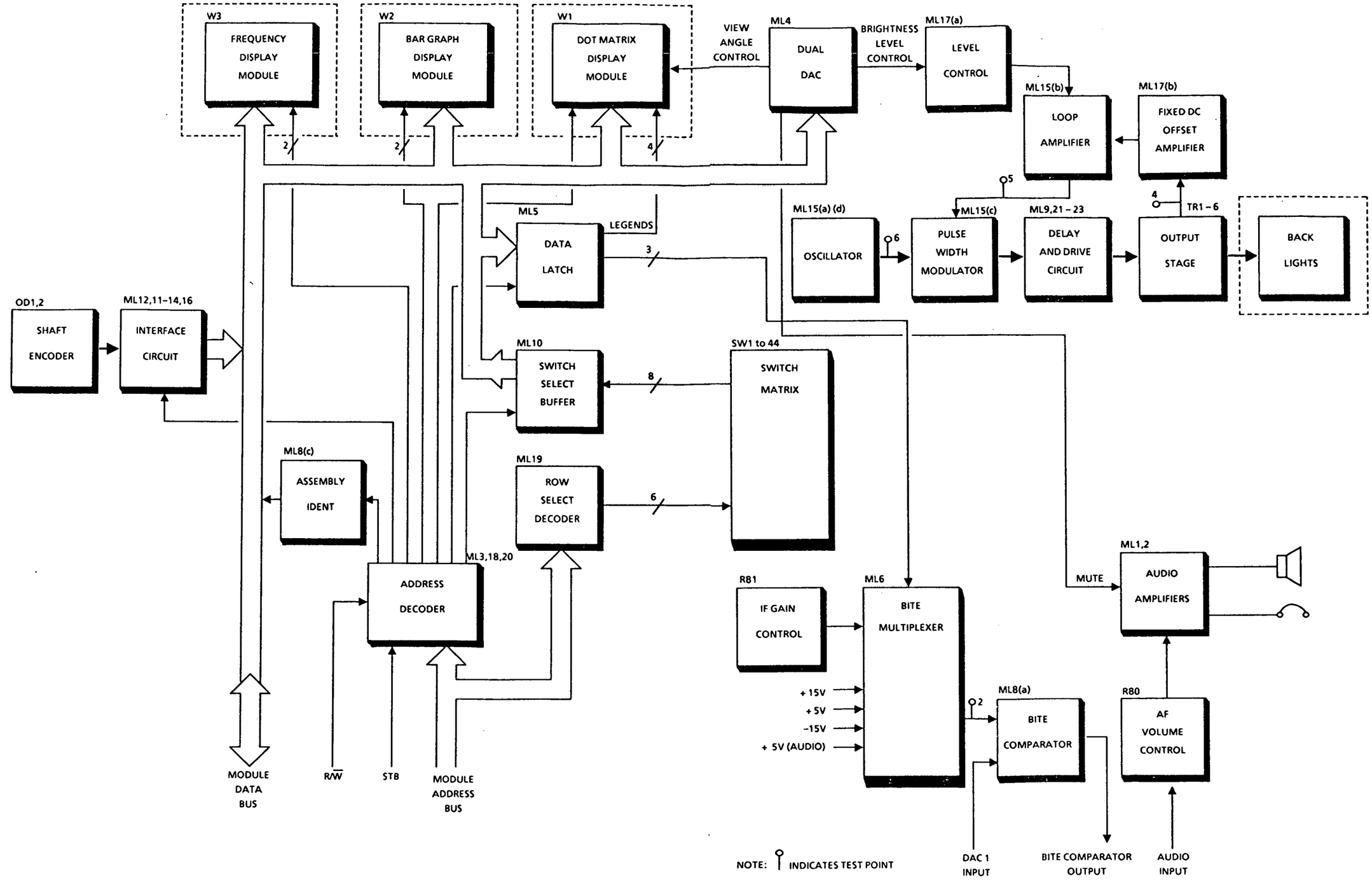
Signal	Signature	Test Node		Remarks
		SWITCHES		
S1	8127	ML19/1	ML10/8	
S2	8127	ML19/1	ML10/6	
S3	391C	ML19/13	ML10/8	
S4	391C	ML19/13	ML10/6	
S5	391C	ML19/13	ML10/4	
S6	391C	ML19/13	ML10/2	
S7	1CAH	ML19/5	ML10/8	
S8	1CAH	ML19/5	ML10/6	
S9	1CAH	ML19/5	ML10/4	
S10	1CAH	ML19/5	ML10/2	
S11	A3CH	ML19/14	ML10/8	
S12	A3CH	ML19/14	ML10/6	
S13	A3CH	ML19/14	ML10/4	
S14	A3CH	ML19/14	ML10/2	
S15	H73H	ML19/12	ML10/8	
S16	H73H	ML19/12	ML10/6	
S17	H73H	ML19/12	ML10/4	
S18	H73H	ML19/12	ML10/2	
S19	FFCU	ML19/15	ML10/8	
S20	FFCU	ML19/15	ML10/6	
S21	FFCU	ML19/15	ML10/4	
S22	FFCU	ML19/15	ML10/2	
S23	FFCU	ML19/15	ML10/11	
S24	FFCU	ML19/15	ML10/13	
S25	FFCU	ML19/15	ML10/15	
S26	FFCU	ML19/15	ML10/17	
S27	H73H	ML19/12	ML10/13	
S28	H73H	ML19/12	ML10/15	
S29	H73H	ML19/12	ML10/17	
S30	H73H	ML19/12	ML10/11	
S31	A3CH	ML19/14	ML10/13	
S32	A3CH	ML19/14	ML10/15	
S33	A3CH	ML19/14	ML10/17	
S34	1CAH	ML19/5	ML10/11	
S35	1CAH	ML19/5	ML10/13	
S36	1CAH	ML19/5	ML10/15	
S37	1CAH	ML19/5	ML10/17	
S38	391C	ML19/13	ML10/13	
S39	391C	ML19/13	ML10/15	
S40	391C	ML19/13	ML10/17	
S41	8127	ML19/1	ML10/11	
S42	8127	ML19/1	ML10/13	
S43	8127	ML19/1	ML10/15	
S44	8127	ML19/1	ML10/17	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Display Assemblies							
			LCD Module (Frequency)			CD86664	
			LCD Module (Mode)			CD86665	
			LCD Module (Meter)			CD86666	
			Lamp Board (Meter)			BD87598	
			Lamp Board (Frequency/Mode)			BD87599	
Electro-Mechanical Devices							
			Switch, Optical			945210H	
			Switch, Pushbutton			945172I	
			Switch, Rocker			938535N	
Front Panel Board						ST86482	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R52	M4	120k	Thick Film Chip	0.125	2	943915R	124
R53	M4	18k	Thick Film Chip	0.125	2	943905K	183
R54	M4	100k	Thick Film Chip	0.125	2	943914A	104
R55	M4	68k	Thick Film Chip	0.125	2	943912C	683
R56	M1	47k	Thick Film Chip	0.125	2	943910E	473
R57	M1	22k	Thick Film Chip	0.125	2	943906B	223
R58	M1	100k	Thick Film Chip	0.125	2	943914A	104
R59	M2	4k7	Thick Film Chip	0.125	2	943898N	472
R60	M1	180R	Thick Film Chip	0.125	2	943881V	181
R61	M1	33k	Thick Film Chip	0.125	2	943908Z	333
R62	N1	180R	Thick Film Chip	0.125	2	943881V	181
R63	N1	100k	Thick Film Chip	0.125	2	943914A	104
R64	P1	10k	Thick Film Chip	0.125	2	943902F	103
R65	P1	10k	Thick Film Chip	0.125	2	943902F	103
R66	R1	220R	Thick Film Chip	0.125	2	943882M	221
R67	P4	2k2	Thick Film Chip	0.125	2	943894R	222
R68	R4	100k	Thick Film Chip	0.125	2	943914A	104
R69	R7	18k	Thick Film Chip	0.125	2	943905K	183
R70	R5	8k2	Thick Film Chip	0.125	2	943901O	822
R71	R4	3k2	Thick Film Chip	0.125	2	943896P	322
R72	R7	100k	Thick Film Chip	0.125	2	943914A	104
R73	R5	68k	Thick Film Chip	0.125	2	943912C	683
R74	R4	47k	Thick Film Chip	0.125	2	943910E	473
R75	S3	220k	Thick Film Chip	0.125	2	943918G	224
R76	S7	270R	Thick Film Chip	0.125	2	943883T	271
R77	S4	220k	Thick Film Chip	0.125	2	943918G	224
R78	S2	47k	Thick Film Chip	0.125	2	943910E	473
R79	T7	1k8	Thick Film Chip	0.125	2	943893A	182
R80		10k	Variable, Linear		20	AD87133	
R81		10k	Variable, Log		20	AD87098	
Capacitors				V			
C1		220µ	Electrolytic	40	-10 +50	945005L	
C2		33µ	Electrolytic	40	-10 +50	945205N	
C3	B1	330µ	Electrolytic	25	-10 +50	945006C	
C4	B2	100µ	Electrolytic	25	-10 +50	921546L	
C5	B3	100n	Ceramic Chip	50	20	945146T	
C6	B2	100n	Ceramic Chip	50	20	945146T	
C7	B3	18p	Ceramic Chip	50	5	941790U	
C8	B2	18p	Ceramic Chip	50	5	941790U	
C9	C3	100n	Ceramic Chip	50	20	945146T	
C10	C2	100n	Ceramic Chip	50	20	945146T	
C11	C5	3µ3	Tantalum Chip	16	20	945050N	
C12	C4	100n	Ceramic Chip	50	20	945146T	
C13	C3	100n	Ceramic Chip	50	20	945146T	
C14	C3	6µ8	Tantalum Chip	35	20	945052L	
C15	C2	6µ8	Tantalum Chip	35	20	945052L	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C16	D5	100n	Ceramic Chip	50	20	945146T	
C17	D5	100n	Ceramic Chip	50	20	945146T	
C18	D2	6µ8	Tantalum Chip	35	20	945052L	
C19	D3	100n	Ceramic Chip	50	20	945146T	
C20	E5	100n	Ceramic Chip	50	20	945146T	
C21	D4	100n	Ceramic Chip	50	20	945146T	
C22	E6	100n	Ceramic Chip	50	20	945146T	
C23	E5	100n	Ceramic Chip	50	20	945146T	
C24	F5	3µ3	Tantalum Chip	16	20	945050N	
C25	G5	3µ3	Tantalum Chip	16	20	945050N	
C26	K1	100n	Ceramic Chip	50	20	945146T	
C27	L1	3µ3	Tantalum Chip	16	20	945050N	
C28	L2	100p	Ceramic Chip	50	5	941799N	
C29	L2	10n	Ceramic Chip	50	10	941775D	
C30	M5	100p	Ceramic Chip	50	5	941799N	
C31	N1	3µ3	Tantalum Chip	16	20	945050N	
C32	P1	100n	Ceramic Chip	50	20	945146T	
C33	P1	3µ3	Tantalum Chip	16	20	945050N	
C34	R4	100n	Ceramic Chip	50	20	945146T	
C35	R7	1µ	Tantalum Chip	35	20	945049Z	
C36	S3	1n	Ceramic Chip	50	10	941772O	
C37	S3	1n	Ceramic Chip	50	10	941772O	
C38	S4	100n	Ceramic Chip	50	20	945146T	
C39	S2	47p	Ceramic Chip	50	5	941795H	
Inductors				W			
L1	D5	6µH8	Choke	0.2	10	939694S	
Diodes							
D1	E4		BZX84-C 5V1, Zener			945108J	
D2	F5		BAS 16			943951D	
D3	F5		BAS 16			943951D	
D4	L1		BZX84-C 5V1, Zener			945108J	
D5	M4		BAS 16			943951D	
D6	S7		BAS 16			943951D	
D7	T7		BAS 16			943951D	
Transistors							
TR1	E5		ZTX 650L, NPN			945212F	
TR2	E5		ZTX 650L, NPN			945212F	
TR3	E5		ZTX 750L, PNP			945211O	
TR4	E5		ZTX 750L, PNP			945211O	
TR5			MMBT2222A, NPN			943949Y	
TR6			MMBT2222A, NPN			943949Y	
TR7	D2		BC 859, PNP			943942N	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Integrated Circuits		CAUTION:	*SSD - STATIC SENSITIVE DEVICES				
ML1			380, Audio Amplifier			945018H	
ML2			380, Audio Amplifier			945018H	
ML3	E6	*SSD	74HC32, Quad 2-Input OR Gate			943975D	
ML4	K5	*SSD	74HC273, D-Type Flip-Flop			943989G	
ML5	K5	*SSD	74HC377, D-Type Flip-Flop			943990E	
ML6	L4	*SSD	4051, 8-Channel Multiplexer			943993J	
ML7	L3	*SSD	74HC14, Hex Schmitt Trigger Inverter			945209J	
ML8	L2		339, Quad Voltage Comparator			945023R	
ML9	L2	*SSD	74HC74, Dual D-Type Flip-Flop			943977L	
ML10	L5	*SSD	74HC244SSD, Octal Line Driver			943987I	
ML11	L3	*SSD	4516, Binary Up/Down Counter			945047B	
ML12	L2	*SSD	74HC86, Quad Exclusive OR Gate			943979J	
ML13	M3	*SSD	4516, Binary Up/Down Counter			945047B	
ML14	M2	*SSD	74HC74, Dual D-Type Flip-Flop			943977L	
ML15	M2		324, Quad Operational Amplifier			945026G	
ML16	M5	*SSD	74HC244, Octal Line Driver			943987I	
ML17	R4		324, Quad Operational Amplifier			945026G	
ML18	R3	*SSD	74HC139, Dual 2 to 4 Line Decoder			943982V	
ML19	R2	*SSD	4051, 8-Channel Multiplexer			943993J	
ML20	R2	*SSD	74HC138, 3 to 8 Line Decoder			943980X	
ML21	S3	*SSD	74HC123, Retriggerable Monostable			945206E	
ML22	S2	*SSD	74HC74, Dual D-Type Flip-Flop			943977L	
ML23	S2	*SSD	74HC08, Quad 2-Input AND Gate			943972Y	
Connectors							
PL1			Plug, 34-Way			945453W	
PL2			Plug, 20-Way			943728L	
PL3			Plug, 3-Way			943740N	
Switches							
S1 to S44			Push button			945172I	
S45			Rocker			938535N	
Miscellaneous							
W1			Cable Assembly			BA87139	
W2			Cable Assembly			BA87139	
W3			Cable Assembly			BA87139	
TP1 to TP9			Terminal, Assembly (test points)			936148X	
P1 to P6			Terminal, Pin			916945K	
LK1 to LK4			Comprising: Plug, 4-Way			945062S	
			Shorting Link			943684I	



Front Panel Assembly (RA3701/2): Block Diagram **Fig.11.4**

CHAPTER 12

POWER SUPPLY REGULATOR MODULE

CONTENTS

ILLUSTRATIONS

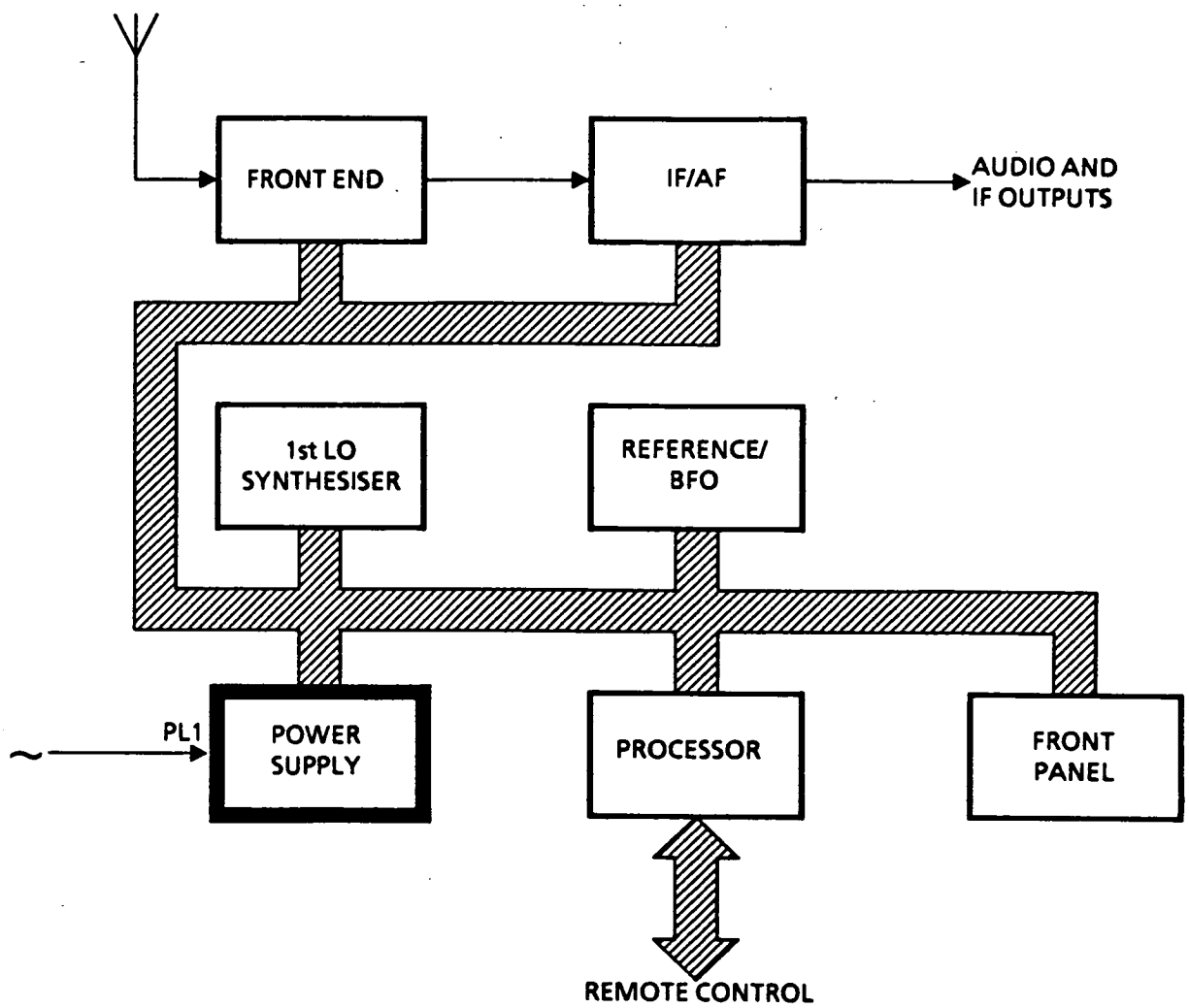


Fig. 12.1 Receiver Block Diagram

CHAPTER 12

POWER SUPPLY REGULATOR MODULE

INTRODUCTION

1 The Power Supply Regulator Module forms part of a linear AC power supply to provide four regulated voltages of +24 V, +15 V, +5 V and - 15 V which are distributed via the motherboard for use throughout the equipment. In addition, two unregulated supplies of +15V and +5 V are also provided for use in the Front Panel Assembly and 1st LO Synthesiser Module respectively.

Fig.12.1 Receiver Block Diagram

2 A power-up reset circuit is also included to inhibit functions in the Processor Module and the Front Panel Assembly until the +5 V supply has reached its rated level after switch-on. If the +5 V rail falls below this level during normal operation, the reset circuit is activated.

3 This description includes the major power supply components mounted on the chassis so that an overall explanation of the power supply operation can be realised. No adjustments are necessary.

MODULE DESCRIPTION

4 The following description should be read in conjunction with the Power Supply Regulator Module Block and Circuit Diagrams included with this chapter. Component references shown on the Block Diagram allow it to be related to the Circuit Diagram.

Mains Input

5 The power input connector PL1, supply filter components and voltage selector are all contained in a MAINS VOLTAGE SELECTOR AND FILTER package. The voltage selector consists of a drum which can be inserted in four different ways to suit a mains input voltage of 100, 120, 220 or 240 volts, thereby arranging an appropriate POWER TRANSFORMER primary connection.

6 The supply path to the POWER TRANSFORMER is interrupted by a POWER ON/OFF SWITCH mounted on the Front Panel Assembly, thus allowing the mains input to be switched off. Mains input protection is provided by a 2A slow-blow fuse (FS1).

7 Four bridge rectifiers, each followed by a smoothing capacitor, are fed with AC outputs produced by separate windings on the POWER TRANSFORMER and provide unregulated DC supplies for the regulators.

Supply Regulation

8 The regulators for the +24 V, +15 V and +5 V supplies use the same basic circuit constructed from discrete components, while the -15 V supply uses a standard three-terminal monolithic regulator. In addition to providing a stabilised voltage output, all three discrete component regulators feature short-circuit protection to prevent damage to the power supply should the external circuit fail.

9 For two of these regulators (+15 V and +5 V), overvoltage protection is also included to prevent damage to the equipment if the supply voltage exceeds its limits. When activated, this circuit causes the fuse to blow. Each regulated output voltage is monitored by a light emitting diode (LED) mounted on top of the module.

10 The three-terminal monolithic -15 V regulator contains a current limiting circuit to maintain the peak current passed to a safe value. If the current dissipation becomes too high for the heat sinking provided, an internal thermal shutdown circuit takes over to prevent damage to the regulator.

Voltage Stabilization

11 Since the regulators for the +24 V, +15 V and +5 V supplies are similar, only the operation of the +5 V regulator is described. In this circuit the difference between the output voltage and a +5 V reference voltage is sensed by an error amplifier formed by comparator ML5(a) and drive amplifier TR2, and this is used to control a series pass transistor, TR1, which in turn controls the output voltage.

Overload Protection

12 Under normal operating conditions the overload protection circuit, comprising ML5(b) and blocking diode D16, has no effect due to D16 being reversed biased by approximately +25 V on ML5(b) output. This is because the voltage drop across the load sensing resistors, R4 and R5, is arranged to be insufficient to drive ML5(b) output low for normal supply currents.

13 As current flow through the sensing resistors increases to the point of foldback, comparator ML5(b) begins to turn off TR2 by sinking current through D16. As TR2 turns off, the output voltage drops and hence the load current drops until both the voltage and current have folded back to a safe level. R41 divided by the parallel combination of R42 and R47 sets the maximum gain around the foldback loop.

14 To prevent the foldback circuit operating on switch-on, a start-up voltage derived from the +5 V REFERENCE circuit is applied via R46 to the comparator to ensure that it powers up in the correct state.

15 During normal operation, a potential divider formed by R45 and R46 connected between the start-up voltage rail and the regulator output, provides the correct voltage at the foldback comparator input.

Overvoltage Protection

16 Use is made of a crowbar protection circuit comprising thyristor SCR1 and zener diode D17 to prevent overvoltage conditions occurring at the supply output. Any overvoltage causes zener D17 to conduct and a bias voltage is developed across R43 which is used to fire the thyristor gate. The thyristor switches on and causes a high current to pass through the fuse until it blows, thus disabling the regulator.

Internal +30 V Supply

17 The operational amplifier devices used throughout the power supply require a +30 V supply to operate. This is provided by a +30 V SUPPLY circuit which operates from the output of the +24 V RECTIFICATION circuit.

Reset Circuit

18 Upon switch-on, a POWER-UP RESET GENERATOR maintains an active low on the reset line for approximately 0.5 seconds to allow the supplies to reach their rated levels. In this circuit, ML6(a) applies +4.9 V to both ML6(c) and ML6(d) at switch-on. Due to circuit capacitance, the +5 V regulated output applied to the other inputs of these comparators takes longer to reach its operating voltage. This results in ML6(c) and ML6(d) outputs being initially high, turning on both TR9 and TR8 and holding the reset line low. When the +5 V rail achieves its operating level, ML6(c) output falls, turning off TR9. This allows time constant R51, C20 to charge up and ML6(d) output falls, turning off TR8 and removing the low on the reset line.

19 The reset line is also activated for approximately 0.25 seconds when the +5 V supply falls below +4.9 V, as would occur, for instance, if the +5 V supply were momentarily shorted. ML6(c) senses the voltage drop and switches on TR9 to clamp ML6(d) output high. This subsequently switches on TR8 to place a low on the reset line. On recovery of the +5 V supply the circuit action is as before but with a shorter reset pulse due to the now charged capacitance in the +5 V supply.

Reference Circuit

20 The +5V reference for the comparators in the regulators and reset circuits is derived from the +30 V SUPPLY using a +5 V REFERENCE device.

FAULT FINDING

General

21 Fault finding techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the power supply is contained in the following sections.

Fault Directory

22 Use the following fault directory to identify the fault condition and take the necessary corrective action. Note that all loads presented to the module are assumed to be correct.

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
1	All supply indicators unlit.	(a) Mains fuse (FS1) on chassis blown.	(a) Replace. If blows again, check that the correct mains tapping is selected and then check for short circuit around mains input.
		(b) Open circuit in voltage selector unit components, power transformer or mains on/off switch.	(b) Locate faulty component and replace. (Use power supply circuit diagram in Chap.13).
		(c) PL1 on Regulator Module not connected.	(c) Reconnect.
2	+5V indicator only unlit.	(a) Fuse FS1 blown.	(a) Replace. If blows again, check for a short circuit around the +5V regulator or between supplies i.e. +20V and +5V.
		(b) +5V regulator or rectification circuit faulty.	(b) Check voltage on TP1 to determine whether the fault is on the chassis (Chap. 13) or Power Supply Regulator Module, then check circuit voltages.
3	+15V indicator only unlit.	(a) Fuse FS2 blown.	(a) As Fault No. 2 but substituting the +15V regulator.
		(b) +15V regulator or rectification circuit faulty.	(b) Check voltage on TP6, then proceed as in Fault No. 2.
4	-15V indicator only unlit.	-15V regulator or rectification circuit faulty.	Check voltage on TP5 to determine whether the -15V regulator or -15V rectifier is faulty, then check circuit voltages.
5	+24V indicator only unlit.	+24V regulator or rectification circuit faulty.	Check voltage on TP10 to determine whether the +24V regulator or +24V rectifier is faulty, then check circuit voltages.
6	All +24V, +15V, +5V regulated outputs absent or wrong voltage.	(a) +30V op.amp. supply faulty.	(a) Check voltage on TP3.
		(b) Start-up voltage derived from +5V reference absent.	(b) Check voltage on TP8, to verify +5V reference.
7	Data corruption in Processor occurring when power is switched off and on.	No reset pulse being generated.	Check TP2 with oscilloscope for presence of pulse on power-up.
8	Any one of the regulated or unregulated voltages low.	(a) Over voltage protection circuit faulty.	(a) Check circuit voltages.
		(b) Excess loading of supply line.	(b) Trace origin by removing modules one at a time.

PARTS LIST

23 The Racal part number for a complete Power Supply Regulator Module is ST86489.

24 Information on the identification and handling of SMDs is provided in Chapter 2. The parts list for the Power Supply Regulator Module is as follows:

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R1		1k5	Metal Film	0.25	2	911166K	
R2		1k5	Metal Film	0.25	2	911166K	
R3		2k2	Metal Oxide	0.5	2	910984X	
R4		100M	Metal Film	0.25	5	943996Y	
R5		100M	Metal Film	0.25	5	943996Y	
R6		10R	Wire Wound, Vitreous Enamel	2.5	5	913571G	
R7		100M	Metal Film	0.25	5	943996Y	
R8		100M	Metal Film	0.25	5	943996Y	
R9		220M	Metal Film	0.25	5	943997P	
R10		68R	Wire Wound, Vitreous Enamel	2.5	5	913592B	
R11	B3	2k7	Thick Film Chip	0.125	2	943895Y	272
R12	C3	10k	Thick Film Chip	0.125	2	943902F	103
R13	C0	330R	Thick Film Chip	0.125	2	943884K	331
R14	C0	220k	Thick Film Chip	0.125	2	943918G	224
R15	C1	1k8	Thick Film Chip	0.125	1	945161U	182
R16	D0	6k8	Thick Film Chip	0.125	2	943900H	682
R17	C0	100k	Thick Film Chip	0.125	2	943914A	104
R18	C1	47R	Thick Film Chip	0.125	2	943873W	470
R19	E1	6k8	Thick Film Chip	0.125	1	945163S	682
R20	D0	27k	Thick Film Chip	0.125	2	943907S	273
R21	D1	22k	Thick Film Chip	0.125	2	943906B	223
R22	D0	22k	Thick Film Chip	0.125	2	943906B	223
R23	D0	10k	Thick Film Chip	0.125	2	943902F	103
R24	D0	33R	Thick Film Chip	0.125	2	943871Y	330
R25	E2	4k7	Thick Film Chip	0.125	1	945162B	472
R26	E2	4k7	Thick Film Chip	0.125	1	945162B	472
R27	E2	3k9	Thick Film Chip	0.125	2	943897W	392
R28	E2	1k	Thick Film Chip	0.125	2	943890L	102
R29	E3	33R	Thick Film Chip	0.125	2	943871Y	330
R30	E2	100k	Thick Film Chip	0.125	2	943914A	104
R31	E2	47R	Thick Film Chip	0.125	2	943873W	470
R32	E1	220k	Thick Film Chip	0.125	2	943918G	224
R33	E0	330R	Thick Film Chip	0.125	2	943884K	331
R34	E2	10k	Thick Film Chip	0.125	2	943902F	103
R35	E2	22R	Thick Film Chip	0.125	2	943869T	220
R36	F2	4k7	Thick Film Chip	0.125	1	945162B	472
R37	F3	22R	Thick Film Chip	0.125	2	943869T	220
R38	F2	10k	Thick Film Chip	0.125	2	943902F	103
R39	J1	22k	Thick Film Chip	0.125	2	943906B	223
R40	K0	6k8	Thick Film Chip	0.125	2	943900H	682
R41	K0	100k	Thick Film Chip	0.125	2	943914A	104
R42	K0	5k6	Thick Film Chip	0.125	2	943899E	562
R43	K2	330R	Thick Film Chip	0.125	2	943884K	331
R44	K2	10R	Thick Film Chip	0.125	2	943865X	100
R45	L1	100R	Thick Film Chip	0.125	2	943878J	101
R46	L1	10k	Thick Film Chip	0.125	2	943902F	103
R47	L1	120R	Thick Film Chip	0.125	2	943879Q	121
R48	L2	22R	Thick Film Chip	0.125	2	943869T	220
R49	N0	330R	Thick Film Chip	0.125	2	943884K	331
R50	P4	10k	Thick Film Chip	0.125	2	943902F	103
R51	P4	100k	Thick Film Chip	0.125	2	943914A	104
R52	P4	22R	Thick Film Chip	0.125	2	943869T	220
R53	R4	3k3	Thick Film Chip	0.125	2	943896P	332
R54	R4	10k	Thick Film Chip	0.125	2	943902F	103
R55	R3	10k	Thick Film Chip	0.125	2	943902F	103

Resistors				W			
R56	R4	10k	Thick Film Chip	0.125	2	943902F	103
R57	R4	150k	Thick Film Chip	0.125	2	943916I	154
R58	R3	10k	Thick Film Chip	0.125	2	943902F	103
R59	S4	680R	Thick Film Chip	0.125	2	943888G	681
R60	S4	100R	Thick Film Chip	0.125	2	943878J	101

Capacitors				V	
C1		220µ	Electrolytic	16	941843N
C2		220µ	Electrolytic	40	945005L
C3		100µ	Electrolytic	63	945179T
C4		6µ8	Electrolytic	63	945003N
C5		10µ	Electrolytic	63	943012F
C6		1M	Electrolytic	63	943307W
C7	B3	100n	Ceramic Chip	50	945146T
C8	D1	10n	Ceramic Chip	50	941775D
C9	D1	6µ8	Tantalum Chip	35	945052L
C10	E3	100n	Ceramic Chip	50	945146T
C11	F2	10n	Ceramic Chip	50	941775D
C12	J2	100n	Ceramic Chip	50	945146T
C13	J2	100n	Ceramic Chip	50	945146T
C14	J2	100n	Ceramic Chip	50	945146T
C15	J1	10n	Ceramic Chip	50	941775D
C16	K0	100n	Ceramic Chip	50	945146T
C17	K3	100n	Ceramic Chip	50	945146T
C18	L1	10n	Ceramic Chip	50	941775D
C19	N2	100n	Ceramic Chip	50	945146T
C20	P4	1µ	Tantalum Chip	35	945049Z
C21	P3	100n	Ceramic Chip	50	945146T
C22	P2	100n	Ceramic Chip	50	945146T
C23	P2	100n	Ceramic Chip	50	945146T
C24	R4	10n	Ceramic Chip	50	941775D

Diodes			
D1		BY225-100, Bridge Rectifier	945144V
D2		550-0406, LED Assembly	945143O
D3		550-0406, LED Assembly	945143O
D4		550-0406, LED Assembly	945143O
D5		550-0406, LED Assembly	945143O
D6		1N4002	923564Z
D7		1N4002	923564Z
D8		1N4002	923564Z
D9		BY225-100, Bridge Rectifier	945144V
D10		1N4002	923564Z
D11		1N4002	923564Z
D12	B3	BZX84-C30, Zener	945126P
D13	D1	BAS 16	943951D
D14	E2	BZX84-C18, Zener	945121C
D15	G1	BAS 16	943951D
D16	K0	BAS 16	943951D
D17	M2	BZX84-C 5V6, Zener	945109A

Thyristors

SCR1	S2800A, SCR	945527A
SCR2	S2800A, SCR	945527A

Transistors

TR1	Not used	
TR2	BD 677, NPN	945139L
TR3	BD 244B, PNP	945140Z
TR4	BD 677, NPN	945139L
TR5	BD 677, NPN	945139L
TR6	Not used	
TR7	BFY 51, NPN	908753E
TR8 P4	BC 849, NPN	943941W
TR9 R4	BC 849, NPN	943941W

Integrated Circuits

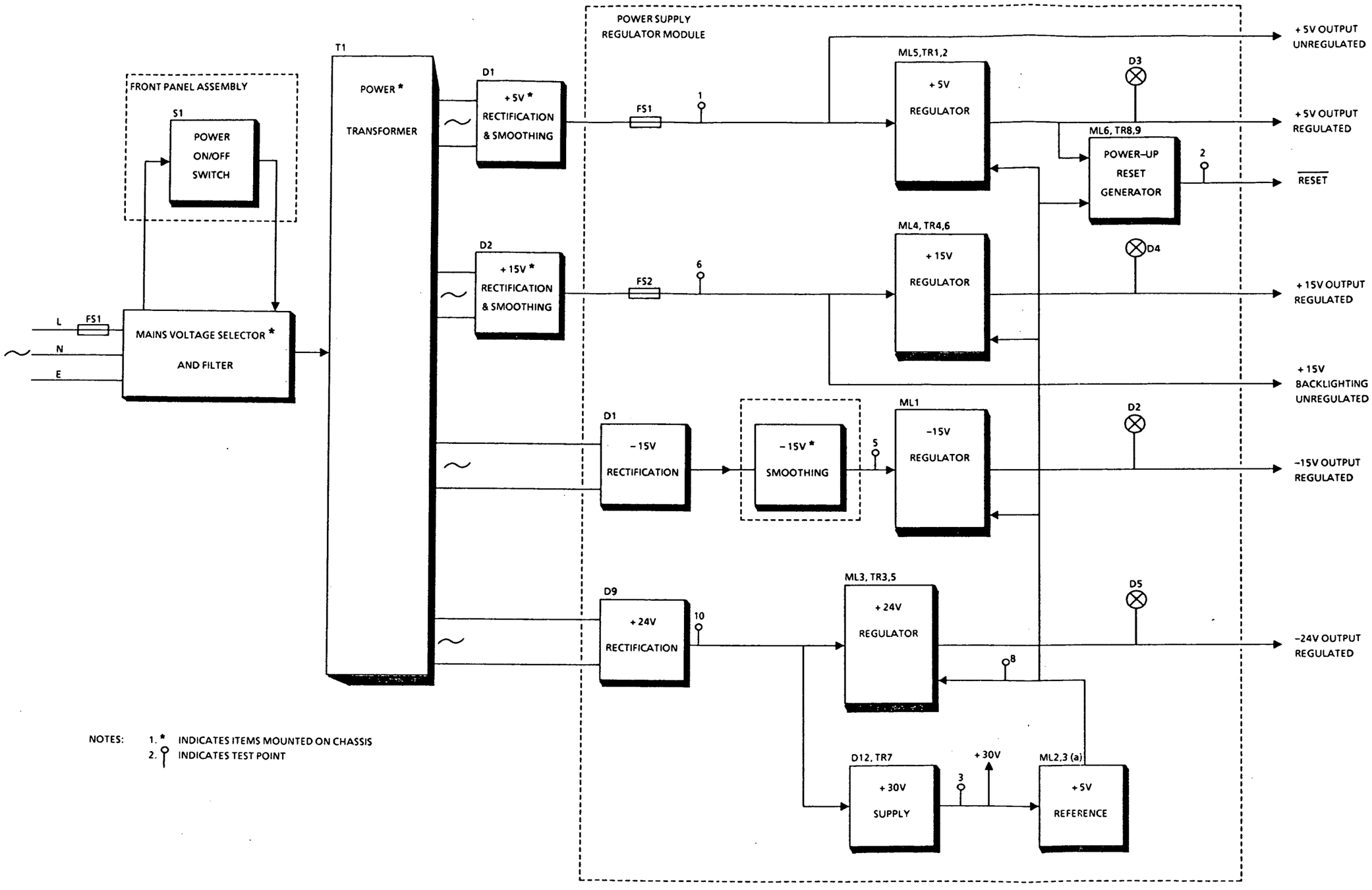
ML1	7915, -15V Regulator	939916B
ML2	02, +5V Reference	945021T
ML3 D0	324, Quad Operational Amplifier	945026G
ML4 F1	324, Quad Operational Amplifier	945026G
ML5 K0	324, Quad Operational Amplifier	945026G
ML6 R4	324, Quad Operational Amplifier	945026G

Connectors

PL1	Plug, 15-Way	945165Q
SK1	Socket, 25-Way	945166H

Miscellaneous

FS1	Fuse Link, 5 Amp	922453L
FS2	Fuse Link, 5 Amp	922453L
TP1 to TP10	Terminal, Assembly (test points)	936148X



NOTES: 1. * INDICATES ITEMS MOUNTED ON CHASSIS
2. ⚲ INDICATES TEST POINT

Power Supply: Block Diagram **Fig.12.2**

CHAPTER 13

CHASSIS ASSEMBLY

CONTENTS

ILLUSTRATIONS

CHAPTER 13

CHASSIS ASSEMBLY

INTRODUCTION

1 The Chassis Assembly supports both the Front Panel Assembly and the Power Supply Regulator Module and houses a motherboard into which a number of screened modules may be plugged. The use of an open frame construction permits easy access and replacement of modules, and allows the same frame to be configured with different modules according to the equipment application.

ASSEMBLY DESCRIPTION

Construction

2 The Chassis Assembly consists of two extruded aluminium side-members joined by cross rails which support the plug- in modules. The motherboard is supported in a similar way with its underside protected by a bottom cover.

3 Each module plugs vertically into a 64-way DIN connector on the motherboard and is held in place by two securing bolts to the cross- rails.

4 A sheet metal 'box' at the front of the assembly forms a compartment to house some power supply components and the optional Frequency Standard Module.

Mains Input

5 The Chassis Assembly houses the mains input and some rectification and smoothing components used by the power supply as shown in Fig. 13.1. These are also included in the module description for the Power Supply Regulator Module.

6 A mains voltage selector unit is mounted on the chassis behind the Power Supply Regulator Module and contains the mains input plug (PL1), an AC filter, a mains fuse (FS1) and a voltage selector drum. Both these latter items are accessible via a cover. The drum can be inserted in four different ways to select a mains input of 100, 120, 220 or 240 volts as required.

7 A torroidal power transformer plus the rectifiers and smoothing capacitors associated with the +5 V and +15 V supplies are mounted in the compartment at the front of the assembly.

Motherboard Connections

8 The Motherboard Circuit Diagram (Fig. 13.2) provided with this chapter shows that each plug-in socket is connected in the same way by means of a module bus. This bus provides all module interconnections which do not carry RF signals; these are made via miniature coaxial (SMB) connectors on the rear of the modules.

9 When the motherboard is installed in a dual receiver, switch SA provides isolation between the 1st IF and ISB AGC lines for each receiver to allow independent operation. The three switches (1 to 3) comprising switch SA are all set to ON for single receivers and all set to OFF for dual receivers.

FAULT FINDING

General

10 Fault finding on the motherboard consists of continuity and short circuit checks in accordance with the circuit diagram.

11 The power supply components mounted on the chassis are included with Power Supply Regulator Module for the purposes of fault finding.

PARTS LIST

12 The parts list for the Chassis Assembly is as follows:

BASIC CHASSIS (ST86480/001)

SK1	Connector, Socket, 5-Way	928267A
T1	Transformer	CT87105
TB2	Terminal Block, 16-Way	943995H
FS1	Fuse, 2A (mains)	922457H

CAPACITOR PLATE ASSEMBLY (ST86483)

Capacitors			V	
C1	22M	Electrolytic	25	945000Y
C5	15M	Electrolytic	63	943999N
C14	2M2	Electrolytic	63	940060X

Diodes

D1	26MB10A	930088S
D2	26MB10A	930088S

Terminals

TB1	Terminal Block, 12-way	923013Q

MOTHERBOARD (ST86483)

Switches

SA	Slide, DIL	945319Z

Connectors

SK1 to SK10	Socket, 64-Way	940340E

Cables

W1	Cable Assembly, 34-Way	BA87470
W2	Cable Assembly, 20-Way	BA87469
W3	Cable Assembly, 25-Way	BA87141

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
MAINS HOUSING ASSEMBLY (ST87229)							
Connectors							
PL1			Plug, 3-way			945138U	
Circuit Protection Devices				V			
VDR1			Suppressor, Metal Oxide	275		945055A	

CHAPTER 14

FREQUENCY STANDARD MODULE

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FREQUENCY STANDARD MODULE

INTRODUCTION

1 The Frequency Standard Module provides a 5 MHz reference signal of high accuracy and long term stability for use by the Reference/BFO Module.

2 Depending upon the degree of frequency stability required, one of three types of 5 MHz frequency standard may be fitted.

MODULE DESCRIPTION

3 The three types of frequency standard are described below and should be read in conjunction with the appropriate circuit diagram included in this chapter.

Frequency Standard Type 9442 (Fig. 14.1)

4 The Racal 9442 frequency standard is a fast warm-up crystal oscillator which provides a high degree of accuracy with long term stability and low power consumption. The crystal is housed in a temperature controlled oven which, together with a low excitation maintaining circuit and a buffer amplifier to minimise the effect of load changes, is fitted in a metal can with polyurethane foam to provide heat insulation. Mechanical setting of frequency is by a multi-turn control accessed through a hole in the top face of the oscillator can and a hole in the top cover of the receiver.

5 The oscillator supply voltage is derived from the Reference/BFO Module. This +15 V supply is routed via the 5 MHz output connector and stabilised at +12 V, using a 3-terminal voltage regulator mounted on the module, before application to the oscillator.

Frequency Standard Type 9420 (Fig. 14.2)

6 The Racal 9420 frequency standard is similar in construction to the 9442 but provides higher stability at the expense of a slightly longer warm-up time. A hole in the top of the can and in the top cover of the receiver, allows access to the internal multi-turn trimmer capacitor used for coarse frequency adjustment. Fine adjustment of frequency is achieved by means of a potentiometer external to the frequency standard and accessible through a hole in the side member of the receiver. The supply is stabilized by a 3-terminal voltage regulator as before.

Frequency Standard Type TCXO (Fig. 14.3)

7 The TCXO frequency standard is a temperature compensated crystal oscillator. The supply to the TCXO is also stabilized by a 3-terminal voltage regulator. A potentiometer external to the TCXO and accessible via a hole in the side member of the receiver, allows its frequency to be adjusted.

FAULT FINDING

8 Fault finding is limited to checking the operation of the components providing the stabilized supply voltage to the frequency standard. The frequency standard itself is not a user serviceable item and it should be replaced if found to be faulty.

ALIGNMENT

9 This procedure details the adjustments required for aligning the Frequency Standard Module.

10 **Test Equipment**

The following items of test equipment, as detailed in Chapter 2, are required for aligning the Frequency Standard Module:

(1) Frequency Counter.

(2) Reference frequency standard (accuracy ± 1 part in 10^9).

Frequency Adjustment

11 Ensure that the EXT/INT switch on the Reference/BFO Module is set to INT and the output frequency from the REF/BFO is switched to 10 MHz.

12 Ensure that the receiver has been running continuously for at least one hour with the internal frequency standard connected to the Reference/BFO Module.

13 Connect the counter input to the REF IN/OUT socket (SK1 on the Reference/BFO Module) on the receiver.

14 Connect the reference frequency standard to the external standard input on the counter and ensure that the counter is locked to this input.

15 Using the correct trimming tool, adjust the frequency control(s) until the frequency of the receiver reference output indicated on the counter is within the limits specified below for the frequency standard option fitted:

TCXO : 10 MHz ± 1 Hz
9442 : 10 MHz ± 0.03 Hz
9420 : 10 MHz ± 0.01 Hz

PARTS LIST

16 The parts lists for the various types of Frequency Standard Module are as follows:

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
FREQUENCY STANDARD 9442 (ST86497)							
Capacitors				V			
C1		1µ	Tantalum Chip	35		945049Z	
C2		1µ	Tantalum Chip	35		945049Z	
C3		10n	Ceramic Chip	50		941775D	
C4		10n	Ceramic Chip	50		941775D	
Inductor				W			
L1		10µH	Choke	0.2	10	922364Q	
Integrated Circuit							
ML1			7812, +12V Regulator			933987X	
Connector							
PL1			Plug, SMB			938429T	
Oscillator							
Y1			5 MHz Crystal			933706O	
FREQUENCY STANDARD 9420 (ST87243)							
Resistors							
R4		10k	Cermet, Variable, Linear		10	928362W	
Capacitors				V			
C1		1µ	Tantalum Chip	35		945049Z	
C2		1µ	Tantalum Chip	35		945049Z	
C3		10n	Ceramic Chip	50		941775D	
C4		10n	Ceramic Chip	50		941775D	
Inductor				W			
L1		10µH	Choke	0.2	10	922364Q	

Integrated Circuit

ML1	7812, +12V Regulator	933987X

Connector

PL1	Plug, SMB	938429T

Oscillator

Y1	5 MHz Frequency Standard	921601J

FREQUENCY STANDARD TCXO (ST86498)

Resistors

			W		
R1	220R	Thick Film Chip	0.125	1	945160D
R2	220R	Thick Film Chip	0.125	1	945160D
R3	680R	Thick Film Chip	0.125	2	943888G
R4	10 k	Cermet, Variable, Linear		10	928362W

Capacitors

			V		
C1	1µ	Tantalum Chip	35		945049Z
C2	1µ	Tantalum Chip	35		945049Z
C3	10n	Ceramic Chip	50		941775D
C4	10n	Ceramic Chip	50		941775D

Inductor

			W		
L1	10µH	Choke	0.2	10	922364Q

Integrated Circuit

ML2	317, +1.2/37V Regulator	945063J

Connector

PL1	Plug, SMB	938429T

Oscillator

Y2	TCXO	BD80789

CHAPTER 15

PROCESSOR MODULE (IEEE)

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PROCESSOR MODULE (IEEE)

INTRODUCTION

1 The Processor Module communicates with all modules connected to a module bus carried by the motherboard. It processes operational control settings to provide the necessary command signals for controlling various functions within these modules. The control settings may be received either from the Front Panel Assembly or via the IEEE-488 remote interface at the rear of the module.

Fig. 15.1 Receiver Block Diagram

2 The processing is performed by a 16-bit 68000 microprocessor supported by 256 kbytes of EPROM, 64 kbytes of RAM and 8 kbytes of EEPROM. Communication is via parallel interface/timers (PI/T), a dedicated IEEE-488 interface device and digital to analogue converters (DACs).

3 BITE programs stored in the EPROM allow the Processor to perform comprehensive tests of the receiver's performance. A signature analysis facility is also provided as a further aid to locating faults in the digital circuits to component level.

MODULE DESCRIPTION

4 The following description should be read in conjunction with the Processor Module Block and Circuit Diagrams included with this chapter. Component references shown on the Block Diagram allow it to be related to the Circuit Diagram.

Processor

5 The PROCESSOR fetches data either from the input or memory devices, processes the information according to program code stored in the EPROM, and then sends the results of these computations to an output or memory device. The PROCESSOR is driven from an 8 MHz CRYSTAL OSCILLATOR by means of which all its actions and those of the supporting devices are synchronised.

6 If desired, the internal clock for the PROCESSOR may be disabled by connecting ML27 pin 4 to 0 V via link LK2. This link may also be removed to permit the connection of an external clock source for test purposes.

Address Decoding

7 According to the status of address lines A18-22, the ADDRESS DECODER asserts the appropriate select line to allow the various on-board devices to communicate with the PROCESSOR, thereby ensuring that only the relevant data is routed to and from these devices. The ADDRESS DECODER is disabled by the 3-bit function code (FC0-3) during interrupts.

Internal Bus Structure

8 Address lines A1-17 form the ADDRESS BUS. This is used by the PROCESSOR to address the memory and interface devices to allow data transfer via a 16-bit bidirectional DATA BUS. This bus is split into two bytes (D0-7 and D8-15) and is interfaced to the PROCESSOR via a bidirectional DATA BUFFER. Data transfers are handled by control signals on the CONTROL BUS.

9 During data transactions, acknowledgement to the PROCESSOR that data transfer is completed is produced by the DTACK COUNTER to terminate the bus cycle.

Memory Devices

10 As well as providing storage for the main program, the EPROM contains the BITE program which is initiated at power-up, returning to the normal program on completion of testing. Included with the main program are the continuous BITE tests which are performed automatically without operator intervention. Signature analysis routines are also held in this memory.

11 Non-volatile storage of operational settings for up to 100 channels and power-down information containing the current front panel settings and receiver configuration is provided by the EEPROM, which requires no back-up battery supply. Data can be written into this memory when bit 7 of port B of PARALLEL I/O INTERFACE TIMER 2 is driven to active low. The current operational settings are updated if a change has occurred since they were last copied to the EEPROM, but only if they remain at these settings for more than one minute.

12 Two 32k by 8 static RAM devices form the RAM store. In addition to storing the front panel settings, it also serves as a working memory for storing intermediate results and computations during program execution. A back-up supply is provided by the charge held in C1 to provide short term data retention while the power is switched off.

13 If, for example, the power is momentarily interrupted, the front panel settings stored in the RAM are recalled when power is restored. The data is checked using a checksum and if it is uncorrupted, it is used as the receiver's operational settings. If the data in the RAM is corrupted, for example, because the supply has been switched off for some time, the data is taken from the EEPROM. A reset pulse generated in the Power Supply Regulator Module at power- up is used to disable the RAM until the supplies reach their rated values, thus avoiding data corruption.

Interface Devices

14 The PROCESSOR is interfaced to other modules in the equipment through the use of PARALLEL I/O INTERFACE TIMER 1. This bidirectional parallel interface provides a module bus for internal communication with all modules connected to it. It consists of an 8-bit address bus, an 8-bit data bus, read/write and strobe control lines, 3 interrupt lines, plus a BITE line for BITE measurements. A programmable event timer is also contained in this device for timing periodic events such as servicing the front panel shaft encoder or push buttons or updating the displays.

15 A second bidirectional parallel interface, PARALLEL I/O INTERFACE TIMER 2, mainly interfaces signals for the rear panel PARALLEL I/O 25-way connector (SK1) to allow the connection of external equipment. It is also used to read the status of seven DIL TEST SWITCHES. As before, a programmable timer is contained in this device. This acts as a 'watchdog timer' which applies a hardware reset unless it is serviced by the software at defined regular intervals.

16 Parallel data is also latched from the DATA BUS by DATA LATCH 1 and presented via OUTPUT DRIVERS as control signals for external equipment connected to SK1.

17 Interfacing with remotely-controlled equipment using the IEEE-488 standard is performed by a General Purpose Interface Adaptor (GPIA). This device is controlled by the PROCESSOR and handles the flow of transmitted and received data between the IEEE-488 remote link (through the TRANSCEIVERS) and the PROCESSOR. The TRANSCEIVERS provide the electrical interface for the data, management and control lines between the GPIA and the IEEE-488 standard 24-way connector (SK2) on the rear panel.

18 The IEEE-488 bus consists of 16 signal lines which are categorised into:

(1) 8 data lines used to transfer data and interface commands between equipments connected to the bus.

(2) 3 handshake lines which synchronise the transmission and reception of data and ensure that the transfer is correctly performed.

(3) 5 general interface management lines to carry interface commands which are used to control bus activity and maintain an orderly flow of data through the interfaces connected to it.

19 For a more detailed description of the remote interface, refer to ANSI/IEEE std. 488-1978. Further details are also provided in Chapter 5 of this manual.

20 Depending on the receiver version in which it is fitted, the PROCESSOR operates either as the controller of the remote system or as a slave.

21 The GPIA in a slave receiver both transmits and receives data in response to external interface commands on the management and data lines connected to the IEEE-488 remote link, via the BUFFERS and TRANSCEIVERS.

22 A PROCESSOR acting as the controller uses PARALLEL INTERFACE TIMER 2 to send a controlling interface command over one of the management lines to the IEEE-488 remote link, via the TRANSCEIVERS, in order to communicate with the GPIAs in the slave receivers. The processor also controls its own interface devices (BUFFERS, TRANSCEIVERS and GPIA).

23 Details of remote control operation are contained in Chapter 5 of the RA3700 Series Operators Manual. Chapter 6 of the Operators Manual gives typical system configurations. Details of programming the remote interface for operation with computer controlled systems are provided in Chapter 5 of this manual.

24 Three analogue control lines are derived by the digital to analogue conversion of parallel data presented to DAC 1 and DAC 2. Each DAC has a latched 8-bit digital input and an output range between 0 and 2.55 V in 10 mV steps. The DAC outputs are buffered by voltage followers.

25 The DAC 1 output is used for BITE metering while the DAC 2 output is used for setting the manual gain level. The DAC 3 output is derived from the DAC 1 output, which is strobed through a DAC 3 SAMPLE AND HOLD CIRCUIT by bit 3 of port B of PI/T 1 to provide a periodic refresh. The DAC 3 output is only used in the dual receiver versions to provide the manual gain setting for the second receiver.

26 Two internal interrupt lines (IPL0 and IPL1) are also provided on the Processor Module. The IPL1 line has the higher priority and is connected to the GPIA device. The IPL0 line is connected to both PI/T devices and deals with general purpose timer interrupts and external interrupts from the scan inhibit inputs at the PARALLEL I/O connector.

Test Facilities

27 The seven DIL TEST SWITCHES provide access to various test facilities including manually initiated BITE tests and signature analysis. According to the desired operating mode, the switches are set to the positions shown in Table 15.1 and their status read via PI/T 1 at power-up.

TABLE 15.1

Test Switch Positions

Function Selected	Switch No.			
	5	6	7	8
Normal Operation	ON	ON	ON	ON
Receiver Default Set-up	OFF	ON	ON	ON
Unit Confidence Test	ON	OFF	ON	ON
Signature Analysis	ON*	ON*	OFF	ON
Processor Free-Run (Signature Analysis)	OFF	OFF	OFF	OFF

* Dependent on selected signature analysis routine

28 On a slave receiver (RA3703/RA3704) the DIL TEST SWITCHES allow the unit confidence test to be run locally. This facility may also be used on a receiver where a fault prevents the unit confidence test being run from the front panel via the menu system.

29 The DIL TEST SWITCHES also allow the PROCESSOR to operate in a free-run mode. With switch 8 set to OFF, the PROCESSOR data bus is isolated from the rest of the circuit and a test data word is injected into the PROCESSOR causing it to execute a one-word instruction. This instruction is continually stepped through the entire address range to create a repetitive data pattern and allow signature analysis to be performed on the Processor and associated circuitry within the Processor Module.

30 Normally in the initial power-up mode, switches 1 to 4 have no significance. However if signature analysis has been entered, switches 1 to 7 are then used to enter and execute the various signature analysis routines stored in the EPROM. In addition to checking the Processor Module, these routines check the module bus on the motherboard and the digital circuitry of any other module connected to it. Further details of signature analysis, are contained in Chapter 3.

31 A 3-digit, 7-segment LED DISPLAY is used for test purposes. It is driven by parallel data latched into DATA LATCH 2 and controlled by three lines taken from the data output of DATA LATCH 1. The display is primarily used to show BITE test faults as some faults may prevent the front panel displays from being used. If a failure occurs the LED DISPLAY flashes its BITE test number

BITE Measurement System

32 The BITE Measurement System enables the PROCESSOR to measure the supply voltages and check the analogue outputs of DAC 2 and DAC 3 by comparing them with the output of DAC 1.

33 It comprises of an ANALOGUE MULTIPLEXER operating in conjunction with a BITE COMPARATOR. The voltage to be measured is selected by the ANALOGUE MULTIPLEXER which is controlled by three lines taken from Port C of PI/T2. This selected voltage is then compared in the BITE COMPARATOR with a test voltage established on the DAC 1 line. The resulting output is read by the PROCESSOR via PI/T 1.

34 To enable BITE measurements to be performed in the other modules of the receiver, the DAC 1 line is taken to a BITE comparator in each of these modules. All comparator outputs are connected to an open- collector BITE return line whose status is also read by the PROCESSOR via PI/T 2.

SOFTWARE PROGRAM IDENTIFICATION

35 Using the menu system, the issue of the software program residing in the EPROM may be identified as follows:

(1) Press MENU until the following level 6 options are presented on the right-hand display:

BW	SERIAL	FREQ	S/W
	PORTS	RES	ID

(2) Press M4 to select the S/W ID option and the security code prompt appears.

(3) Enter the receiver security code and the following menu is presented:

SERIAL	S/W
NUMBER	ISSUE

(4) Press M3 to select S/W ISSUE and display the software issue number.

(5) Press M4 to exit back to level 6 options or press RCL to revert back to the receiver operating conditions.

RECEIVER SERIAL NUMBER IDENTIFICATION

36 Using the menu system, the serial number of the receiver is programmed into the EPROM so that it may be identified from the front panel. This facility would be of use in a rack-mounted receiver where the internally-mounted serial number plate is not visible. In the event of the Processor Module being replaced, this facility allows the serial number to be re-entered into the new module. The procedure is as follows:

(1) Carry out the previous procedure for identifying the software issue until the following menu is presented:

SERIAL	S/W
NUMBER	ISSUE

(2) Press M1 to select the SERIAL NUMBER option and the current serial number, if any, is displayed.

(3) Key in the receiver serial number required and press ENTER. The display reverts back to the level 6 options.

(4) Press RCL to revert back to the receiver operating conditions.

FAULT FINDING

General

37 Fault finding techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the Processor Module is contained in the following sections.

BITE Tests

38 The following BITE tests for the Processor Module are arranged in the order in which they are performed or presented for selection.

TEST NUMBER	:	001
TITLE	:	Checksum PD1
PERFORMED	:	Power-up
DESCRIPTION	:	Performs a 16-bit checksum on the EPROM fitted to the PD1 position on the Processor Module. PD1 is indicated as being faulty if the result does not agree with the expected checksum.
FAULT DIRECTORY	:	Fault No. 5

TEST NUMBER	:	002
TITLE	:	Checksum PD2
PERFORMED	:	Power-up
DESCRIPTION	:	As previous BITE test but checks the EPROM fitted to the PD2 position.
FAULT DIRECTORY	:	Fault No. 5

TEST NUMBER	:	003
TITLE	:	RAM test ML12
PERFORMED	:	Power-up
DESCRIPTION	:	Checks the RAM fitted to position ML12 on the Processor Module by writing and reading the following data patterns into the first 32K bytes: all 0's all 1's, walking 0's walking 1's and (except at power-up) a test of the independence of the address lines.
FAULT DIRECTORY	:	Fault No. 5

TEST NUMBER	:	004
TITLE	:	RAM test ML11
PERFORMED	:	Power-up
DESCRIPTION	:	As previous BITE test but checks the RAM fitted to the ML11 position, which provides the second 32K bytes.
FAULT DIRECTORY	:	Fault No. 5

TEST NUMBER	:	005
TITLE	:	EEPROM test
PERFORMED	:	Power-up
DESCRIPTION	:	Checks the data residing in the EEPROM at power-up against the corresponding checksums. A failure to program the EEPROM during normal operation also causes the test number to be displayed on the Processor Module displays.
FAULT DIRECTORY	:	Fault No. 8

TEST NUMBER : 006, 007, 008, 009

TITLE : +5V rail, +15V rail, -15V rail, +24V rail.

PERFORMED : Power-up, unit confidence test, select test.

DESCRIPTION : The appropriate power supply test voltage is selected at the Processor Module and checked.

LIMITS :

Test No.	Supply	Mux I/P	Mux Limits	
			Lower	Upper
006	+5 V	×2	1.78V	2.22V
007	+15 V	×4	1.70V	2.21V
008	-15 V	×6	1.65V	2.24V
009	+24 V	×5	1.73V	2.45V

FAULT DIRECTORY : Fault No. 7

TEST NUMBER : 011

TITLE : DAC test

PERFORMED : Power-up, unit confidence test, select test.

DESCRIPTION : This test checks that the DAC 1 (BITE measurement system) and DAC 2 (IF gain) analogue outputs track to 1 bit across their operating ranges.

FAULT DIRECTORY : Fault No. 10

TEST NUMBER : 012

TITLE : Processor I/O

PERFORMED : Select test.

DESCRIPTION : This test causes the 4-bit antenna output on SK1 and the DAC 1 and DAC 2 outputs to ramp continuously, thus exercising every value. The test will always pass as it is intended for fault finding with the use of additional test equipment.

TEST NUMBER	:	013
TITLE	:	Parallel I/O 1
PERFORMED	:	Select test.
DESCRIPTION	:	The test partially checks the parallel I/O signal lines to the 25-way connector (SK1) on the Processor Module. It requires the use of the external parallel loopback 1 connector to interconnect the following: ANT 0 to AUX 0 ANT 1 to AUX 1 ANT 2 to AUX 2 ANT 3 to AUX 3 COR 1 to MUTE 1 All combinations of bits are tested to ensure that all lines can be driven and read correctly without any crosstalk.
FAULT DIRECTORY	:	Fault No. 11

TEST NUMBER	:	013
TITLE	:	Parallel I/O 2
PERFORMED	:	Select test.
DESCRIPTION	:	Similar to previous test but checks the remainder of the parallel I/O signal lines to SK1 using the parallel loopback 2 connector to interconnect the following: ANT 0 to SCAN INHIBIT 1 ANT 1 to SCAN INHIBIT 2 ANT 2 to DUMP 1 ANT 3 to DUMP 2 COR 2 to MUTE 2
FAULT DIRECTORY	:	Fault No. 11

TEST NUMBER	:	101
TITLE	:	RX data bus.
PERFORMED	:	Power-up.
DESCRIPTION	:	Checks that the parallel interface (PI/T 1) to the receiver modules can drive the data bus. A walking '1' pattern is placed on the data bus and read back into the PI/T such that instantaneous levels are obtained. Short circuits on the data bus are detected by this method.
FAULT DIRECTORY	:	Fault No. 2

TEST NUMBER	:	102
TITLE	:	RX address bus.
PERFORMED	:	Power-up.
DESCRIPTION	:	Checks the receiver address bus as in test 101.
FAULT DIRECTORY	:	Fault No. 2

TEST NUMBER	:	103
TITLE	:	RX bus control.
PERFORMED	:	Power-up.
DESCRIPTION	:	Checks the signals used to control the flow of data on the RX bus. The RX bus strobe line is checked by reading it at the RX bus R/W line and vice versa.
FAULT DIRECTORY	:	Fault No. 2

TEST NUMBER	:	104
TITLE	:	RX BITE line.
PERFORMED	:	Power-up.
DESCRIPTION	:	Checks that no module's BITE circuit asserts the BITE line when their multiplexers are all deselected. DAC1 line is set to 160 mV to allow even a low voltage at a module's multiplexer output to be detected.
FAULT DIRECTORY	:	Fault No. 4

Fault Directory

39 Use the following fault directory to identify the fault condition and take the necessary corrective action. The Processor Module relies heavily on signature analysis as a means of tracing faults to component level. Note that all inputs to the module are assumed to be correct, including the power supplies.

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
1	No response to any control setting, displays blank, and no number displayed on Processor Module LED's	(a) Master clock inoperative. (b) Reset permanently activated. (c) Processor, address decode or address bus fault. (d) Data bus or EPROM fault.	(a) Check TP3 for 8 MHz. square wave (CMOS levels). (b) Check status of Processor reset line. (c) Check supplies to Processor and carry out free-run signature analysis routine. (d) Carry out free-run signature analysis routine 0.
2	As above but LED's display a number (see Table 3.1 , Chap.3).	Module bus parallel I/O interface faulty.	Use signature analysis routine 6 to locate fault around PI/T 2.
3	Unable to update displayed operational settings.	(a) Parallel I/O event timer or processor interrupts faulty. (b) Faulty RAM. (c) Faulty EPROM.	(a) Use signature analysis routine 5 to locate fault. (b) See Fault No. 1. (c) See Fault No. 5.
4	Receiver responds to controls but BITE indicates multiple faults.	(a) BITE hardware fault. (b) DAC 1 inoperative.	(a) Check action of BITE comparator/ multiplexer using signature analysis routine 4. (b) See Fault No. 11.
5	Incorrect response to control settings.	(a) EPROM faulty. (b) Faulty PI/T 1. (c) RAM faulty.	(a) Select BITE tests 001 and 002 to confirm whether PD1 or PD2 is faulty. (b) See Fault No. 2. (c) Check ML11 and ML12 using BITE tests 003 and 004. Use signature analysis routine 0.
6	No indication on Processor Module LEDs but receiver appears to operate normally.	LED display or data latches faulty.	Use signature analysis routine 6 to locate fault.
7	Power supply rails fail BITE test (Power Supply Regulator Module assumed serviceable).	BITE hardware fault.	Check inputs to analogue multiplexer and refer to Fault No. 4.
8	Unable to program channels or retain operating settings when receiver is switched off for a long period.	EEPROM or address decode faulty.	Check ML6 using BITE test 005 and signature analysis routine 2.
9	If power is momentarily interrupted, changes to operating settings made within the last minute are not stored.	(a) RAM back-up supply faulty. (b)RAM faulty.	(a) Check C1 is being charged via TR8. (b) Check ML11 and ML12 using BITE tests 003 and 004. Use signature analysis routine 0.
10	No manual gain control.	DAC 2 inoperative.	Select BITE test 012 and check for a sawtooth waveform of between 0 V and 2.55 V on DAC output. Use signature analysis routine 4 to check digital inputs.

Fault Directory (continued)

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
11	No response to one or more signal I/O connections to SK1 (parallel I/O).	Parallel I/O interface (PI/T2) faulty.	Select BITE tests 013 and 014 to check all I/O lines. Check chip enable on TP7.
12	No response to scan inhibit inputs.	(a) Parallel I/O interface faulty (b) Processor interrupts absent.	(a) See Fault No. 11. (b) Use signature analysis routine 6 to check SCAN INHIBIT inputs.

Signature Analysis Routines

40 ROUTINE FREE-RUN

This routine checks the fundamental operation of the Processor address bus and address decoding.

Processor Module DIL switch settings: SW8 OFF
SW1-7 ON

Signature Analyser connections and settings:

Start: A23 (ML4/52) Processor Module, negative trigger
Stop: A23 (ML4/52) Processor Module, negative trigger
Clock: TP3 Processor Module, positive trigger
Earth: TP2 Processor Module

Note : Signatures xxxxF signify a flashing probe indicator.

Signal	Signature	Test Node						Remarks
+5V	H3UH	ML4/49	ML4/14					
0V	0000	TP2	ML4/16	ML4/53				
CLK	0000F	XL1/8	LK2/1	LK2/2	ML27/4	ML22/2		
AS	379H	ML4/6	TP9	ML27/6	ML18/4	ML17/1		
UDS	379H	ML4/7	ML17/10	ML14/9				
LDS	379H	ML4/8	ML17/4	ML14/1	ML14/13			
R/(W)	H3UH	ML4/9	ML27/17	ML14/5	ML8/43	ML20/1	ML19/1	
	ML7/43	ML14/12	ML14/10					
(R)/W	0000	ML27/3	PD1/20	PD2/20	ML2/22	ML11/22	ML12/22	
		ML27/1	ML27/15					
RESET	H3UH	ML26/8	ML27/20	ML4/18	ML4/17	ML7/39		
IPL0	H3UH	ML16/8	ML4/25					
IPL1	H3UH	ML16/11	ML4/24					
FC0	0000	ML4/28	ML16/1					
FC1	HU3H	ML4/27	ML16/2					
FC2	HU3H	ML4/26	ML16/13					
ML16/12	HU3H	ML16/12	ML18/6	ML26/3				
VPA	UAU7	ML17/3	ML4/21	ML22/7				
A1	PH02	ML4/29	ML8/29	ML12/10				
	ML7/29	PD2/21	ML2/10	PD1/21				
A2	CU97	ML4/30	ML8/28	ML12/9				
	ML7/28	PD2/22	PD1/22	ML2/9				

Signature Analysis Routines (continued)

Signal	Signature	Test Node				Remarks
A3	09PF	ML4/31	ML8/27	ML2/8	ML7/27	
		PD1/23	PD2/23			
A4	C571	ML4/32	ML8/26	ML2/7	ML7/26	
		PD1/24	PD2/24			
A5	5149	ML4/33	ML8/25	ML7/25	ML2/6	
		PD1/25	PD2/25			
A6	4126	ML4/34	ML2/5	PD1/26	PD2/26	
A7	348F	ML4/35	ML2/4	PD1/27	PD2/27	
A8	8P92	ML4/36	ML2/3	PD1/28	PD2/28	
A9	P1F4	ML4/37	ML2/25	PD1/29	PD2/29	
A10	UA57	ML4/38	ML2/24	PD1/31	PD2/31	
A11	062P	ML4/39	ML2/21	PD1/32	PD2/32	
A12	69HA	ML4/40	ML2/23	PD1/33	PD2/33	
A13	HHUC	ML4/41	ML2/2	PD1/34	PD2/34	
A14	A312	ML4/42	ML2/26	PD1/35	PD2/35	
A15	1030	ML4/43	PD1/36	PD2/36		
A16	1191	ML4/44	PD1/37	PD2/37		
A17	0HU4	ML4/45	PD1/38	PD2/38		
A18	CU97	ML4/46	ML15/2	ML15/14		
A19	1U1C	ML4/47	ML15/3	ML15/13		
A20	U487	ML4/48	ML18/1			
A21	P726	ML4/50	ML18/2			
A22	91U8	ML4/51	ML18/3			
A23	FH01	ML4/52	ML22/3			
DTACK	91U4	ML27/12	ML4/10			
ML27/14	P460	ML27/14	ML22/9			
RAM R/(W)	H3UH	ML14/11				
RAM (R)/W	H3UH	ML14/8				
EE R/W	H3UH	ML14/3	ML2/27			
PD1 CE	7413	ML18/15	PD1/2			
PD2 CE	0A8U	ML18/14	PD2/2			
E CE	A1CF	ML18/13	ML2/20			
RAM CE	7P41	ML18/12	ML30/1	ML30/2		
ML18/11	FU32	ML18/11	ML17/5	ML17/9		
ML17/6	FU32	ML17/6	ML15/1			
ML17/8	FU32	ML17/8	ML15/15			
A	CCC3	ML15/4	TP7	ML8/41		
B	UAU7	ML15/5				
C	8726	ML15/6	ML13/11			
D	HAAH	ML15/7	ML24/4			
E	CCC3	ML15/12	ML7/41			
F	UAU7	ML15/11				
G	8726	ML15/10	ML25/11			
H	HAAH	ML15/9	ML23/4			

Signature Analysis Routines (continued)

ROUTINE 0

This routine checks the RAM and the data read into the Processor via the Data Buffer.

Processor Module DIL switch setting: SW7 OFF
SW1-6,8 ON

Start: TP7 Processor Module, negative trigger
Stop: TP7 Processor Module, negative trigger
Clock: TP9 Processor Module, positive trigger
Earth: TP2 Processor Module

NOTE: The gating period is approximately 5 seconds for this test, therefore allow sufficient time for signatures to settle.

Signal	Signature	Test Node						Remarks
RAM 5V	5883	ML11/28	ML12/28	ML30/14				
RAM 0V	0000	ML11/14	ML12/14					
CE	05PP	ML11/20	ML12/20	ML30/1	ML18/12			
OE	34PF	ML11/22	ML12/22	ML27/3				
WE(L)	6F6U	ML11/27	ML14/11					
WE(U)	6F6U	ML12/27	ML14/8					
DO	836F	ML4/5	ML20/18	ML20/2	ML11/11	PD1/19	PD2/19	
D1	HA5C	ML4/4	ML20/17	ML20/3	ML11/12			
D2	0C85	ML4/3	ML20/16	ML20/4	ML11/13			
D3	9714	ML4/2	ML20/15	ML20/5	ML11/15			
D4	AOUF	ML4/1	ML20/14	ML20/6	ML11/16			
D5	C769	ML4/64	ML20/13	ML20/7	ML11/17			
D6	0480	ML4/63	ML20/12	ML20/8	ML11/18			
D7	SHUA	ML4/62	ML20/11	ML20/9	ML11/19			
D8	P694	ML4/61	ML19/18	ML19/2	ML12/11			
D9	9H0F	ML4/60	ML19/17	ML19/3	ML12/12			
D10	90A6	ML4/59	ML19/16	ML19/4	ML12/13			
D11	783P	ML4/58	ML19/15	ML19/5	ML12/15			
D12	8U47	ML4/57	ML19/14	ML19/6	ML12/16			
D13	P371	ML4/56	ML19/13	ML19/7	ML12/17			
D14	C6HU	ML4/55	ML19/12	ML19/8	ML12/18			
D15	4712	ML4/54	ML19/11	ML19/9	ML12/19			

Signature Analysis Routines (continued)

ROUTINE 1

This routine checks the LED Display and associated data latches.

Processor Module DIL switch settings: SW7,1 OFF
SW2-6,8 ON

Signature Analyser connections and settings:

Start: TP7 Processor Module, negative trigger
Stop: TP7 Processor Module, negative trigger
Clock: TP9 Processor Module, positive trigger
Earth: TP2 Processor Module

Signal	Signature	Test Node				Remarks
+5V	63A3	ML25/20	ML13/20			
OE/OV	0000	ML25/1	ML25/10	ML13/1	ML13/10	
LDS	5P5H	ML4/8	ML17/4			
ML17/6	C213	ML17/6	ML15/1			
C	P061	ML15/6	ML13/11			
G	3HUP	ML15/10	ML25/11			
UDS	H1C0	ML4/7	ML17/10			
ML17/8	3HUP	ML17/8	ML15/15			
a	U10P	ML13/2	R58			
b	6825	ML13/5	R56			
c	96P3	ML13/6	R54			
d	9F9U	ML13/9	R52			
e	5P42	ML13/12	R57			
f	4P8U	ML13/15	R55			
g	53F0	ML13/16	R53			
dp	5139	ML13/19	R51			
C3	U314	ML25/15	ML1/1			
C2	89FU	ML25/16	ML1/4			
C1	7AHC	ML25/19	ML1/7			

Signature Analysis Routines (continued)

ROUTINE 2

This routine checks the EEPROM.

WARNING: The contents of the EEPROM will be corrupted when this routine is run.

Processor Module DIL switch settings: SW7,2 OFF
SW1,3-6,8 ON

Signature Analyser connections and settings:

Start: TP7 Processor Module, negative trigger
Stop: TP7 Processor Module, negative trigger
Clock: TP9 Processor Module, positive trigger
Earth: TP2 Processor Module

Signal	Signature	Test Node	Remarks
+5V	481P	ML2/28	
0V	0000	ML2/14	
CE	2P2F	ML18/13 ML2/20	
DO	HP27	ML2/11	
D1	8PP4	ML2/12	
D2	8A11	ML2/13	
D3	159F	ML2/15	
D4	U49U	ML2/16	
D5	1354	ML2/17	
D6	3UH2	ML2/18	
D7	85FH	ML2/19	

Signature Analysis Routines (continued)

ROUTINE 3

This routine checks that the Processor can communicate with the receiver module bus via PI/T1.

Processor Module DIL switch settings: SW7,1,2 OFF
SW3-6,8 ON

Signature Analyser connections and settings:

Start: TP7 Processor Module, negative trigger
Stop: TP7 Processor Module, negative trigger
Clock: TP9 Processor Module, positive trigger
Earth: TP2 Processor Module

Signal	Signature	Test Node		Remarks
+5V	5HHC	ML7/12		
0V	0000	ML7/38		
CE	U61P	ML15/12	ML7/41	
RESET	5HHC	ML7/39		
R/W	936A	ML7/43		
PIRQ	5HHC	ML7/35	ML7/33	
D8	3900	ML7/44		
D9	7H75	ML7/45		
D10	9C5U	ML7/46		
D11	4056	ML7/47		
D12	PA1U	ML7/48		
D13	323P	ML7/1		
D14	8AU4	ML7/2		
D15	14AP	ML7/3		
A1	C033	ML7/29		
A2	2180	ML7/28		
A3	5C85	ML7/27		
A4	6H65	ML7/26		
A5	U6U1	ML7/25		
PC1	314F	ML7/31	ML27/11	
PC2	P0C2	ML7/30	ML27/13	
PC4	3UPP	ML7/34		
PC6	P9UU	ML7/36		
PC7	28H4	ML7/37		
M-WR	C224	ML27/9	PL1/8B	
M-STB	H905	ML27/7	PL1/8A	
M-A0	019H	ML7/4	PL1/12A	
M-A1	A3C9	ML7/5	PL1/12B	
M-A2	UPA8	ML7/6	PL1/11A	
M-A3	UF40	ML7/7	PL1/11B	
M-A4	C6FF	ML7/8	PL1/10A	
M-A5	1757	ML7/9	PL1/10B	
M-A6	4C0B	ML7/10	PL1/9A	
M-A7	1783	ML7/11	PL1/9B	
M-D0	78P9	ML7/17	PL1/7A	
M-D1	ACA6	ML7/18	PL1/7B	
M-D2	453F	ML7/19	PL1/6A	
M-D3	C248	ML7/20	PL1/6	
M-D4	F3U3	ML7/21	PL1/5A	
M-D5	864P	ML7/22	PL1/5B	
M-D6	UF53	ML7/23	PL1/4A	
M-D7	3758	ML7/24	PL1/4B	

Signature Analysis Routines (continued)

ROUTINE 4

This routine checks that the data lines to the DACs and IEEE controller.

Processor Module DIL switch settings: SW7,3 OFF
SW1,2,4-6,8 ON

Signature Analyser connections and settings:

Start: TP7 Processor Module, negative trigger
Stop: TP7 Processor Module, negative trigger
Clock: TP9 Processor Module, positive trigger
Earth: TP2 Processor Module

Signal	Signature	Test Node		Remarks
+5V	PU58	ML23/10	ML24/10	
0V	0000	ML23/9	ML24/9	
D0	HA74	ML24/2		
D1	9A90	ML24/1		
D2	U6H8	ML24/16		
D3	5736	ML24/15		
D4	9391	ML24/14		
D5	HA49	ML24/13		
D6	05U5	ML24/12		
D7	3P80	ML24/11		
D8	U762	ML23/2		
D9	904H	ML23/1		
D10	F252	ML23/16		
D11	7F13	ML23/15		
D12	8AF5	ML23/14		
D13	9432	ML23/13		
D14	F8HC	ML23/12		
D15	H9UU	ML23/11		

Signature Analysis Routines (continued)

ROUTINE 5

This routine checks PI/T 2 watchdog timer/reset and the PI/T 1 event timer.

Processor Module DIL switch settings: SW7,1,3 OFF
SW2,4-6,8 ON

Signature Analyser connections and settings:

Start: ML4/17 negative trigger
Stop: ML4/18 negative trigger
Clock: TP9 Processor module, positive trigger
Earth: TP2 Processor Module

Signal	Signature	Test Node					Remarks
+5V	A544	ML8/12					
0V	0000	ML8/38					
D0	P11C	ML8/44	ML20/2				
D1	89AF	ML8/45	ML20/3				
D2	P78P	ML8/46	ML20/4				
D3	C263	ML8/47	ML20/5				
D4	6HC7	ML8/48	ML20/6				
D5	0UC4	ML8/1	ML20/7				
D6	AU01	ML8/2	ML20/8				
D7	FFC6	ML8/3	ML20/9				
A1	5HA7	ML8/29	ML4/29				
A2	U999	ML8/28	ML4/30				
A3	395H	ML8/27	ML4/31				
A4	4FAF	ML8/26	ML4/32				
A5	4A70	ML8/25	ML4/33				
IPLO(PIT)	2FP3	ML7/33	ML7/35	ML21/11	ML8/35		
ML21/10	89A7	ML21/10	ML16/10				
ML16/9	A544	ML16/9					
IPL1	A544	ML4/24	ML16/11				
IPLO	2FP3	ML16/8	ML4/25				
TOUT	H2A2	ML8/33	ML26/10				
R	H2A2	ML26/8	ML7/39	ML22/1	ML4/18	ML4/17	
SA1	A544	ML8/4					
SA2	0000	ML8/5					
SA3	A544	ML8/6					
SA4	0000	ML8/7					
SA5	0000	ML8/8					
SA6	0000	ML8/9					
SA7	A544	ML8/10					

Signature Analysis Routines (continued)

ROUTINE 6

This routine checks the parellel output line data latch.

NOTE: The Processor Module LED displays 666.

Processor Module DIL switch settings: SW7,3,2 OFF
SW1,4,5,6,8 ON

Signature Analyser connections and settings:

Start: ML7/41 Processor Module, negative trigger
Stop: ML7/41 Processor Module, negative trigger
Clock: TP9 Processor Module, positive trigger
Earth: TP2 Processor Module

Signal	Signature	Test Node	Remarks
+5V	848F	ML8/12	
0V	0000	ML8/38	
ML25/2	465U	ML25/2	
ML25/5	PUPC	ML25/5	
ML25/6	9HCU	ML25/6	
ML25/12	1PUF	ML25/12	

PARTS LIST

41 The Racal part number for a complete IEEE-488 Processor Module is ST87649.

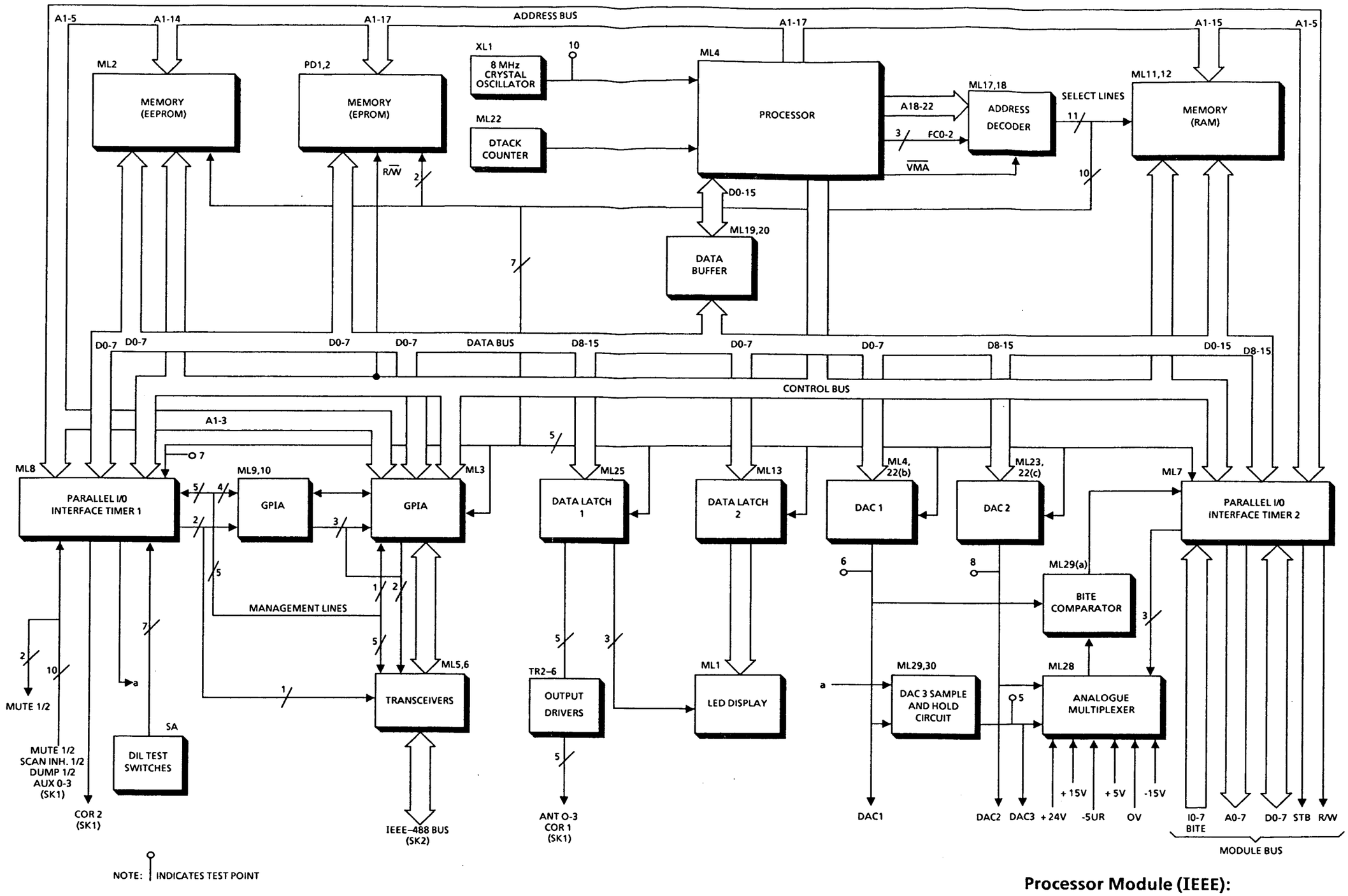
42 Information on the identification and handling of SMDs is provided in Chapter 2. The parts list for the Processor Module is as follows:

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R1		10k	Thick Film Network			934506N	
R2		10k	Thick Film Network			934506N	
R3		10k	Thick Film Network			934506N	
R4		3k3	Thick Film Network			939677T	
R5		10k	Thick Film Network			934506N	
R6		1k	Thick Film Network			940019R	
R7		1k	Thick Film Network			940019R	
R8		10k	Thick Film Network			934506N	
R9	D9	10k	Thick Film Chip	0.125	2	943902F	103
R10	D4	1k	Thick Film Chip	0.125	2	943890L	102
R11	D4	1k	Thick Film Chip	0.125	2	943890L	102
R12	D4	2k2	Thick Film Chip	0.125	2	943894R	222
R13	D3	2k2	Thick Film Chip	0.125	2	943894R	222
R14	D3	2k2	Thick Film Chip	0.125	2	943894R	222
R15	D3	2k2	Thick Film Chip	0.125	2	943894R	222
R16	D2	2k2	Thick Film Chip	0.125	2	943894R	222
R17	D2	2k2	Thick Film Chip	0.125	2	943894R	222
R18	D1	2k2	Thick Film Chip	0.125	2	943894R	222
R19	D1	2k2	Thick Film Chip	0.125	2	943894R	222
R20	D1	2k2	Thick Film Chip	0.125	2	943894R	222
R21	D0	2k2	Thick Film Chip	0.125	2	943894R	222
R22	D8	10k	Thick Film Chip	0.125	2	943902F	103
R23	E8	10k	Thick Film Chip	0.125	2	943902F	103
R24	E8	10k	Thick Film Chip	0.125	2	943902F	103
R25	E1	2k2	Thick Film Chip	0.125	2	943894R	222
R26	F1	2k2	Thick Film Chip	0.125	2	943894R	222
R27	F1	2k2	Thick Film Chip	0.125	2	943894R	222
R28	F1	2k2	Thick Film Chip	0.125	2	943894R	222
R29	F1	2k2	Thick Film Chip	0.125	2	943894R	222
R30	F1	2k2	Thick Film Chip	0.125	2	943894R	222
R31	H1	10k	Thick Film Chip	0.125	2	943902F	103
R32	H1	3k3	Thick Film Chip	0.125	2	943896P	332
R33	J1	3k3	Thick Film Chip	0.125	2	943896P	332
R34	M1	22k	Thick Film Chip	0.125	2	943906B	223
R35	N1	120k	Thick Film Chip	0.125	2	943915R	124
R36	N3	15k	Thick Film Chip	0.125	2	943904D	153
R37	N1	18k	Thick Film Chip	0.125	2	943905K	183
R38	N3	10k	Thick Film Chip	0.125	2	943902F	103
R39	N1	18k	Thick Film Chip	0.125	2	943905K	183
R40	N3	10k	Thick Film Chip	0.125	2	943902F	103
R41	N1	100k	Thick Film Chip	0.125	2	943914A	104
R42	N3	39k	Thick Film Chip	0.125	2	943909Q	393
R43	P1	10k	Thick Film Chip	0.125	2	943902F	103
R44	P1	100k	Thick Film Chip	0.125	2	943914A	104
R45	N9	100k	Thick Film Chip	0.125	2	943914A	104
R46	R1	3k3	Thick Film Chip	0.125	2	943896P	332
R47	R2	3k3	Thick Film Chip	0.125	2	943896P	332
R48	R2	3k3	Thick Film Chip	0.125	2	943896P	332
R49	R4	390R	Thick Film Chip	0.125	2	943885B	391
R50	T2	22k	Thick Film Chip	0.125	2	943906B	223
R51	T9	2k2	Thick Film Chip	0.125	2	943894R	222
R52	T8	2k2	Thick Film Chip	0.125	2	943894R	222
R53	T9	2k2	Thick Film Chip	0.125	2	943894R	222
R54	T8	2k2	Thick Film Chip	0.125	2	943894R	222
R55	T9	2k2	Thick Film Chip	0.125	2	943894R	222
R56	T8	2k2	Thick Film Chip	0.125	2	943894R	222
R57	V9	2k2	Thick Film Chip	0.125	2	943894R	222
R58	V8	2k2	Thick Film Chip	0.125	2	943894R	222

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors			W				
R59	T2	10k	Thick Film Chip	0.125	2	943902F	103
R60	V2	10k	Thick Film Chip	0.125	2	943902F	103
R61	Y3	4k7	Thick Film Chip	0.125	2	943898N	472
R62	Z2	100k	Thick Film Chip	0.125	2	943914A	104
R63	Z2	100k	Thick Film Chip	0.125	2	943914A	104
Capacitors			V				
C1		47M	Electrolytic, Aluminium Tubular	5V5	-20 +80	945002G	
C2	D6	100n	Ceramic Chip	50	20	945146T	
C3	E2	100n	Ceramic Chip	50	20	945146T	
C4	G4	100n	Ceramic Chip	50	20	945146T	
C5	G6	100n	Ceramic Chip	50	20	945146T	
C6	H1	100n	Ceramic Chip	50	20	945146T	
C7	J8	100n	Ceramic Chip	50	20	945146T	
C8	M7	100n	Ceramic Chip	50	20	945146T	
C9	L6	100n	Ceramic Chip	50	20	945146T	
C10	L4	100n	Ceramic Chip	50	20	945146T	
C11	L1	100n	Ceramic Chip	50	20	945146T	
C12	N7	100n	Ceramic Chip	50	20	945146T	
C13	N4	100n	Ceramic Chip	50	20	945146T	
C14	N1	100n	Ceramic Chip	50	20	945146T	
C15	P1	100n	Ceramic Chip	50	20	945146T	
C16	P3	470n	Ceramic Chip	50	20	941767E	
C17	R7	100n	Ceramic Chip	50	20	945146T	
C18	R5	100n	Ceramic Chip	50	20	945146T	
C19	R4	1µ	Tantalum Chip	35	20	945049Z	
C20	V6	100n	Ceramic Chip	50	20	945146T	
C21	W9	100n	Ceramic Chip	50	20	945146T	
C22	W2	100n	Ceramic Chip	50	20	945146T	
C23	Y6	100n	Ceramic Chip	50	20	945146T	
C24	Y1	100n	Ceramic Chip	50	20	945146T	
C25	Z3	33µ	Tantalum Chip	10	20	945054T	
C26	Z5	100n	Ceramic Chip	50	20	945146T	
Inductors			W				
L1		150nH	Choke	0.2	10	940392R	
L2		150nH	Choke	0.2	10	940392R	
Diodes							
D1	C3		BAS 16			943951D	
D2	C3		BAS 16			943951D	
D3	C2		BAS 16			943951D	
D4	C1		BAS 16			943951D	
D5	C0		BAS 16			943951D	
D6	D3		BAS 16			943951D	
D7	D3		BAS 16			943951D	
D8	D2		BAS 16			943951D	
D9	D1		BAS 16			943951D	
D10	D0		BAS 16			943951D	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Transistors							
TR1	C3		MMBT2222A NPN			943949Y	
TR2	C3		MMBT2222A NPN			943949Y	
TR3	C2		MMBT2222A NPN			943949Y	
TR4	C1		MMBT2222A NPN			943949Y	
TR5	C0		MMBT2222A NPN			943949Y	
TR6	C0		MMBT2222A NPN			943949Y	
TR7	Y3		MMBT2222A NPN			943949Y	
TR8	Y3		BCX 71J PNP			943950M	
Integrated Circuits		CAUTION: *SSD - STATIC SENSITIVE DEVICES					
ML1			Display, Triple 7-Segment, Red			945175X	
ML2		*SSD	28C64, 8k x 8-Bit EEPROM			945350Y	
ML3			68488			941270N	
ML4		*SSD	68000, 16-Bit Microprocessor			945154C	
ML5			3447			941271U	
ML6			3447			941271U	
ML7		*SSD	68230, Parallel Interface Timer			945153L	
ML8		*SSD	68230, Parallel Interface Timer			945153L	
ML9	C8	*SSD	74HCT245, Octal Bus Transceiver			943988Z	
ML10	D8	*SSD	74HCT241, Octal Buffer			945311X	
ML11	L8	*SSD	62256, 32k x 8-Bit Static RAM			945252N	
ML12	M8	*SSD	62256, 32k x 8-Bit Static RAM			945252N	
ML13	V9	*SSD	74HC377, D-Type Flip-Flop			943990E	
ML14	M6	*SSD	74HCT32, Quad 2-Input OR Gate			943976U	
ML15	P7	*SSD	74HCT139, 2 to 4 Line Decoder/Demultiplexer			945157R	
ML16	S6	*SSD	74HCT10, Triple 3-Input NAND Gate			943973F	
ML17	T6	*SSD	74HCT32, Quad 2-Input OR Gate			943976U	
ML18	V6	*SSD	74HCT138, 3 to 8 Line Decoder/Latch			943981O	
ML19	X6	*SSD	74HCT245, Octal Bus Transceiver			943988Z	
ML20	Y6	*SSD	74HCT245, Octal Bus Transceiver			943988Z	
ML21	F4	*SSD	74HCT04, Hex Inverter			945152E	
ML22	M4	*SSD	74HCT161, Synchronous 4-Bit Binary Counter			943984T	
ML23	N4		428, D/A Converter			945158Y	
ML24	R4		428 D/A Converter			945158Y	
ML25	F2	*SSD	74HC377, D-Type Flip-Flop			943990E	
ML26	G1		74LS09, Quad 2-Input AND Gate			945155J	
ML27	M1	*SSD	74HCT240, Octal Inverter Buffer			943986B	
ML28	N2		4051, 8 Channel Multiplexer			943993J	
ML29	P2		324, Quad Operational Amplifier			945026G	
ML30	S2	*SSD	74HC4066, Quad Analogue Switch			945151N	
PD1		*SSD	27210, 64k x 16-Bit EPROM			945364B	
PD2		*SSD	27210, 64k x 16-Bit EPROM			945364B	
Connectors							
PL1			Plug, 64-way			940339G	
Switches							
SA			Slide, DIL			945176E	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Miscellaneous							
W1			Cable Assembly			BA87138	
W2			Cable Assembly			BA87140	
LK2			Comprising:				
			Plug, 4-way			943168X	
			Shorting Link			943684I	
TP1 to TP10			Terminal, Assembly (test points)			936148X	
XL1			Crystal Oscillator 8 MHz			945170K	



Processor Module (IEEE): Block Diagram **Fig 15.2**

CHAPTER 16

FRONT PANEL ASSEMBLY (RA3703/RA3704/RA3705)

CONTENTS

ILLUSTRATIONS

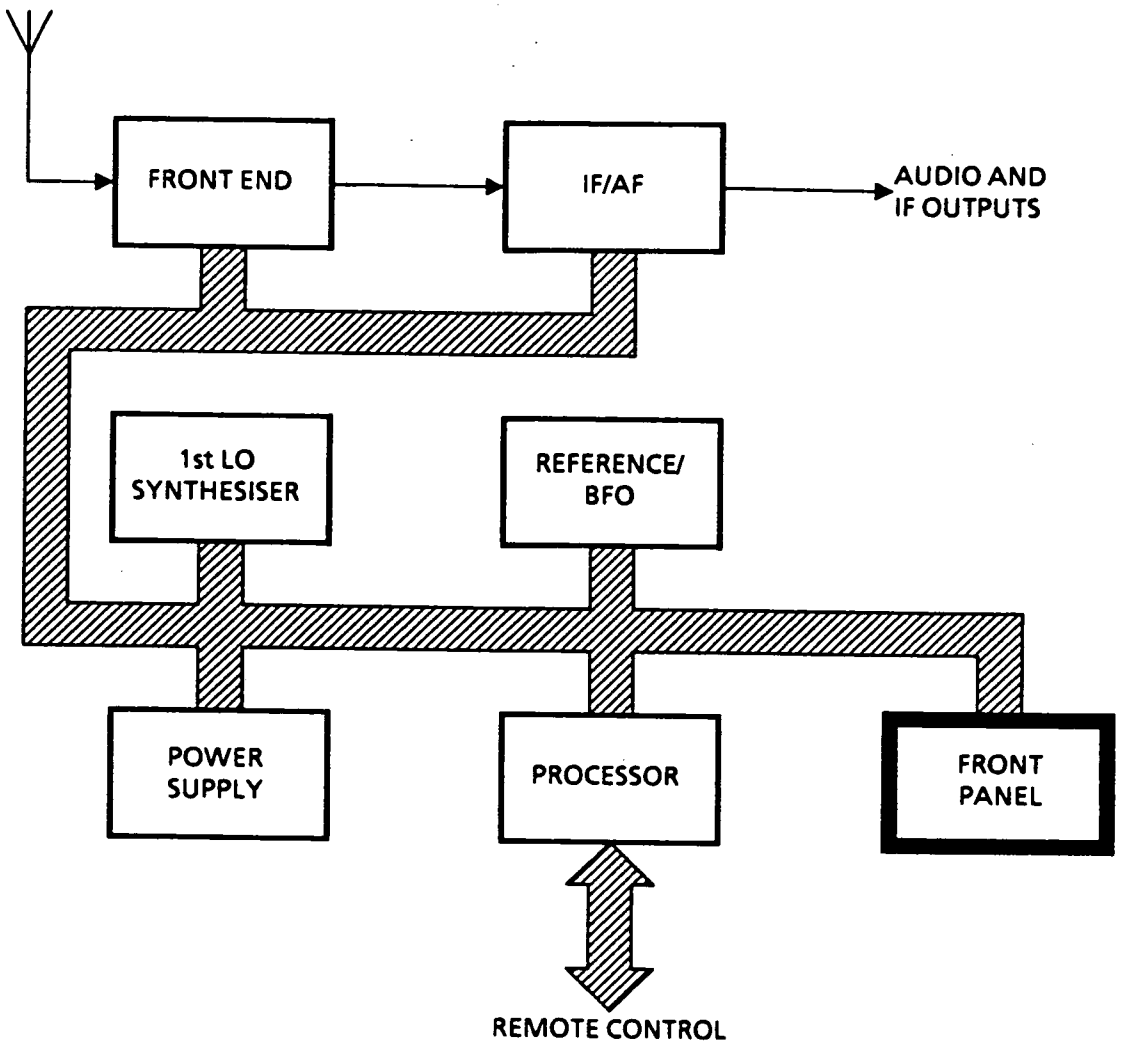


Fig. 16.1 Receiver Block Diagram

CHAPTER 16

FRONT PANEL ASSEMBLY (RA3703/RA3704/RA3705)

INTRODUCTION

1 This version of the Front Panel Assembly is fitted to single and dual slave receivers (RA3703/RA3704/RA3705) to provide both audio monitoring and fault indication facilities. In addition, switches are provided to allow the address and remote link parameters for the slave receiver to be locally set up from the front panel. The electronic components are carried on a printed circuit board mounted behind the front panel.

Fig. 16.1 Receiver Block Diagram

ASSEMBLY DESCRIPTION

2 The following description should be read in conjunction with the Front Panel Assembly Block and Circuit Diagrams included in this chapter. Component references shown in the Block Diagram allow it to be related to the Circuit Diagram.

Audio Monitoring

3 A separate AUDIO AMPLIFIER with its own VOLUME control is provided for each PHONES socket on the front panel. The AUDIO AMPLIFIER driving the PHONES 1 socket is fed with the Audio A Input and is used by single receivers as well as receiver 1 in dual receivers. The Audio B Input is used only for receiver 2 in dual receivers and feeds the AUDIO AMPLIFIER driving the PHONES 2 socket.

Fault Indicators

4 Visual indication of a fault condition detected by the receiver BITE system is provided by a pair of light emitting diodes (LED) mounted on the front panel. The FAULT 1 LED is used to indicate a fault in single receivers or receiver 1 in dual receivers. The FAULT 2 LED is used solely to indicate a fault in receiver 2 in dual receivers.

5 The LEDs are each driven by an LED DRIVER stage which is controlled by data held in the DATA LATCH.

Receiver Address Switches

6 The receiver address may be set up for use in remote control systems. This is achieved using two pairs of rotary switches on the front panel, normally concealed behind a removable cover. The two ADDRESS 1 switches (SC, SD) provide a 2-digit address for single receivers and receiver 1 in dual receivers. Likewise, the two ADDRESS 2 switches (SE, SF) provide the same facility for receiver 2 in dual receivers (serial ASCII versions only).

Link Configuration Switches

7 Two banks of eight switches are mounted below the ADDRESS SWITCHES on the front panel and are also concealed behind the cover. These LINK CONFIGURATION SWITCHES allow the remote link parameters to be configured from the front panel of the slave receiver. Chapter 6 of the RA3700 Series Operators Manual contains details of the switch settings for the various available link configurations.

Bus Interface

8 The ADDRESS DECODER detects addresses on the Module Address Bus from the Processor Module and then produces read or write pulses according to the status of the R/W input. These pulses allow the Processor to read data from the DATA BUFFERS and write data to the DATA LATCH, using the Module Data Bus. Pulses on the strobe input ensure correct timing of write pulses.

9 The DATA BUFFERS allow the status of the LINK CONFIGURATION SWITCHES and ADDRESS SWITCHES to be read at power-up only. The DATA LATCH outputs are used to control a BITE MULTIPLEXER and select the appropriate FAULT LED by enabling its LED DRIVER stage.

10 The Processor identifies the Front Panel Assembly by the identification code read out of the ASSEMBLY IDENT onto the Module Data Bus.

BITE Measurement System

11 The BITE measurement system, comprising the BITE MULTIPLEXER operating in conjunction with a BITE COMPARATOR, allows the Processor to measure various voltages in the Front Panel Assembly. The voltage to be measured is selected by the BITE MULTIPLEXER and compared in the BITE COMPARATOR with a voltage generated by a digital to analogue converter (DAC) in the Processor Module. The Processor measures the level of the selected voltage by applying voltages representing upper and lower limits to the BITE COMPARATOR and then monitoring the resulting output.

FAULT FINDING

General

12 Fault finding techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the Front Panel Assembly is contained in the following sections.

BITE Tests

13 The following BITE tests for the Front Panel Assembly are arranged in the order in which they are performed or presented for selection.

TEST NUMBER : 151

TITLE : BITE hardware

PERFORMED : Continuous, unit confidence test, select test

DESCRIPTION : DAC 1 line is set to 2.55 volts (i.e. max). BITE multiplexer input X1 (+ 5volts) is selected and the output of the BITE comparator is checked to ensure that it is low.

LIMITS : Less than 0.8 V at TP7.

FAULT DIRECTORY : Fault No. 2

TEST NUMBER : 152, 153

TITLE : + 5V rail, +15V audio rail

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : The appropriate BITE multiplexer input is selected and the supply voltage is checked.

LIMITS :

Test No.	Supply	Mux. Input	Mux. Limits (TP7)	
			Lower	Upper
152 153	+5 V +15 V (Audio)	X2 X3	1.78V 1.7 V	2.22 V 2.21 V

FAULT DIRECTORY : Fault No. 4

SIGNATURE ANALYSIS ROUTINE

17 This routine checks that the module control signals are interfaced and decoded correctly from the module bus.

Processor Module DIL switch setting: SW1,3,5,6,8 OFF
SW2,4,7 ON

Signature Analyser connections:

Start: TP11 Front panel negative trigger
Stop: TP11 Front panel negative trigger
Clock: Test point 8A on extender assembly, negative trigger
Earth: Test point 1B on extender assembly

Note : Signatures xxxxF signify a flashing probe indicator.

Signal	Signature	Test Node						Remarks
+5v	99FA							
OV	0000							
		DATA BUS INTERFACES						
M-D0	A8AU	R6/2	ML5/3	ML1/3	ML2/3	ML3/3	ML4/3	Module bus
M-D1	HA09	R6/3	ML5/5	ML1/5	ML2/5	ML3/5	ML4/5	Module bus
M-D2	6190	R6/4	ML5/7	ML1/7	ML2/7	ML3/7	ML4/7	Module bus
M-D3	3H2A	R6/5	ML5/9	ML1/9	ML2/9	ML3/9	ML4/9	Module bus
M-D4	12AC	R6/6	ML5/12	ML1/12	ML2/12	ML3/12	ML4/12	Module bus
M-D5	84U3	R6/7	ML5/14	ML1/14	ML2/14	ML3/14	ML4/14	Module bus
M-D6	FU33	R6/7	ML5/16	ML1/16	ML2/16	ML3/16	ML4/16	Module bus
M-D7	PAUO	R6/8	ML5/18	ML1/18	ML2/18	ML3/18	ML4/18	Module bus
		DATA LATCH (ML5)						
Q0/S0	H588	ML5/2	ML6/11					Control S0
Q1/S1	6HPC	ML5/5	ML6/10					Control S1
Q2/S2	31HA	ML5/6	ML6/9					Control S2
Q6	P68C	ML5/16	R26					Fault1 LED
Q7	U46A	ML5/19	R27					Fault2 LED
E	0000	ML5/1						GND
		ADDRESS DECODER						
M-STB	0000F	R33	ML9/6					ADDR DEC
M-A7	0001	R24	ML10/1					ADDR DEC
M-A6	0001	R23	ML10/2					ADDR DEC
M-A5	0001	R22	ML10/9					ADDR DEC
M-A4	0000	R21	ML10/10					ADDR DEC
M-A3	0003	R20	ML9/2					ADDR DEC
M-A2	003H	R19	ML9/3					ADDR DEC
M-A1	00FF	R18	ML9/2	ML8/2				ADDR DEC

SIGNATURE ANALYSIS ROUTINE (continued)

Signal	Signature	Test Node			Remarks
		ADDRESS DECODER			
M-A0	0157	R17	ML9/1	ML8/6	ADDR DEC
M-R/W	03U9	R25	ML9/5	ML8/6	ADDR DEC
ML10	0001	ML10/3	ML10/4		ADDR DEC
ML10b	0001	ML10/8	ML10/5		
Y0	99FAF	ML9/15	ML5/11		
$\overline{E1}$	0001	ML10/6	ML9/4	ML8/4	
$\overline{Y1}$	98H8	ML8/14	ML3/1		
$\overline{Y2}$	9943	ML8/13	ML2/1		
$\overline{Y3}$	998P	ML8/12	ML1/1		
$\overline{Y4}$	99F8	ML8/11	ML4/1		
Y0	9CPU	ML8/15	ML7/70		
		SWITCHES			
		Set SC,SD,SE and SF all to 5.			
1A0	0000	ML4/2	R5/9		READ PORT0
1A1	99FA	ML4/4	R5/8		READ PORT0
1A2	0000	ML4/6	R5/7		READ PORT0
1A3	99FA	ML4/8	R5/6		READ PORT0
2A0	0000	ML4/11	R5/5		READ PORT0
2A1	99FA	ML4/13	R5/4		READ PORT0
2A2	0000	ML4/15	R5/3		READ PORT0
2A3	99FA	ML4/17	R5/2		READ PORT0
1A0	0000	ML3/2	R4/9		READ PORT1
1A1	99FA	ML3/4	R4/8		READ PORT1
1A2	0000	ML3/6	R4/7		READ PORT1
1A3	99FA	ML3/8	R4/6		READ PORT1
2A0	0000	ML3/11	R4/5		READ PORT1
2A1	99FA	ML3/13	R4/4		READ PORT1
2A2	0000	ML3/15	R4/3		READ PORT1
2A3	99FA	ML3/17	R4/2		READ PORT1
		Set SC,SD,SE and SF all to 0.			
1A0	0000	ML4/2	R5/9		READ PORT0
1A1	0000	ML4/4	R5/8		READ PORT0
1A2	0000	ML4/6	R5/7		READ PORT0
1A3	0000	ML4/8	R5/6		READ PORT0
2A0	0000	ML4/11	R5/5		READ PORT0
2A1	0000	ML4/13	R5/4		READ PORT0
2A2	0000	ML4/15	R5/3		READ PORT0
2A3	0000	ML4/17	R5/2		READ PORT0
1A0	0000	ML3/2	R4/9		READ PORT1

SIGNATURE ANALYSIS ROUTINE (continued)

Signal	Signature	Test Node		Remarks
		SWITCHES		
		Set SC,SD,SE and SF all to 0.		
1A1	0000	ML3/4	R4/8	READ PORT1
1A2	0000	ML3/6	R4/7	READ PORT1
1A3	0000	ML3/8	R4/6	READ PORT1
2A0	0000	ML3/11	R4/5	READ PORT1
2A1	0000	ML3/13	R4/4	READ PORT1
2A2	0000	ML3/15	R4/3	READ PORT1
2A3	0000	ML3/17	R4/2	READ PORT1
		Set SA and SB with 1,3,5,7 ON and 2,4,6,8 OFF		
1A0	99FA	ML2/2	R3/3	READ PORT2
1A1	0000	ML2/4	R3/4	READ PORT2
1A2	99FA	ML2/6	R3/5	READ PORT2
1A3	0000	ML2/8	R3/6	READ PORT2
2A0	99FA	ML2/11	R3/7	READ PORT2
2A1	0000	ML2/13	R3/8	READ PORT2
2A2	99FA	ML2/15	R3/9	READ PORT2
2A3	0000	ML2/17	R3/10	READ PORT2
1A0	99FA	ML1/2	R2/3	READ PORT3
1A1	0000	ML1/4	R2/4	READ PORT3
1A2	99FA	ML1/6	R2/5	READ PORT3
1A3	0000	ML1/8	R2/6	READ PORT3
2A0	99FA	ML1/11	R2/7	READ PORT3
2A1	0000	ML1/13	R2/8	READ PORT3
2A2	99FA	ML1/15	R2/9	READ PORT3
2A3	0000	ML1/17	R2/10	READ PORT3
		Set SA and SB with 2,4,6,8 ON and 1,3,5,7 OFF		
1A0	0000	ML2/2	R3/3	READ PORT2
1A1	99FA	ML2/4	R3/4	READ PORT2
1A2	0000	ML2/6	R3/5	READ PORT2
1A3	99FA	ML2/8	R3/6	READ PORT2
2A0	0000	ML2/11	R3/7	READ PORT2
2A1	99FA	ML2/13	R3/8	READ PORT2
2A2	0000	ML2/15	R3/9	READ PORT2
2A3	99FA	ML2/17	R3/10	READ PORT2
1A0	0000	ML1/2	R2/3	READ PORT3
1A1	99FA	ML1/4	R2/4	READ PORT3
1A2	0000	ML1/6	R2/5	READ PORT3
1A3	99FA	ML1/8	R2/6	READ PORT3
2A0	0000	ML1/11	R2/7	READ PORT3

SIGNATURE ANALYSIS ROUTINE (continued)

Signal	Signature	Test Node	Remarks
		SWITCHES Set SA and SB with 2,4,6,8 ON and 1,3,5,7 OFF	
2A1	99FA	ML1/13 R2/8	READ PORT3
2A2	0000	ML1/15 R2/9	READ PORT3
2A3	99FA	ML1/17 R2/10	READ PORT3
		MULTIPLEXER	
$\overline{E}$	0000F	ML6/6	
A0	0000F	ML6/13	

Fault Directory

14 Use the following fault directory to identify the fault condition and take the necessary corrective action. Note that all inputs to the assembly are assumed to be correct.

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
1	Fails to run BITE tests for Front Panel Assembly.	Address decoder/assembly ident. not responding.	Check address decoding/assembly ident logic operation using signature analysis routine if necessary.
2	BITE hardware fault.	Comparator/multiplexer inoperative.	Use BITE test 151 to check comparator operation. Select all BITE tests for the front panel to check multiplexer operation for all analogue inputs. Use signature analysis routine to check multiplexer addressing.
3	BITE indicates failure but manual check shows no fault.	BITE hardware fault.	As Fault No. 2.
4	Power supply fault within module.	Faulty component drawing excess current.	Locate and replace faulty component.
5	No audio output.	(a) Audio amplifier faulty. (b) Audio input absent. (c) Faulty volume control.	(a) Check signal levels around suspect amplifier. (b) Check audio is being applied to the volume control. (c) Check operation.
6	No response to settings made on address or link configuration switches.	(a) Switches faulty. (b) Data buffer faulty or not selected by address decoder.	(a) Check switch operation. (b) Check signal and control lines using oscilloscope.
7	Fault LED fails to indicate a fault condition.	(a) LED or driver faulty. (b) Data latch faulty.	(a) Check voltage levels. (b) Check output and control lines using oscilloscope.

PARTS LIST

15 The Racal part number for a complete Front Panel Assembly (RA3703/RA3704/RA3705) is ST88181.

16 Information on the identification and handling of SMDs is provided in Chapter 2. The parts list for the Front Panel Assembly is as follows:

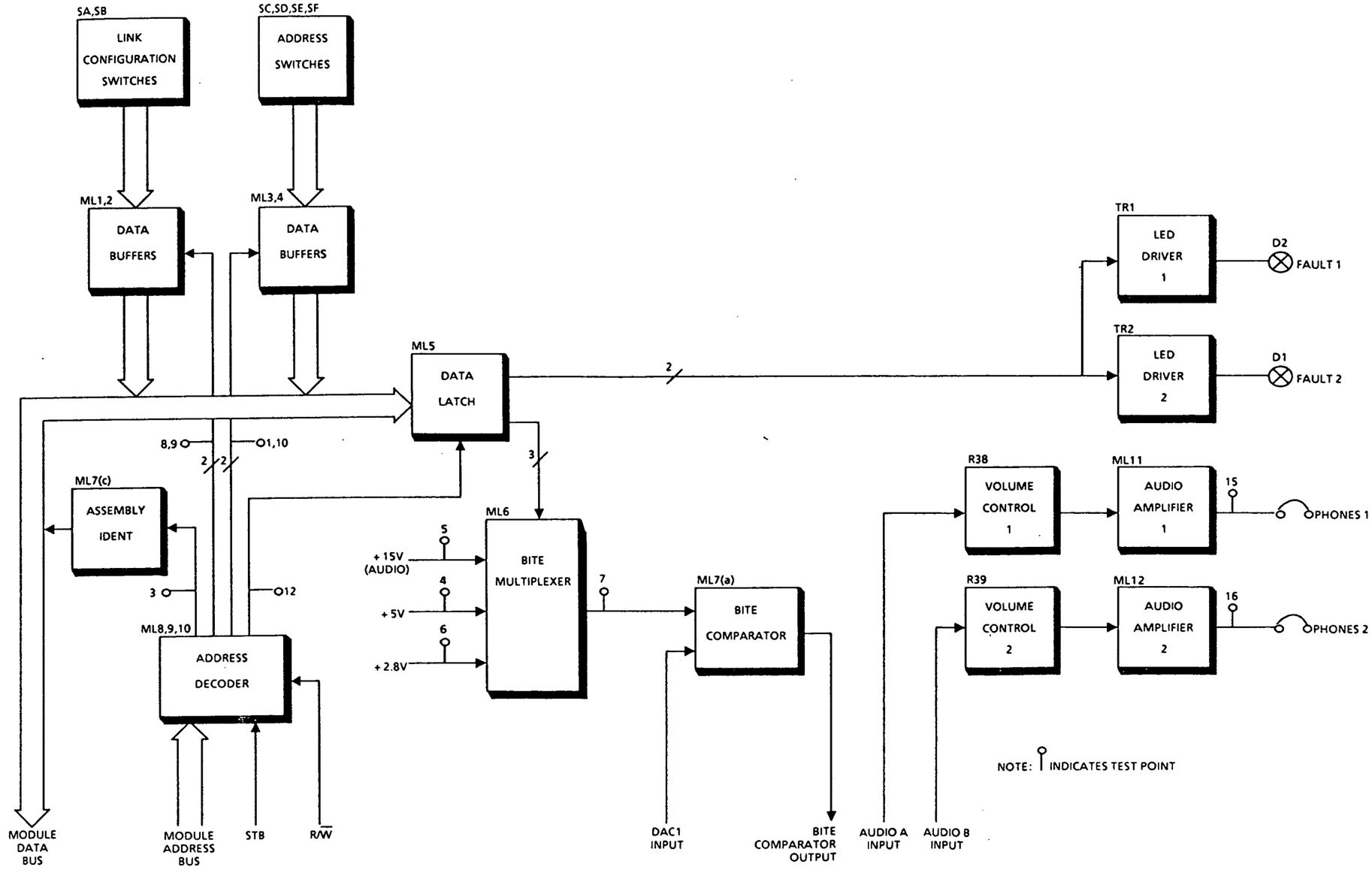
Outline missing

Resistors			W			
R1	470R	Thick Film Chip	0.125	2	943886I	
R2	33k	Thick Film Network			934507U	
R3	33k	Thick Film Network			934507U	
R4	33k	Thick Film Network			934507U	
R5	33k	Thick Film Network			934507U	
R6	33k	Thick Film Network			934507U	
R7	10k	Thick Film Chip	0.125	2	943902F	103
R8	15k	Thick Film Chip	0.125	2	943904D	153
R9	10k	Thick Film Chip	0.125	2	943902F	103
R10	120k	Thick Film Chip	0.125	2	943915R	124
R11	18k	Thick Film Chip	0.125	2	943905K	183
R12	1k8	Thick Film Chip	0.125	2	943893A	182
R13	22k	Thick Film Chip	0.125	2	943906B	223
R14	10k	Thick Film Chip	0.125	2	943902F	103
R15	1k2	Thick Film Chip	0.125	2	943891C	122
R16	33k	Thick Film Network			934507U	
R17	10k	Thick Film Chip	0.125	2	943902F	103
R18	10k	Thick Film Chip	0.125	2	943902F	103
R19	10k	Thick Film Chip	0.125	2	943902F	103
R20	10k	Thick Film Chip	0.125	2	943902F	103
R21	10k	Thick Film Chip	0.125	2	943902F	103
R22	10k	Thick Film Chip	0.125	2	943902F	103
R23	10k	Thick Film Chip	0.125	2	943902F	103
R24	10k	Thick Film Chip	0.125	2	943902F	103
R25	10k	Thick Film Chip	0.125	2	943902F	103
R26	10k	Thick Film Chip	0.125	2	943902F	103
R27	10k	Thick Film Chip	0.125	2	943902F	103
R28	2R2	Thick Film Chip	0.125	5	945208C	
R29	2R2	Thick Film Chip	0.125	5	945208C	
R30	470R	Thick Film Chip	0.125	2	943886I	471
R31	470R	Thick Film Chip	0.125	2	943886I	471
R32	33k	Thick Film Chip	0.125	2	943908Z	333
R33	10k	Thick Film Chip	0.125	2	943902F	103
R34	1k2	Thick Film Chip	0.125	2	943891C	122
R35	390R	Thick Film Chip	0.125	2	943885B	391
R36	390R	Thick Film Chip	0.125	2	943885B	391
R37	1k2	Thick Film Chip	0.125	2	943891C	122
R38	10k	Variable, Logarithmic		20	AD87098	
R39	10k	Variable, Logarithmic		20	AD87098	

Capacitors			V		
C1	3µ3	Tantalum Chip	16	20	945050N
C2	100n	Ceramic Chip	50	20	945146T
C3	100n	Ceramic Chip	50	20	945146T
C4	3µ3	Tantalum Chip	16	20	945050N
C5	100n	Ceramic Chip	50	20	945146T
C6	220µ	Electrolitic, Tubular	40	-10 +50	945005L
C7	100n	Ceramic Chip	50	20	945146T
C8	100n	Ceramic Chip	50	20	945146T
C9	330µ	Electrolitic, Tubular	25	-10 +50	945006C
C10	330	Electrolitic, Tubular	25	-10 +50	945006C
C11	18p	Ceramic Chip	50	5	941790U

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C12		18p	Ceramic Chip	50	5	941790U	
C13		100n	Ceramic Chip	50	20	945146T	
C14		100n	Ceramic Chip	50	20	945146T	
C15		6µ8	Tantalum Chip	35	20	945052L	
C16		100n	Ceramic Chip	50	20	945146T	
C17		6µ8	Tantalum Chip	35	20	945052L	
C18		6µ8	Tantalum Chip	35	20	945052L	
C19		6µ8	Tantalum Chip	35	20	945052L	
Diodes							
D1			521-9248, LED			929351Z	
D2			521-9248, LED			929351Z	
D3			521-9250, LED			929350I	
Transistors							
TR1			BC 849, NPN			943941W	
TR2			BC 849, NPN			943941W	
Integrated Circuits		CAUTION:	*SSD - STATIC SENSITIVE DEVICES				
ML1		*SSD	74HC244, Octal Line Driver			943987I	
ML2		*SSD	74HC244, Octal Line Driver			943987I	
ML3		*SSD	74HC244, Octal Line Driver			943987I	
ML4		*SSD	74HC244, Octal Line Driver			943987I	
ML5		*SSD	74HC377, D-Type Flip-Flop			943990E	
ML6		*SSD	4051, 8-Channel Multiplexer			943993J	
ML7			339, Quad Voltage Comparator			945023R	
ML8		*SSD	74HC138, 3 to 8 Line Decoder			943980X	
ML9		*SSD	74HC138, 3 to 8 Line Decoder			943980X	
ML10		*SSD	74HC32, Quad 2-Input OR Gate			943975D	
ML11			380, Audio Amplifier			945018H	
ML12			380, Audio Amplifier			945018H	
Connectors							
PL1			Plug, 34-way			945453W	
PL2			Plug, 20-way			943728L	
PL3			Plug, 3-way			943740N	
Switches							
SA			Slide, DIL			941448W	
SB			Slide, DIL			941448W	
SC			Rotary, BCD			943673U	
SD			Rotary, BCD			943673U	
SE			Rotary, BCD			943673U	
SF			Rotary, BCD			943673U	
SG			Rocker			938535N	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Miscellaneous							
TP1 to TP16			Terminal, Assembly (test points)			936148X	
P1 to P6			Terminal, Pin			916945K	



Front Panel Assembly (RA3703/4/5): Block Diagram **Fig.16.2**

CHAPTER 17

FSK MODULE

CONTENTS

ILLUSTRATIONS

CHAPTER 17

FSK MODULE

INTRODUCTION

1 The FSK Module takes the audio from the receiver bus on the motherboard and demodulates 2-tone FSK signals to produce a low-level telegraph output to drive a teleprinter. Two channels are provided for operation in dual or ISB receivers. Diversity operation is provided by a diversity combiner which automatically switches the strongest channel input to the teleprinter output.

Fig. 17.1 Receiver Block Diagram

MODULE DESCRIPTION

2 The following description should be read in conjunction with the FSK Module Block and Circuit Diagrams included in this chapter. Component references shown on the Block Diagram allow it to be related to the Circuit Diagram. Because the operation of the two channels is the same, only channel A is described.

Input Band Pass Filter

3 The FSK audio signal on the Audio A input is passed through a band pass filter centred on 2 kHz. This filter is formed by two active filters using operational amplifiers, one a HIGH PASS FILTER and the other a LOW PASS FILTER, to give a band-limited audio between 1 kHz and 3.8 kHz.

Limiter

4 Amplitude variations on the audio input are removed by a LIMITER formed by two high-gain operational amplifiers. These clip the audio input to produce a 25 V peak-to-peak square wave at the audio frequency.

Discriminator

5 The FSK signal is demodulated by a frequency discriminator comprising BAND PASS FILTERS, RECTIFIERS, FILTERS and a SUMMER. In the discriminator the limited input signal is split into two parallel paths and applied to a pair of active BAND PASS FILTERS formed by operational amplifiers and centred on 2.7 kHz and 1.4 kHz respectively.

6 The characteristics of the two filters are given in Fig. 17.2. When the outputs of the two filters are combined, after rectification, in the SUMMER, the filter characteristic of the upper BAND PASS FILTER is inverted. Summing the filter outputs in this way gives the characteristic 'S' curve of an FSK discriminator. For input frequencies between 1.5 kHz and 2.5 kHz the output voltage of the discriminator (at TP7) is approximately proportional to the input frequency.

Fig. 17.2 Discriminator Characteristics

7 Each filter output is rectified by a full-wave RECTIFIER comprising two rectifier stages formed by inverting operational amplifiers. During the negative half-cycle output from the upper BAND PASS FILTER, the output of the first rectifier stage, ML7(c), is clamped to 0 volts by D16 connected between the output and inverting input. This stage is then bypassed by R78 so that the inverted form of the negative-going signal appears at the output of the second rectifier stage, ML6(a).

8 During the positive-going half-cycle output from the filter, D16 and D14 are biased such that the first rectifier stage inverts the signal, which is then inverted again in the second stage. This results in the input and output signals of the RECTIFIER being in phase. The action of the RECTIFIER serving the lower BAND PASS FILTER is identical.

9 Each RECTIFIER output is smoothed by a FILTER to produce a DC level which is applied to one input of a differential amplifier operating as the SUMMER. A preset BALANCE resistor is included in the non-inverting input to allow the output of the SUMMER to be set to 0 volts when a 2 kHz signal (no shift) is present at the Audio A input.

10 The summed output is fed to output drive and metering circuits via a voltage follower BUFFER which provides smoothing at its input. A BITE detector monitors the BUFFER output and produces a scaled voltage for the BITE MULTIPLEXER.

FSK Output Slicing and Level Shifting

11 The buffered output from the discriminator drives a SLICER which is connected in an open-loop configuration to produce output levels approaching the supply voltages, i.e. ± 15V. A BUFFER takes this sliced signal and produces a logic high for an input frequency above 2 kHz and a logic low for an input frequency below 2 kHz.

12 A LED visible through the top of the module is turned on for frequencies below 2 kHz and off for frequencies above 2 kHz. When setting up the module, a 2 kHz signal is applied to the audio input and the discriminator preset resistor adjusted until the LED just turns off.

13 The demodulated FSK output from the discriminator is passed through an INTERNAL/EXTERNAL DEMODULATION SWITCH which selects either the internal or external demodulated FSK signal for application to the diversity switching circuit.

Diversity Switching Circuit

14 The outputs from the two discriminators are brought together in a DIVERSITY SWITCHING CIRCUIT which (if enabled) automatically switches the strongest signal to the main output.

15 In the DIVERSITY SWITCHING circuit the two channels are first passed through gates ML15(a) and (b). The gates are controlled via the module interface circuits and invert the signals as required to determine whether a low or high frequency represents a MARK.

16 In non-diversity mode, either channel A or B may be constantly directed to the main output by change-over switch ML11(c). This switch is controlled by latch ML10(a) whose output may be set to the required state by signals on the set/reset control lines from the module interface.

17 The output of ML11(c) is gated by latch ML10(b) which is used in conjunction with gate ML15(d) to switch the main output on or off, or set the output high or low as required.

18 Two further gates, ML9(d) and ML17(d), allow the channel A and B outputs from the DIVERSITY SWITCHING circuit to be switched on or off.

19 All three outputs are taken via INVERTERS to LINE DRIVERS which provide the teleprinter outputs at the rear panel socket (SK1). The INVERTERS may be used to invert the output signals to determine whether a high or low level represents a MARK to the teleprinter.

20 When diversity mode is selected and the same signal is present on both discriminator outputs, ML15(c) and ML19(a) enable ML9(b) to pass the clock output from the 20 kHz OSCILLATOR.

21 The clock signal latches the status of the DIVERSITY AGC COMPARATOR output into latch ML10(a). This status signal is low when the DIV AGC A input is lower than the DIV AGC B input, indicating that the FSK input to channel A is the stronger signal.

22 ML10(a) output controls change-over switch ML11(c) to select the demodulated FSK signal from the stronger channel. The relative high speed of the clock signal ensures that switching occurs as soon as the input conditions are changed. The selected output is then clocked into latch ML10(b) for routing to the main teleprinter output as before.

Tuning Meter Drive

23 When the receiver is correctly tuned to the FSK transmission, a tuning meter drive circuit produces a DC signal which results in a zero centre reading on the Front Panel Assembly tuning meter.

24 In this metering circuit the discriminator output is fed to two identical positive-going PEAK DETECTORS, one of which is converted to detect negative-going signals by an INVERTER included in the input path. These peak levels therefore represent the maximum and minimum frequencies present in the audio signal.

25 The PEAK DETECTOR output signals are applied via voltage follow BUFFER stages to a SUMMER, which subtracts one from the other to produce a DC level proportional to the average of the two input frequencies.

26 The SUMMER output is converted to a BITE level for application to the BITE MULTIPLEXER. This subsequently drives the tuning meter on the front panel for a zero indication when the peak levels of the two tones are equal.

Bus Interface

27 A unique hardwired code is received on the Module Address input to the FSK Module. This code is used by the ADDRESS DECODER to detect addresses on the Module Address Bus from the Processor Module and then produce read or write pulses according to the status of the R/W input. These pulses allow the Processor to read data from the 3-STATE BUFFER or write data to the DATA LATCHES, using the Module Data Bus. Pulses on the strobe input ensure correct timing of write pulses. The 3-STATE BUFFER gives the Processor access to the FSK Module identification code and also monitors the state of the diversity switch and FSK teleprinter outputs. The outputs of the DATA LATCHES are used to control the switching of internal/external inputs, diversity mode and channel outputs, as well as the BITE MULTIPLEXER.

BITE Measurement System

28 The BITE measurement system, comprising the BITE MULTIPLEXER operating in conjunction with a BITE COMPARATOR, allows the Processor Module to monitor the drive output of the FSK metering circuits and measure various voltages and operating levels in the FSK Module. The voltage to be measured is selected by the BITE MULTIPLEXER and compared in the BITE COMPARATOR with a voltage generated by a digital to analogue converter (DAC) in the Processor Module. The Processor measures the level of the selected voltage by applying voltages representing upper and lower limits to the BITE COMPARATOR and then monitoring the resulting output.

FAULT FINDING

General

29 Fault finding techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the FSK Module is contained in the following sections.

BITE Tests

30 The following BITE tests for the FSK Module are arranged in the order in which they are performed or presented for selection.

TEST NUMBER	:	451
TITLE	:	BITE hardware
PERFORMED	:	Continuous, unit confidence test, select test
DESCRIPTION	:	DAC 1 line is set to 2.55 volts (i.e. max). BITE multiplexer input X1 (+5 volts) is selected and the output of the BITE comparator is checked to ensure that it is low.
LIMITS	:	Less than 0.5 V at TP3.
FAULT DIRECTORY	:	Fault No. 2

TEST NUMBER : 452, 453, 454

TITLE : +5 V rail, +15 V rail, -15 V rail.

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : The appropriate BITE multiplexer input is selected and the supply voltage is checked.

LIMITS :

Test No.	Supply	Mux. Input	Mux. Limits (TP3)	
			Lower	Upper
452	+5 V	X2	1.78 V	2.22 V
453	+15 V	X3	1.70 V	2.21 V
454	-15 V	X4	1.73 V	2.13 V

FAULT DIRECTORY : Fault No. 4

TEST NUMBER : 455

TITLE : FSK disc. sweep.

PERFORMED : Unit confidence test, select test.

DESCRIPTION : The BFO is selected and the receiver is tuned to 0 MHz to provide an FSK audio test tone. The BFO frequency is swept across the discriminator operating range in 100 Hz steps. BITE multiplexer input X8 (channel A) is selected to measure the discriminator output at each step. If channel B is being used the test is repeated with BITE multiplexer input X7 selected.

LIMITS :

FSK Audio Input (kHz)	Discriminator Voltage (TP3)	
	Low	High
1.5	1.4	2.3
1.6	1.28	2.13
1.7	1.16	1.96
1.8	1.04	1.80
1.9	0.92	1.65
2.0	0.80	1.50
2.1	0.68	1.36
2.2	0.56	1.22
2.3	0.44	1.08
2.4	0.32	0.94
2.5	0.20	0.80

FAULT DIRECTORY : Fault No. 5

TEST NUMBER : 456

TITLE : FSK meter sweep.

PERFORMED : Unit confidence test, select test.

DESCRIPTION : As test 455 but BITE multiplexer input X10 (channel A) is selected to measure the metering circuit output. If channel B is being used the test is repeated with BITE multiplexer X9 selected.

LIMITS :

FSK Audio Input (kHz)	Tuning Meter Voltage (TP3)	
	Lower	Upper
1.5	1.5	2.2
1.6	1.4	2.06
1.7	1.3	1.93
1.8	1.2	1.8
1.9	1.1	1.7
2.0	1.0	1.6
2.1	0.9	1.5
2.2	0.8	1.4
2.3	0.7	1.3
2.4	0.6	1.2
2.5	0.5	1.1

FAULT DIRECTORY : Fault No. 7

TEST NUMBER : 457

TITLE : FSK slicer sweep.

PERFORMED : Unit confidence test, select test.

DESCRIPTION : As test 455 but monitors the status of the slicer output (logic 0 or 1). It achieves this by reading the logic level of the output via the module data bus. The test is carried out in the output polarity in which the module is configured (i.e. normal or inverted).

LIMITS :

FSK Audio Input (kHz)	Slicer Logic Level
1.5	0
1.6	0
1.7	0
1.8	0
1.9	0
2.0	Not Checked
2.1	1
2.2	1
2.3	1
2.4	1
2.5	1

FAULT DIRECTORY : Fault No. 6

Fault Directory

31 Use the following fault directory to identify the fault condition and take the necessary corrective action. Note that all inputs to the module are assumed to be correct.

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
1	Fails to run BITE tests for FSK Module.	Address decoding/module ident. not responding.	Check address decoding/module ident logic operation using signature analysis routine if necessary.
2	BITE hardware fault.	Comparator/multiplexer inoperative.	Use BITE test 451 to check comparator operation. Select all BITE tests for this module to check multiplexer operation for all analogue inputs. Use signature analysis routine to check multiplexer addressing.
3	BITE indicates failure but manual check shows no fault.	(a) BITE hardware fault. (b) Faulty BITE detector.	(a) As above. (b) Check operation of suspect BITE detector.
4	Power supply fault within module.	Faulty component drawing excess current or open circuit choke L1, L2 or L3.	Locate and replace faulty component.
5	Channel A or B output fails to switch in response to FSK audio input signals.	(a) High pass filter or limiter faulty. (b) Discriminator faulty. (c) Discriminator incorrectly set up. (d) Slicer faulty. (e) Diversity/output circuits faulty.	(a) Select CW. Tune receiver to 0 MHz and BFO to 2 kHz. Check square wave present on TP5. (b) Tune BFO over the range 1.5 kHz to 2.5 kHz and check voltage on TP8 follows the S curve (Fig. 17.2), passing through 0 V at 2 kHz. (c) Adjust R3 (R5) according to alignment procedure. If unable to set up, check operation of preceding stages (see above). (d) See Fault No. 6. (e) See Fault No. 8.
6	Discriminator output correct (0V on TP8 at 2 kHz) but MONITOR LED does not turn on and off as frequency is swept past 2 kHz.	Slicer or buffer faulty.	Check circuit voltages.
7	FSK output operating correctly but no FSK tuning facility.	(a) Metering circuit faulty. (b) BITE hardware faulty.	(a) Check operation of inverter, peak detectors, buffers and summer in metering circuit as BFO is tuned over the range 1.5 kHz to 2.5 kHz. (b) See fault No. 2.
8	As the frequency is swept past 2 kHz the signal switches correctly at the diversity switching input but not at the output.	Diversity switching gating not selected correctly.	Check status of control lines from data latches using oscilloscope.
9	Strongest signal not selected by diversity switching circuit.	(a) 20 kHz oscillator inoperative. (b) Diversity AGC comparator faulty. (c) Diversity switching circuit faulty.	(a) Check operation using oscilloscope or counter. (b) Check output changes state as inputs are varied. (c) Check operation of gates and latch (ML10(a)) controlling changeover switch ML11(c).

Signature Analysis Routine

32 This routine checks that the module control signals are interfaced and decoded correctly from the module bus.

Processor module DIL switch settings: SW1,4,7 OFF
SW2,3,5,6,8 ON

Signature analyser connections:

Start: 9A Extender assembly, negative trigger
Stop: 9A Extender assembly, negative trigger
Clock: 8A Extender assembly, positive trigger
Earth: 1A Extender assembly

Note : Signatures xxxxF signify a flashing probe indicator.

Signal	Signature	Test Node					Remarks
+5V	H9A0						
OV	0000						
		DATA BUS INTERFACES					
M-D0	654F	PL1/7A	ML25/18	ML12/3	ML16/3		Module bus
M-D1	4764	PL1/7B	ML25/16	ML12/4	ML16/4		Module bus
M-D2	H670	PL1/6A	ML25/14	ML12/7	ML16/7		Module bus
M-D3	2C8A	PL1/6B	ML25/12	ML12/8	ML16/8		Module bus
M-D4	UACU	PL1/5A	ML25/9	ML12/13	ML16/13		Module bus
M-D5	3HPH	PL1/5B	ML25/7	ML12/14	ML16/14		Module bus
M-D6	44UF	PL1/4A	ML25/5	ML12/17	ML16/17		Module bus
M-D7	4H04	PL1/4B	ML25/3	ML12/18	ML16/18		Module bus
		ADDRESS DECODER					
M-A0	UF4A	PL1/12A	R152	ML18/1			Module address
M-A1	0CH4	PL1/12B	R148	ML18/2			Module address
M-A2	PU8U	PL1/11A	R156	ML18/3			Module address
M-A4	0000	PL1/10A	R155	ML26/10			Module address
M-A5	0001	PL1/10B	R154	ML26/12			Module address
M-A6	0001	PL1/9A	R153	ML26/13			Module address
M-A7	H9A0	PL1/9B	R151	ML26/15			Module address
MOD0	0000	PL1/14A	R149	ML26/9			Module address
MOD1	0000	PL1/14B	R145	ML26/11			Module address
MOD2	0000	PL1/13A	R143	ML26/14			Module address
MOD3	H9A0	PL1/13B	R140	ML26/1			Module address
M-R/W	3571	PL1/8B	R137	ML17/4	ML17/10	ML17/9	Module bus
M-STB	0000F	PL1/8A	R141	ML17/2			Module bus
A=B	H9A1	ML26/6	ML18/6	ML17/5			Addr. decoder
ML17/8	PFH1	ML17/8	ML17/1				Addr. decoder
ML17/6	PFH0	ML17/6	ML25/1	ML25/19			ID Buffer
ML17/3	H9A0F	ML17/3	ML18/4				Addr. decoder

Signature Analysis Routine (continued)

Signal	Signature	Test Node				Remarks
		ADDRESS DECODER				
ML18/14	H9A0F	ML18/14	ML12/11			Diversity ctl.
ML26/3	H9A0	ML26/3				A = B
ML26/4	H9A0	ML26/4				A > B
ML26/2	H9A0	ML26/2				A < B
TP1	H9A0	TP1	ML18/15	ML16/11		CP ML16
ML16/1	H9A0	ML16/1				MR ML16
ML12/1	H9A0	ML12/1				MR ML12
		DATA LATCH (BITE Selection) ML16				
Q0	59FP	ML16/2	ML13/10			CONTROL A
Q1	HUC3	ML16/5	ML13/11			CONTROL B
Q2	9F8H	ML16/6	`(L13/14			CONTROL C
Q3	3H12	ML16/9	ML13/13			CONTROL D
		DATA LATCH (Switching Control) ML16				
G	6HHH	ML16/12	ML11/10			Int/Ext Switch
H	F5CA	ML16/15	ML11/9			Int/Ext Switch
B	1189	ML16/16	ML9/13			Diversity Sw.
E	6PA5	ML16/19	ML17/13			Diversity Sw.
		DATA LATCH (Control Buffer) ML12				
Q0	75UU	ML12/2	ML10/4			
Q1	UC6U	ML12/5	ML10/1			
Q2	CF27	ML12/6	ML15/2			
Q3	1U83	ML12/9	ML15/5			
Q4	4P51	ML12/12	ML10/10			
Q5	66C8	ML12/15	ML10/13			
Q6	72FF	ML12/16	ML23/9	ML15/13	ML23/5	Printer Control
		DATA LATCH (Module Ident and Buffer) ML25				
YA1	0000	ML25/2				ID
YA2	0000	ML25/4				ID
YA3	0000	ML25/6				ID
YA4	H9A0	ML25/8				ID
YB1	0000	ML25/11				ID
?a = b	H9A0	ML26/3	ML26/4	ML26/2		
TP1	HA90	ML18/15	ML16/11			
ML16/1	HA90					
ML12/1	HA90					

ALIGNMENT

33 This procedure details the adjustments required for aligning the FSK Module.

Discriminator Balance Adjustment

34 Select CW mode and short AGC. Tune the receiver to 0 MHz and set the BFO to 2 kHz.

35 Check that the DISCRIM. A (or DISCRIM. B for second receiver in a dual receiver or ISB Module) MONITOR LED goes off and on as the associated BALANCE control is adjusted across its range. Set the control so that the MONITOR LED just turns off.

36 REMOTE CONTROL COMMANDS

The following remote commands control functions are associated with the FSK option. They provide the same facilities as are available when operating the receiver locally from the front panel. Refer to the RA3700 Series Operators Manual for further details.

(1) Terminal device on/off — FSKHOLDn / QFSKHOLD

This command toggles the output between the "run" state in which data is sent to the terminal device and the "hold" state in which the output is disabled. In non-diversity mode this controls the output for the channel which is currently being monitored on the front panel. In diversity mode the combined output is controlled.

n is 0 for hold
1 for run

(2) FSK polarity — FSKPOLn / QFSKPOL

This command switches the FSK polarity. In non-diversity mode this controls the polarity for the channel which is currently being monitored on the front panel. In diversity mode both channels are controlled.

n is 0 for normal
1 for inverted

(3) Tuning meter — TMETnnn / QTMET

A 3 digit decimal number in the range 0 to 255 represents the tuning meter reading. The data should be interpreted as indicated in the table overleaf.

Value	Frequency (kHz)	Segment	
000 - 080	< 1.5	1	(left)
080 - 090	1.5 - 1.6	2	
090 - 100	1.6 - 1.7	3	
100 - 110	1.7 - 1.8	4	
110 - 120	1.8 - 1.9	5	
120 - 130	1.9 - 2.0	6	(centre)
130 - 140	2.0 - 2.1	7	
140 - 150	2.1 - 2.2	8	
150 - 160	2.2 - 2.3	9	
160 - 170	2.3 - 2.4	10	
170 - 180	2.4 - 2.5	11	
180 - 255	> 2.5	12	(right)

The frequencies quoted are nominal.

(4) Channel source

FSKCEXTn
QFSKCEXT

FSKOEXTn
QFSKOEXT

The user may select either an internal or an external signal source to feed the terminal device or drive the diversity combiner. This allows the demodulated FSK signal from an external receiver to drive the diversity combiner.

FSKCEXT applies to the sideband which is currently being monitored on the front panel. FSKOEXT applies to the other channel.

n is 0 for internal
1 for external

(5) Operational mode

FSKMODEn
QFSKMODE

This command selects the operational mode (diversity/non-diversity).

n is 1 for two independant FSK channels (eg. in a dual receiver receiving two FSK signals on different frequencies.

n is 2 for single channel reception (eg. in a single receiver). Channel A provides the output.

n is 3 for diversity mode. Channels A and B provide inputs to the diversity combiner which selects the largest signal for the output.

(6) Output polarity — FSKOUTn / QFSKOUT

This command sets up the output polarity to suit the requirements of the output device (eg. printer).

n is 0 for normal
1 for inverted

(7) FSK type — FSKFTYPn / QFSKFTYP

This command sets up the receiver to receive FSK signals in either single sideband or symmetrical mode.

n is 1 for USB. the receiver frequency is set so thst the FSK signal is centred at 2kHz in the upper sideband.

n is 2 for LSB. The receiver frequency is set so that the FSK signal is centred at -2kHz in the lower sideband.

n is 3 for symmetrical. the receiver frequency is set so that the FSK signal is centred on the frequency indicated on the front panel.

PARTS LIST

37 The Racal part number for a complete FSK Module is ST86495.

38 Information on the identification and handling of SMDs is provided in Chapter 2. The parts list for the FSK Module is as follows:

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R1		33k	Thick Film Network			934507U	
R2		33k	Thick Film Network			934507U	
R3		50k	Variable, Linear, Cermet			935105T	
R4		33k	Thick Film Network			934507U	
R5		50k	Variable, Linear, Cermet			935105T	
R6	A6	100k	Thick Film Chip	0.125	2	943914A	104
R7	A3	27k	Thick Film Chip	0.125	2	943907S	273
R8	A3	18k	Thick Film Chip	0.125	2	943905K	183
R9	A6	27k	Thick Film Chip	0.125	2	943907S	273
R10	A3	10k	Thick Film Chip	0.125	2	943902F	103
R11	A3	100k	Thick Film Chip	0.125	2	943914A	104
R12	A3	10k	Thick Film Chip	0.125	2	943902F	103
R13	A3	10k	Thick Film Chip	0.125	2	943902F	103
R14	A6	10k	Thick Film Chip	0.125	2	943902F	103
R15	B8	220k	Thick Film Chip	0.125	2	943918G	224
R16	B8	10k	Thick Film Chip	0.125	2	943902F	103
R17	B3	27k	Thick Film Chip	0.125	2	943907S	273
R18	B6	18k	Thick Film Chip	0.125	2	943905K	183
R19	B8	1k	Thick Film Chip	0.125	2	943890L	102
R20	B8	27k	Thick Film Chip	0.125	2	943907S	273
R21	B6	10k	Thick Film Chip	0.125	2	943902F	103
R22	B3	6k8	Thick Film Chip	0.125	2	943900H	682
R23	B8	4k7	Thick Film Chip	0.125	2	943898N	472
R24	B8	150R	Thick Film Chip	0.125	2	943880O	151
R25	C4	1k	Thick Film Chip	0.125	2	943890L	102
R26	C3	220k	Thick Film Chip	0.125	2	943918G	224
R27	C3	220k	Thick Film Chip	0.125	2	943918G	224
R28	C6	220k	Thick Film Chip	0.125	2	943918G	224
R29	C4	4k7	Thick Film Chip	0.125	2	943898N	472
R30	C3	150R	Thick Film Chip	0.125	2	943880O	151
R31	C2	1k	Thick Film Chip	0.125	2	943890L	102
R32	C8	6k8	Thick Film Chip	0.125	2	943900H	682
R33	D8	22k	Thick Film Chip	0.125	2	943906B	223
R34	D6	1k	Thick Film Chip	0.125	2	943890L	102
R35	D3	22k	Thick Film Chip	0.125	2	943906B	223
R36	D8	10k	Thick Film Chip	0.125	2	943902F	103
R37	D8	12k	Thick Film Chip	0.125	2	943903M	123
R38	D8	10k	Thick Film Chip	0.125	2	943902F	103
R39	D4	10k	Thick Film Chip	0.125	2	943902F	103
R40	D3	10k	Thick Film Chip	0.125	2	943902F	103
R41	D8	10k	Thick Film Chip	0.125	2	943902F	103
R42	D8	22k	Thick Film Chip	0.125	2	943906B	223
R43	D4	12k	Thick Film Chip	0.125	2	943903M	123
R44	D3	22k	Thick Film Chip	0.125	2	943906B	223
R45	E8	22k	Thick Film Chip	0.125	2	943906B	223
R46	E4	10k	Thick Film Chip	0.125	2	943902F	103
R47	E3	22k	Thick Film Chip	0.125	2	943906B	223
R48	F8	470R	Thick Film Chip	0.125	2	943886I	471
R49	F6	82k	Thick Film Chip	0.125	2	943913T	823
R50	F3	470R	Thick Film Chip	0.125	2	943886I	471
R51	F1	82k	Thick Film Chip	0.125	2	943913T	823
R52	F8	4k7	Thick Film Chip	0.125	2	943898N	472
R53	F6	22k	Thick Film Chip	0.125	2	943906B	223
R54	F5	10k	Thick Film Chip	0.125	2	943902F	103
R55	F3	4k7	Thick Film Chip	0.125	2	943898N	472
R56	F1	22k	Thick Film Chip	0.125	2	943906B	223

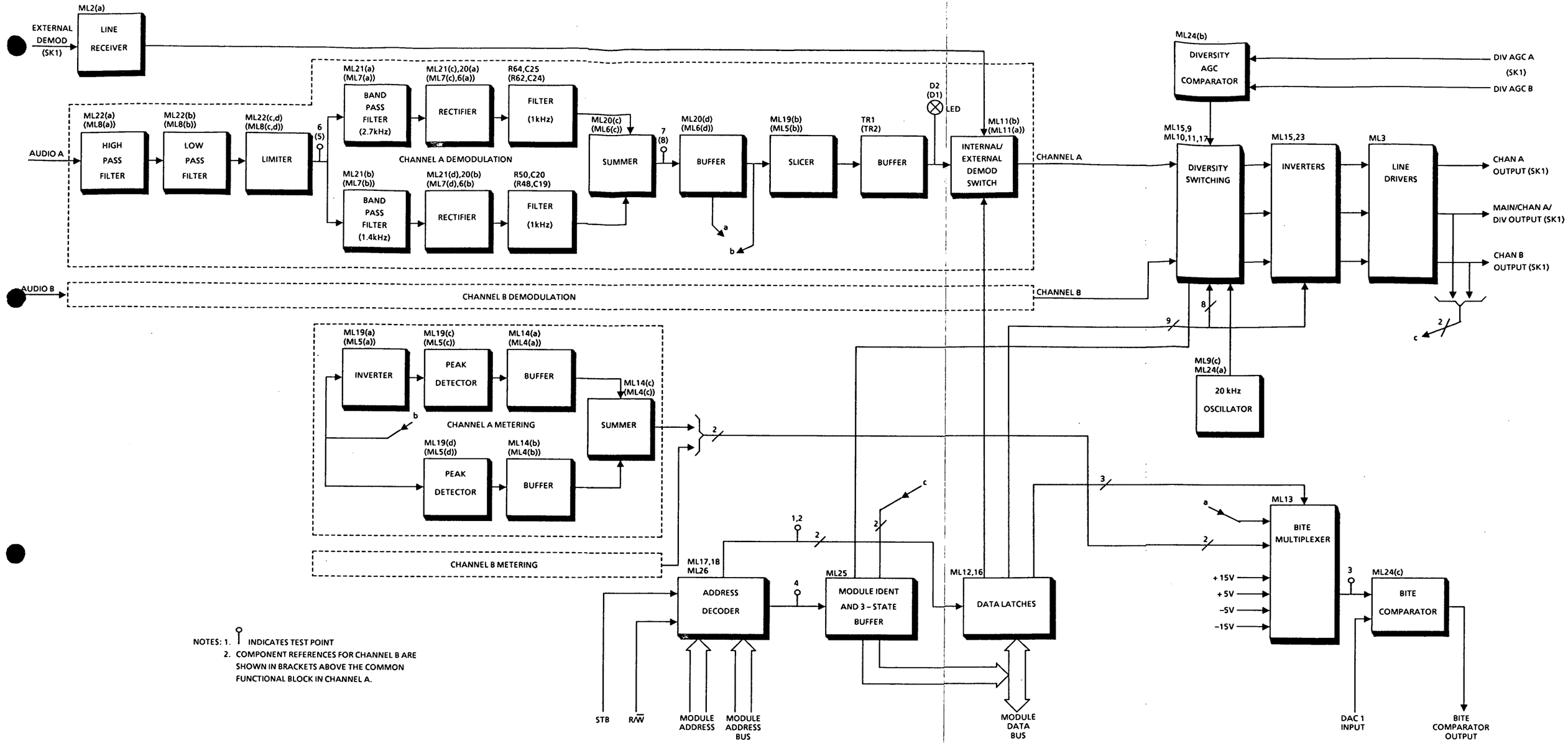
Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R57	F1	10k	Thick Film Chip	0.125	2	943902F	103
R58	G8	4k7	Thick Film Chip	0.125	2	943898N	472
R59	G6	82k	Thick Film Chip	0.125	2	943913T	823
R60	G3	4k7	Thick Film Chip	0.125	2	943898N	472
R61	G1	82k	Thick Film Chip	0.125	2	943913T	823
R62	G8	470R	Thick Film Chip	0.125	2	943886I	471
R63	G6	22k	Thick Film Chip	0.125	2	943906B	223
R64	G3	470R	Thick Film Chip	0.125	2	943886I	471
R65	G1	22k	Thick Film Chip	0.125	2	943906B	223
R66	G1	4k7	Thick Film Chip	0.125	2	943898N	472
R67	G5	4k7	Thick Film Chip	0.125	2	943898N	472
R68	G3	4k7	Thick Film Chip	0.125	2	943898N	472
R69	H8	4k7	Thick Film Chip	0.125	2	943898N	472
R70	H6	4k7	Thick Film Chip	0.125	2	943898N	472
R71	H1	4k7	Thick Film Chip	0.125	2	943898N	472
R72	H3	4k7	Thick Film Chip	0.125	2	943898N	472
R73	H8	4k7	Thick Film Chip	0.125	2	943898N	472
R74	H6	4k7	Thick Film Chip	0.125	2	943898N	472
R75	H1	4k7	Thick Film Chip	0.125	2	943898N	472
R76	H3	180k	Thick Film Chip	0.125	1	945464K	184
R77	H8	180k	Thick Film Chip	0.125	1	945464K	184
R78	H6	4k7	Thick Film Chip	0.125	2	943898N	472
R79	H3	82k	Thick Film Chip	0.125	1	945463D	823
R80	H1	4k7	Thick Film Chip	0.125	2	943898N	472
R81	H8	82k	Thick Film Chip	0.125	1	945463D	823
R82	J3	4k7	Thick Film Chip	0.125	2	943898N	472
R83	J8	4k7	Thick Film Chip	0.125	2	943898N	472
R84	J6	4k7	Thick Film Chip	0.125	2	943898N	472
R85	J1	4k7	Thick Film Chip	0.125	2	943898N	472
R86	J3	33k	Thick Film Chip	0.125	1	945462M	333
R87	J8	33k	Thick Film Chip	0.125	1	945462M	333
R88	J6	4k7	Thick Film Chip	0.125	2	943898N	472
R89	J1	4k7	Thick Film Chip	0.125	2	943898N	472
R90	J3	4k7	Thick Film Chip	0.125	1	945162B	472
R91	J8	4k7	Thick Film Chip	0.125	1	945162B	472
R92	J6	4k7	Thick Film Chip	0.125	2	943898N	472
R93	J9	2k7	Thick Film Chip	0.125	1	945459A	272
R94	J4	2k7	Thick Film Chip	0.125	1	945459A	272
R95	J1	4k7	Thick Film Chip	0.125	2	943898N	472
R96	K9	27k	Thick Film Chip	0.125	1	945461F	273
R97	K8	1k5	Thick Film Chip	0.125	1	945457S	152
R98	K4	27k	Thick Film Chip	0.125	1	945461F	273
R99	K3	1k5	Thick Film Chip	0.125	1	945457S	152
R100	K9	18k	Thick Film Chip	0.125	1	945460O	183
R101	K8	27k	Thick Film Chip	0.125	1	945461F	273
R102	K4	18k	Thick Film Chip	0.125	1	945460O	183
R103	K3	27k	Thick Film Chip	0.125	1	945461F	273
R104	K9	820R	Thick Film Chip	0.125	1	945455U	821
R105	K8	2k2	Thick Film Chip	0.125	2	943894R	222
R106	K4	820R	Thick Film Chip	0.125	1	945455U	821
R107	K3	2k2	Thick Film Chip	0.125	2	943894R	222
R108	L6	12k	Thick Film Chip	0.125	1	945465B	123
R109	L1	12k	Thick Film Chip	0.125	1	945465B	123
R110	L9	1k5	Thick Film Chip	0.125	1	945457S	152
R111	L8	10k	Thick Film Chip	0.125	2	943902F	103
R112	L4	1k5	Thick Film Chip	0.125	1	945457S	152
R113	L3	10k	Thick Film Chip	0.125	2	943902F	103

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R114	L9	2k7	Thick Film Chip	0.125	1	945459A	272
R115	L8	10k	Thick Film Chip	0.125	2	943902F	103
R116	L6	12k	Thick Film Chip	0.125	1	945465B	123
R117	L4	2k7	Thick Film Chip	0.125	1	945459A	272
R118	L3	10k	Thick Film Chip	0.125	2	943902F	103
R119	L1	12k	Thick Film Chip	0.125	1	945465B	123
R120	L9	220k	Thick Film Chip	0.125	2	943918G	224
R121	L8	220k	Thick Film Chip	0.125	2	943918G	224
R122	L4	220k	Thick Film Chip	0.125	2	943918G	224
R123	L3	220k	Thick Film Chip	0.125	2	943918G	224
R124	L1	12k	Thick Film Chip	0.125	1	945465B	123
R125	L6	18k	Thick Film Chip	0.125	1	945460O	183
R126	L3	10k	Thick Film Chip	0.125	2	943902F	103
R127	M8	10k	Thick Film Chip	0.125	2	943902F	103
R128	M1	2k2	Thick Film Chip	0.125	1	945458J	222
R129	M6	12k	Thick Film Chip	0.125	1	945465B	123
R130	M6	2k2	Thick Film Chip	0.125	1	945458J	222
R131	M1	18k	Thick Film Chip	0.125	1	945460O	183
R132	P1	100k	Thick Film Chip	0.125	2	943914A	104
R133	P3	33k	Thick Film Chip	0.125	2	943908Z	333
R134	P1	100k	Thick Film Chip	0.125	2	943914A	104
R135	P3	3k3	Thick Film Chip	0.125	2	943896P	332
R136	P1	100k	Thick Film Chip	0.125	2	943914A	104
R137	T1	22k	Thick Film Chip	0.125	2	943906B	223
R138	T8	15k	Thick Film Chip	0.125	2	943904D	153
R139	T8	10k	Thick Film Chip	0.125	2	943902F	103
R140	T3	22k	Thick Film Chip	0.125	2	943906B	223
R141	V2	22k	Thick Film Chip	0.125	2	943906B	223
R142	V7	10k	Thick Film Chip	0.125	2	943902F	103
R143	V3	22k	Thick Film Chip	0.125	2	943906B	223
R144	V7	18k	Thick Film Chip	0.125	2	943905K	183
R145	V2	18k	Thick Film Chip	0.125	2	943906B	183
R146	V8	22k	Thick Film Chip	0.125	2	943915R	223
R147	V7	120k	Thick Film Chip	0.125	2	943905K	124
R148	V3	18k	Thick Film Chip	0.125	2	943906B	183
R149	V2	22k	Thick Film Chip	0.125	2	943906B	223
R150	V7	22k	Thick Film Chip	0.125	2	943906B	223
R151	V3	22k	Thick Film Chip	0.125	2	943906B	223
R152	V2	22k	Thick Film Chip	0.125	2	943906B	223
R153	W3	22k	Thick Film Chip	0.125	2	943906B	223
R154	W2	22k	Thick Film Chip	0.125	2	943906B	223
R155	W3	22k	Thick Film Chip	0.125	2	943906B	223
R156	W2	22k	Thick Film Chip	0.125	2	943906B	223
R157	T7	10k	Thick Film Chip	0.125	2	943902F	103
Capacitors				V			
C1	A7	10n	Ceramic Chip	50	10	941775D	
C2	A4	10n	Ceramic Chip	50	10	941775D	
C3	A0	10n	Ceramic Chip	50	10	941775D	
C4	A7	10n	Ceramic Chip	50	10	941775D	
C5	A2	180p	Ceramic Chip	50	5	941802O	
C6	B2	180p	Ceramic Chip	50	5	941802O	
C7	B5	10n	Ceramic Chip	50	10	941775D	
C8	B2	180p	Ceramic Chip	50	5	941802O	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C9	B2	2µ2	Electrolitic Chip	63	-10 +50	945468Q	
C10	B7	2µ2	Electrolitic Chip	63	-10 +50	945468Q	
C11	C7	2µ2	Electrolitic Chip	63	-10 +50	945468Q	
C12	C2	2µ2	Electrolitic Chip	63	-10 +50	945468Q	
C13	C1	10n	Ceramic Chip	50	10	941775D	
C14	E3	10n	Ceramic Chip	50	10	941775D	
C15	E7	10n	Ceramic Chip	50	10	941775D	
C16	E2	10n	Ceramic Chip	50	10	941775D	
C17	E7	10n	Ceramic Chip	50	10	941775D	
C18	E1	10n	Ceramic Chip	50	10	941775D	
C19	F7	2µ2	Electrolitic Chip	63	-10 +50	945468Q	
C20	F3	2µ2	Electrolitic Chip	63	-10 +50	945468Q	
C21	G5	100n	Ceramic Chip	50	20	945146T	
C22	G1	100n	Ceramic Chip	50	20	945146T	
C23	G9	10n	Ceramic Chip	50	1	945536Q	
C24	G7	2µ2	Electrolitic Chip	63	-10 +50	945468Q	
C25	G2	2µ2	Electrolitic Chip	63	-10 +50	945468Q	
C26	G4	10n	Ceramic Chip	50	1	945536Q	
C27	H7	10n	Ceramic Chip	50	10	941775D	
C28	H2	10n	Ceramic Chip	50	10	941775D	
C29	H9	10n	Ceramic Chip	50	1	945536Q	
C30	H7	10n	Ceramic Chip	50	10	941775D	
C31	H4	10n	Ceramic Chip	50	1	945536Q	
C32	H2	10n	Ceramic Chip	50	10	941775D	
C33	H9	10n	Ceramic Chip	50	1	945536Q	
C34	H4	10n	Ceramic Chip	50	1	945536Q	
C35	J4	10n	Ceramic Chip	50	1	945536Q	
C36	J9	10n	Ceramic Chip	50	1	945536Q	
C37	J7	10n	Ceramic Chip	50	10	941775D	
C38	J3	10n	Ceramic Chip	50	10	941775D	
C39	K7	10n	Ceramic Chip	50	10	941775D	
C40	K2	10n	Ceramic Chip	50	10	941775D	
C41	K6	1n	Ceramic Chip	50	1	945535J	
C42	K1	1n	Ceramic Chip	50	1	945535J	
C43	K6	470p	Ceramic Chip	50	1	945534S	
C44	K1	470p	Ceramic Chip	50	1	945534S	
C45	K5	10n	Ceramic Chip	50	1	945536Q	
C46	K0	10n	Ceramic Chip	50	1	945536Q	
C47	L5	22n	Ceramic Chip	50	1	945537H	
C48	L0	22n	Ceramic Chip	50	1	945537H	
C49	M5	22n	Ceramic Chip	50	1	945537H	
C50	M0	22n	Ceramic Chip	50	1	945537H	
C51	M7	10n	Ceramic Chip	50	10	941775D	
C52	M3	10n	Ceramic Chip	50	10	941775D	
C53	M5	22n	Ceramic Chip	50	1	945537H	
C54	M2	10n	Ceramic Chip	50	10	941775D	
C55	M7	10n	Ceramic Chip	50	10	941775D	
C56	M0	22n	Ceramic Chip	50	1	945537H	
C57	P5	10n	Ceramic Chip	50	10	941775D	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C58	P7	10n	Ceramic Chip	50	10	941775D	
C59	P3	1n	Ceramic Chip	50	10	941772O	
C60	S2	10n	Ceramic Chip	50	10	941775D	
C61	S4	10n	Ceramic Chip	50	10	941775D	
C62	S8	10n	Ceramic Chip	50	10	941775D	
C63	T4	10n	Ceramic Chip	50	10	941775D	
C64	V5	10n	Ceramic Chip	50	10	941775D	
C65	W5	10n	Ceramic Chip	50	10	941775D	
C66	X4	10n	Ceramic Chip	50	10	941775D	
C67	X3	10µ	Tantalum Chip	35	10	945053C	
C68	X2	100n	Ceramic Chip	50	20	945146T	
C69	Y4	10n	Ceramic Chip	50	10	941775D	
C70	Y3	10µ	Tantalum Chip	35	10	945053C	
C71	Y2	100n	Ceramic Chip	50	20	945146T	
C72	Z3	10µ	Tantalum Chip	35	10	945053C	
C73	Z2	10n	Ceramic Chip	50	10	941775D	
C74	Z7	10µ	Tantalum Chip	35	10	945053C	
C75	Z3	10µ	Tantalum Chip	35	10	945053C	
C76	Z2	100n	Ceramic Chip	50	20	945146T	
Inductors							
L1	X1	3µH3	Choke		10	945030J	
L2	Y1	3µH3	Choke		10	945030J	
L3	Z1	3µH3	Choke		10	945030J	
L4	Z1	150nH	Choke		10	945182F	
Diodes							
D1			550-0406, LED Assembly			945143O	
D2			550-0406, LED Assembly			945143O	
D3	B3		BAS 16			943951D	
D4	B5		BAS 16			943951D	
D5	B4		BAS 16			943951D	
D6	C9		BAS 16			943951D	
D7	D6		BAS 16			943951D	
D8	E6		BAS 16			943951D	
D9	E9		BAS 16			943951D	
D10	E2		BAS 16			943951D	
D11	E4		BAS 16			943951D	
D12	E1		BAS 16			943951D	
D13	H1		BAS 16			943951D	
D14	H5		BAS 16			943951D	
D15	H1		BAS 16			943951D	
D16	H5		BAS 16			943951D	
D17	J1		BAS 16			943951D	
D18	J5		BAS 16			943951D	
D19	J1		BAS 16			943951D	
D20	J5		BAS 16			943951D	
D21	V8		BAS 16			943951D	
Transistors							
TR1	B3		BC 849, NPN			943941W	
TR2	C9		BC 849, NPN			943941W	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Integrated Circuits		CAUTION:	*SSD - STATIC SENSITIVE DEVICES				
ML1			7905, -5V Regulator			945150G	
ML2			26LS32, Quad Differential Line Receiver			938683N	
ML3			26LS30, Dual Differential Line Receiver			938684U	
ML4	B7		348, Quad Operational Amplifier			945466I	
ML5	D7		348, Quad Operational Amplifier			945466I	
ML6	F7		348, Quad Operational Amplifier			945466I	
ML7	J7		348, Quad Operational Amplifier			945466I	
ML8	L7		348, Quad Operational Amplifier			945466I	
ML9	P8	*SSD	74HC00, Quad 2-Input NAND Gate			943968V	
ML10	S8	*SSD	74HC74, Dual D-Type Flip-Flop			943977L	
ML11	P6	*SSD	4053, Triple 2-Channel Multiplexer			945041X	
ML12	S6	*SSD	74HC273, D-Type Flip-Flop			943989G	
ML13	V6	*SSD	4067, 16-Channel Multiplexer			945044M	
ML14	A4		348, Quad Operational Amplifier			945466I	
ML15	P5	*SSD	74HC86, Quad 2-Input Exclusive OR Gate			943979J	
ML16	S4	*SSD	74HC273, D-Type Flip-Flop			943989G	
ML17	T4	*SSD	74HC00, Quad 2-Input NAND Gate			943968V	
ML18	V4	*SSD	74HC138, 3 to 8 Line Decoder			943980X	
ML19	D2		348, Quad Operational Amplifier			945466I	
ML20	F2		348, Quad Operational Amplifier			945466I	
ML21	J2		348, Quad Operational Amplifier			945466I	
ML22	L2		348, Quad Operational Amplifier			945466I	
ML23	N2	*SSD	74HC86, Quad 2-Input Exclusive OR Gate			943979J	
ML24	P2		339, Quad Voltage Comparator			945023R	
ML25	S2	*SSD	74HC244, Octal Line Driver			943987I	
ML26	T2	*SSD	74HC85, 4-Bit Magnitude Comparator			943978S	
Connectors							
PL1			Plug, 64-Way			940339G	
SK1			Socket, 15-Way			945467Z	
Miscellaneous							
TP1 to TP8			Terminal, Assembly (test points)			936148X	



NOTES: 1. ⏀ INDICATES TEST POINT
2. COMPONENT REFERENCES FOR CHANNEL B ARE SHOWN IN BRACKETS ABOVE THE COMMON FUNCTIONAL BLOCK IN CHANNEL A.

FSK Module: Block Diagram **Fig.17.3**

CHAPTER 18

IF FILTER MODULE

CONTENTS

ILLUSTRATIONS

CHAPTER 18

IF FILTER MODULE

INTRODUCTION

1 The IF Filter Module can accommodate up to seven 1.4 MHz crystal filters which may be connected into the receiver IF path to supplement the filters fitted in the IF/AF Module. Two channels are provided for operation in dual or ISB receivers.

Fig. 18.1 Receiver Block Diagram

MODULE DESCRIPTION

2 The following description should be read in conjunction with the IF Filter Module Block and Circuit Diagrams included in this chapter. Component references shown on the Block Diagram allow it to be related to the Circuit Diagram.

IF Input Stages

3 The Channel A Input normally takes the 1.4 MHz IF signal from the Front end Module and passes it to the 1.4 MHz CRYSTAL FILTERS via the CHANNEL A INPUT BUFFER which is controlled by the bus interface. The CHANNEL B INPUT BUFFER also performs the same function if a 1.4 MHz IF signal from the second receiver in a dual receiver, is present on the Channel B Input.

IF Filter Selection

4 According to receiver requirements, up to seven 1.4 MHz CRYSTAL FILTERS may be assigned to Channel A or B, or they may be divided between Channel A and Channel B. This is achieved by the cutting of links LK2 to LK17 and the removal of LK1 during manufacture to provide the required combinations.

5 The filter bypass is used when the required filter is in the IF/AF Module or when the 12 kHz bandwidth is selected.

6 The operation of the additional filters provided by the IF Filter Module is transparent to the operator. The configuration procedure for defining these additional filters is therefore the same as that for the filters in the IF/AF Module (see Chapter 7 for details).

7 The filter selection is performed by diode switches in the FILTER SWITCHING circuits. In these circuits, unwanted filter outputs are shunted by forward biased diodes connected across the output, as determined by a logic low placed on select lines from the bus interface circuits. Unwanted filters are isolated from the others by series diodes which are reversed biased when the select lines are pulled down, thus blocking the signal.

8 For the wanted filter the appropriate shunt diode is switched out of circuit by a logic high appearing on its select line. This allows the filter output signal to pass through the now forward biased series diode to the IF output stages.

Overload Detection

9 Since the AGC is derived from the filtered IF signal, front end overload could occur if the AGC fails to act on a strong signal outside the bandwidth of the selected filter but within the bandwidth of the roofing filter (bypass mode). For each channel an OVERLOAD DETECTOR responds to this condition and provides a signal to the IF/AF Module which then drives the 1st IF AGC to cause a reduction in receiver gain.

IF Output Stages

10 The selected filter output for each channel is passed through the appropriate CHANNEL A or CHANNEL B OUTPUT SELECT circuit, which are enabled via the bus interface.

11 To compensate for losses in the filter and provide a correctly matched 1.4 MHz output at the rear panel, each channel is applied to its corresponding BUFFER AMPLIFIER. The gain of these stages is such that the overall gain of the module is 0 dB.

Bus Interface

12 A unique hardwired code is received on the Module Address input to the IF Filter Module. This code is used by the ADDRESS DECODER to detect addresses on the Module Address Bus from the Processor Module and then produce read or write pulses according to the status of the R/W input. These pulses allow the Processor to read data from the 3-STATE BUFFER or write data to the DATA LATCHES via the LEVEL SHIFTER, using the Module Data Bus. Pulses on the strobe input ensure correct timing of write pulses. The 3-STATE BUFFER gives the Processor access to the IF Filter Module identification code. The outputs of the DATA LATCHES are used to select the required channel by enabling its input and output buffers, as well as controlling a BITE MULTIPLEXER.

BITE Measurement System

13 The BITE measurement system, comprising the BITE MULTIPLEXER operating in conjunction with a BITE COMPARATOR, allows the Processor Module to measure the supply voltages of the IF FilterModule. The voltage to be measured is selected by the BITE MULTIPLEXER and compared in the BITE COMPARATOR with a voltage generated by a digital to analogue converter (DAC) in the Processor Module. The Processor measures the level of the selected voltage by applying voltages representing upper and lower limits to the comparator and then monitoring the resulting output.

14 For passband and overall module gain BITE tests on the IF Filter Module, a test signal is provided by the BFO Input. This test signal is applied via a DUAL BFO SWITCH AND ATTENUATOR at the appropriate level for injecting into the selected filter.

FAULT FINDING

General

15 Fault finding techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the IF Filter Module is contained in the following sections.

BITE Tests

16 The following BITE tests for the IF Filter Module are arranged in the order in which they are performed or presented for selection.

TEST NUMBER	:	551
TITLE	:	BITE hardware
PERFORMED	:	Continuous, unit confidence test, select test
DESCRIPTION	:	DAC 1 line is set to 2.55 volts (i.e. max). BITE multiplexer input X1 (+5 volts) is selected and the output of the BITE comparator is checked to ensure that it is low.
LIMITS	:	Less than 0.8 V at TP2.
FAULT DIRECTORY	:	Fault No. 2

TEST NUMBER : 552, 553, 554

TITLE : +5 V rail, +15 V rail, -15 V rail.

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : The appropriate BITE multiplexer input is selected and the supply voltage is checked.

LIMITS :

Test No.	Supply	Mux. Input	Mux Limits (TP2)	
			Lower	Upper
552	+ 5 V	X2	1.78 V	2.22 V
553	+ 5 V	X3	1.70 V	2.21 V
554	- 15 V	X4	1.65 V	2.24 V

FAULT DIRECTORY : Fault No. 4

Fault Directory

17 Use the following fault directory to identify the fault condition and take the necessary corrective action. Note that all inputs to the module are assumed to be correct.

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
1	Fails to run BITE tests for IF Filter Module.	Address decoding/module ident. not responding.	Check address decoding/module ident logic operation using signature analysis routine if necessary.
2	BITE hardware fault.	Comparator/multiplexer inoperative.	Use BITE test 551 to check comparator operation. Select all BITE tests for this module to check multiplexer operation for all analogue inputs. Use signature analysis routine to check multiplexer addressing.
3	BITE indicates failure but manual check shows no fault.	BITE hardware fault.	As above.
4	Power supply fault within module.	Faulty component drawing excess current or open circuit choke L1, L2 or L3.	Locate and replace faulty component.
5	Unable to select channel A or B.	Module interface faulty.	Using oscilloscope, check status of appropriate select line, or use signature analysis routine.
6	Poor sensitivity.	Low gain in signal path.	Follow the signal gain check procedure.
7	Filter selectivity fault.	(a) Filter configuration data incorrect. (b) Filters missing, damaged or fail to meet specification. (c) Filter switching circuit not functioning.	(a) Check configuration data (Chapter 7). (b) Carry out selectivity check (Chapter 4). (c) Check circuit voltage and control line levels (using oscilloscope) with each filter selected in turn.

Signal Gain Check Procedure

18 The overall channel gain should be 0 dB and may be checked as follows:

(1) Connect the 1.4 MHz output of the Front End Module directly to the IF/AF Module in order to bypass the IF Filter Module (remove the connection to PL2 on the IF/AF Module. Transfer the connection to PL2 (or PL4) on the IF Filter Module to PL2 on the IF/AF Module).

(2) Connect the AC voltmeter with 600 ohm load to the receiver line output (PL6 pins 1 and 9, IF/AF Module), or alternatively, use the front panel meter to monitor the line level.

(3) Set the receiver as follows:

Mode	:	CW
Bandwidth	:	12 kHz
AGC	:	Manual
Receiver frequency	:	0 MHz

(4) Adjust the IF GAIN control to set a reference level on the line output of 0 dBm.

(5) Reconnect the IF Filter Module into the signal path by reversing the procedure in (1) and check that the reading is within 1 dB of the reference.

(6) If the reading fails to meet the above specification, first try adjusting R3 or R4 and then refer to the circuit diagram to check the gain of each stage in the signal path. Check circuit voltages around suspect stage.

Signature Analysis Routine

19 Processor module DIL switch settings: SW1,4,7 OFF
SW2,3,5,6,8 ON

Signature analyser connections and settings:

Start: 9A Extender assembly, negative trigger
Stop: 9A Extender assembly, negative trigger
Clock: 8A Extender assembly, positive trigger
Earth: 1A Extender assembly

Note: Signatures xxxxF signify a flashing probe indicator.

Signal	Signature	Test Node				Remarks
+5V	H9A0					
0V	0000					
		DATA BUS INTERFACE				
M-D0	654F	PL1/7A	ML7/3	R105	ML13/14	Module bus
M-D1	7214	PL1/7B	ML7/5	R106	ML13/10	Module bus
M-D2	P300	PL1/6A	ML7/7	R107	ML13/6	Module bus
M-D3	1PUA	PL1/6B	ML7/9	R108	ML13/3	Module bus
M-D4	UACU	PL1/5A	ML7/12	R104	ML11/14	Module bus
M-D5	089H	PL1/5B	ML7/14	R103	ML11/10	Module bus
M-D6	718F	PL1/4A	ML7/16	R102	ML11/6	Module bus
M-D7	4H04	PL1/4B	ML7/18	R101	ML11/3	Module bus

Signature Analysis Routine (continued)

Signal	Signature	Test Node					Remarks
		ADDRESS DECODER					
M-A0	UF4A	PL1/12A	R81	ML3/14			Module address
M-A1	0CH4	PL1/12B	R79	ML3/10			Module address
M-A2	PU8U	PL1/11A	R78	ML3/6			Module address
M-A4	0000	PL1/10A	R86	ML5/10			Module address
M-A5	0001	PL1/10B	R85	ML5/12			Module address
M-A6	0001	PL1/9A	R84	ML5/13			Module address
M-A7	H9A0	PL1/9B	R83	ML5/15			Module address
MOD0	0000F	PL1/14A	R93	ML5/9			Module address
MOD1	0000	PL1/14B	R91	ML5/11			Module address
MOD2	0000	PL1/13A	R89	ML5/14			Module address
MOD3	H9A0	PL1/13B	R87	ML5/1			Module address
M-R/W	3571	PL1/8B	R75	ML8/1	ML8/2	ML9/12	Module bus
M-STB	0000F	PL1/8A	R76	ML9/1			Module bus
A=B	H9A1	ML5/6	ML9/10	ML9/13			Addr. decoder
ML8/3	PFH1	ML8/3	ML9/2				Addr. decoder
ML9/3	H9A0F	ML9/3	ML9/4	ML9/5			Addr. decoder
ML9/6	0000F	ML9/6	ML9/9				Addr. decoder
ML9/8	H9A0F	ML9/8	ML3/3				Addr. decoder
ML9/11	PFH0	ML9/11	ML7/1	ML7/19			ID Buffer
D	H9A0F	ML4/11	ML3/4				Addr. decoder
C	PU8U	ML4/12	ML3/5				Addr. decoder
B	0CH4	ML4/13	ML3/11				Addr. decoder
A	UF4A	ML4/10	ML3/13				Addr. decoder
		INTERNAL DATA BUS					
D0	654F	ML11/4	ML6/4	ML1/4	ML2/4		Data bus
D1	7214	ML11/5	ML6/6	ML1/6	ML2/6		Data bus
D2	P300	ML11/11	ML6/8	ML1/8	ML2/8		Data bus
D3	1PUA	ML11/13	ML6/10	ML1/10	ML2/10		Data bus
D4	UACU	ML13/4	ML6/16	ML1/16	ML2/16		Data bus
D5	089H	ML13/5	ML6/18	ML1/18	ML2/18		Data bus
D6	718F	ML13/11	ML6/20	ML1/20	ML2/20		Data bus
D7	4H04	ML13/13	ML6/22	ML1/22	ML2/22		Data bus
		DATA LATCH (BITE Selection) ML2					
ML2/5	59FP	ML2/5	ML10/11				CONTROL A0
ML2/7	HUC3	ML2/7	ML10/10				CONTROL A1
ML2/9	9F8H	ML2/9	ML10/9				CONTROL A2
		DATA LATCH (RF Path Selection) ML2					
A	1189	ML2/21	R63				Ch B Select
B	6HHH	ML2/17	R30				Ch A Select
C	08P6	ML2/19	R15	R35			BFO Select
		DATA LATCH (Filter Selection) ML1/ML6					
D	75UU	ML1/5	R58				Filter 15
E	UC6U	ML1/7	R65				Filter 7
F	CF27	ML1/9	R51				Filter 8
G	1U83	ML1/11	R48				Filter 9
H	4P51	ML1/17	R44				Filter 10
I	66C8	ML1/19	R40				Filter 11
J	72FF	ML1/21	R27				Filter 12
K	APC1	ML1/23	R20				Filter 13
L	11FC	ML6/5	R43				By-pass
		DATA LATCH (Output Channel Selection) ML6					
M	6529	ML6/7	R74				Channel B
P	F260	ML6/11	R18				Channel A

ALIGNMENT

20 This procedure details the adjustments required for aligning the IF Filter Module.

Test Equipment

21 The following items of test equipment, as detailed in Chapter 2, are required for aligning the IF Filter Module:

(1) AC Voltmeter.
(2) BITE Kit.

Preliminary

22 Remove the IF Filter Module from the receiver and place it on the bench next to the receiver. Remove the top cover from the module to gain access to the preset component (leave the bottom cover fitted). Reconnect the module to the receiver and connect the 1.4 MHz output of the Front End Module to PL2 on the IF/AF Module, using the extender assembly and coaxial lead provided with the BITE kit. Adjust the preset components according to the procedure below.

Channel Gain Adjustment

23 Connect the AC voltmeter to PL6 pins 1 and 9 on the IF/AF Module. Set the receiver to 0 MHz, CW, 12 kHz bandwidth and manual gain. Set the IF GAIN control for a reference reading of 0 dBm on the AC voltmeter.

24 Reconnect the IF Filter Module into the signal path, using the extension coaxial leads, and adjust R3 or R4 for 0 dBm on the AC voltmeter.

PARTS LIST

25 The Racal part number for a complete MA option IF Filter Module (excluding filters) is ST86494MA.

26 Information on the identification and handling of SMDs is provided in Chapter 2. The parts list for the IF Filter Module is as follows:

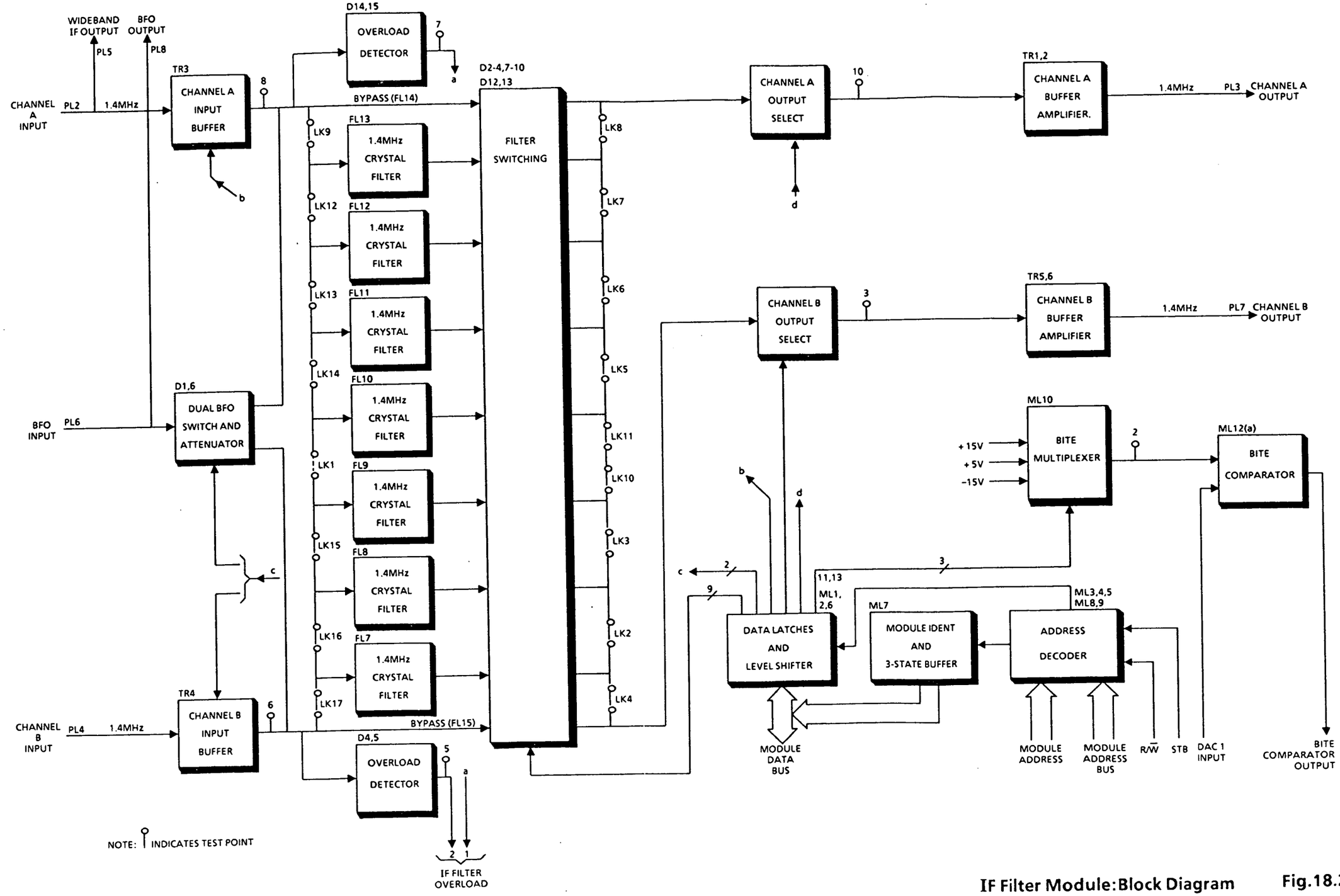
Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R1		33k	Thick Film Network			934507U	
R2		33k	Thick Film Network			934507U	
R3		500R	Variable, Linear, Cermet			940864R	
R4		500R	Variable, Linear, Cermet			940864R	
R5	A8	560R	Thick Film Chip	0.125	2	943887Z	561
R6	B8	1k	Thick Film Chip	0.125	2	943890L	102
R7	B7	1k2	Thick Film Chip	0.125	2	943891C	122
R8	B6	15k	Thick Film Chip	0.125	2	943904D	153
R9	B6	22R	Thick Film Chip	0.125	2	943869T	220
R10	B4	10k	Thick Film Chip	0.125	2	943902F	103
R11	B1	1k	Thick Film Chip	0.125	2	943890L	102
R12	B4	1k8	Thick Film Chip	0.125	2	943893A	182
R13	B4	47k	Thick Film Chip	0.125	2	943910E	473
R14	B3	47k	Thick Film Chip	0.125	2	943910E	473
R15	C5	1k	Thick Film Chip	0.125	2	943890L	102
R16	C4	470R	Thick Film Chip	0.125	2	943886I	471
R17	C7	1k8	Thick Film Chip	0.125	2	943893A	182
R18	C6	1k	Thick Film Chip	0.125	2	943890L	102
R19	C9	4k7	Thick Film Chip	0.125	2	943898N	472
R20	C8	1k	Thick Film Chip	0.125	2	943890L	102
R21	C3	10k	Thick Film Chip	0.125	2	943902F	103
R22	C3	22k	Thick Film Chip	0.125	2	943906B	223
R23	C6	4k7	Thick Film Chip	0.125	2	943898N	472
R24	C0	4k7	Thick Film Chip	0.125	2	943898N	472
R25	C0	8k2	Thick Film Chip	0.125	2	943901O	822
R26	C9	4k7	Thick Film Chip	0.125	2	943898N	472
R27	C7	1k	Thick Film Chip	0.125	2	943890L	102
R28	C5	10R	Thick Film Chip	0.125	2	943865X	100
R29	C1	470R	Thick Film Chip	0.125	2	943886I	471
R30	D3	10k	Thick Film Chip	0.125	2	943902F	103
R31	D3	100R	Thick Film Chip	0.125	2	943878J	101
R32	D2	3k3	Thick Film Chip	0.125	2	943896P	332
R33	D1	3k3	Thick Film Chip	0.125	2	943896P	332
R34	E1	1k9	Thick Film Chip	0.125	2	943890L	102
R35	E4	1k	Thick Film Chip	0.125	2	943890L	102
R36	D3	3k3	Thick Film Chip	0.125	2	943896P	332
R37	E3	3k3	Thick Film Chip	0.125	2	943896P	332
R38	F6	4k7	Thick Film Chip	0.125	2	943898N	472
R39	F2	3k3	Thick Film Chip	0.125	2	943896P	332
R40	F7	1k	Thick Film Chip	0.125	2	943890L	102
R41	F9	4k7	Thick Film Chip	0.125	2	943898N	472
R42	F1	1k	Thick Film Chip	0.125	2	943890L	102
R43	G5	1k	Thick Film Chip	0.125	2	943890L	102
R44	H7	1k	Thick Film Chip	0.125	2	943890L	102
R45	H9	4k7	Thick Film Chip	0.125	2	943898N	472
R46	H1	1k9	Thick Film Chip	0.125	2	943890L	102
R47	K9	4k7	Thick Film Chip	0.125	2	943898N	472
R48	K7	1k	Thick Film Chip	0.125	2	943890L	102
R49	K1	1k	Thick Film Chip	0.125	2	943890L	102
R50	M1	100R	Thick Film Chip	0.125	2	943878J	101
R51	M7	1k	Thick Film Chip	0.125	2	943890L	102
R52	M5	4k7	Thick Film Chip	0.125	2	943898N	472
R53	M9	4k7	Thick Film Chip	0.125	2	943898N	472
R54	M2	3k3	Thick Film Chip	0.125	2	943896P	332
R55	M1	1k	Thick Film Chip	0.125	2	943890L	102
R56	N0	470R	Thick Film Chip	0.125	2	943886I	471

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R57	N0	22k	Thick Film Chip	0.125	2	943906B	223
R58	N5	1k	Thick Film Chip	0.125	2	943890L	102
R59	N0	47k	Thick Film Chip	0.125	2	943910E	473
R60	N0	10k	Thick Film Chip	0.125	2	943902F	103
R61	N1	4k7	Thick Film Chip	0.125	2	943898N	472
R62	P1	47k	Thick Film Chip	0.125	2	943910E	472
R63	P1	10k	Thick Film Chip	0.125	2	943902F	103
R64	P9	4k7	Thick Film Chip	0.125	2	943898N	472
R65	P7	1k	Thick Film Chip	0.125	2	943890L	102
R66	R9	10R	Thick Film Chip	0.125	2	943865X	100
R67	R1	1k	Thick Film Chip	0.125	2	943890L	102
R68	S9	22R	Thick Film Chip	0.125	2	943869T	220
R69	S9	1k2	Thick Film Chip	0.125	2	943891C	102
R70	S9	15k	Thick Film Chip	0.125	2	943904D	153
R71	S8	1k8	Thick Film Chip	0.125	2	943893A	182
R72	S1	8k2	Thick Film Chip	0.125	2	943901O	822
R73	T7	4k7	Thick Film Chip	0.125	2	943898N	472
R74	T7	1k	Thick Film Chip	0.125	2	943890L	102
R75	T1	22k	Thick Film Chip	0.125	2	943906B	223
R76	V1	22k	Thick Film Chip	0.125	2	943906B	223
R77	V1	560R	Thick Film Chip	0.125	2	943887Z	561
R78	V1	22k	Thick Film Chip	0.125	2	943906B	223
R79	V1	22k	Thick Film Chip	0.125	2	943906B	223
R80	V9	1k	Thick Film Chip	0.125	2	943890L	102
R81	V1	22k	Thick Film Chip	0.125	2	943906B	223
R82	W1	33k	Thick Film Chip	0.125	2	943908Z	333
R83	W2	22k	Thick Film Chip	0.125	2	943906B	223
R84	W2	22k	Thick Film Chip	0.125	2	943906B	223
R85	W2	22k	Thick Film Chip	0.125	2	943906B	223
R86	W2	22k	Thick Film Chip	0.125	2	943906B	223
R87	W1	22k	Thick Film Chip	0.125	2	943906B	223
R88	W1	33k	Thick Film Chip	0.125	2	943908Z	333
R89	W1	22k	Thick Film Chip	0.125	2	943906B	223
R90	W1	33k	Thick Film Chip	0.125	2	943908Z	333
R91	X1	22k	Thick Film Chip	0.125	2	943906B	223
R92	X1	33k	Thick Film Chip	0.125	2	943908Z	333
R93	X1	22k	Thick Film Chip	0.125	2	943906B	223
R94	X9	100k	Thick Film Chip	0.125	2	943914A	104
R95	X9	18k	Thick Film Chip	0.125	2	943905K	183
R96	Y9	15k	Thick Film Chip	0.125	2	943904D	153
R97	Y9	10k	Thick Film Chip	0.125	2	943902F	103
R98	Y8	10k	Thick Film Chip	0.125	2	943902F	103
R99	Y8	18k	Thick Film Chip	0.125	2	943905K	183
R100	Y8	120k	Thick Film Chip	0.125	2	943915R	124
R101	Y5	22k	Thick Film Chip	0.125	2	943906B	223
R102	Y5	22k	Thick Film Chip	0.125	2	943906B	223
R103	Y5	22k	Thick Film Chip	0.125	2	943906B	223
R104	Y4	22k	Thick Film Chip	0.125	2	943906B	223
R105	Z5	22k	Thick Film Chip	0.125	2	943906B	223
R106	Z5	22k	Thick Film Chip	0.125	2	943906B	223
R107	Z5	22k	Thick Film Chip	0.125	2	943906B	223
R108	Z4	22k	Thick Film Chip	0.125	2	943906B	223
Capacitors				V			
C1	A7	100n	Ceramic Chip	50	20	945146T	
C2	B9	100n	Ceramic Chip	50	20	945146T	
C3	B2	68p	Ceramic Chip	50	5	941797F	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C4	B6	100n	Ceramic Chip	50	20	945146T	
C5	B5	100n	Ceramic Chip	50	20	945146T	
C6	B4	10n	Ceramic Chip	50	10	941775D	
C7	B3	100n	Ceramic Chip	50	20	945146T	
C8	B5	100n	Ceramic Chip	50	20	945146T	
C9	B3	10n	Ceramic Chip	50	10	941775D	
C10	C9	10n	Ceramic Chip	50	10	941775D	
C11	C9	47p	Ceramic Chip	50	5	941795H	
C12	C6	10n	Ceramic Chip	50	10	941775D	
C13	C8	10n	Ceramic Chip	50	10	941775D	
C14	C4	100n	Ceramic Chip	50	20	945146T	
C15	C3	10n	Ceramic Chip	50	10	941775D	
C16	C1	100n	Ceramic Chip	50	20	945146T	
C17	C6	10n	Ceramic Chip	50	10	941775D	
C18	C4	100n	Ceramic Chip	50	20	945146T	
C19	D1	10n	Ceramic Chip	50	10	941775D	
C20	D9	10n	Ceramic Chip	50	10	941775D	
C21	D8	47p	Ceramic Chip	50	5	941795H	
C22	D7	10n	Ceramic Chip	50	10	941775D	
C23	D5	10n	Ceramic Chip	50	10	941775D	
C24	D5	100n	Ceramic Chip	50	20	945146T	
C25	D4	1µ	Tantalum Chip	35	20	945049Z	
C26	D3	100n	Ceramic Chip	50	20	945146T	
C27	D0	10n	Ceramic Chip	50	10	941775D	
C28	E5	100n	Ceramic Chip	50	20	945146T	
C29	E2	68p	Ceramic Chip	50	5	941797F	
C30	E4	100n	Ceramic Chip	50	20	945146T	
C31	E3	100n	Ceramic Chip	50	20	945146T	
C32	F5	100n	Ceramic Chip	50	20	945146T	
C33	F3	10n	Ceramic Chip	50	10	941775D	
C34	F9	10n	Ceramic Chip	50	10	941775D	
C35	F8	47p	Ceramic Chip	50	5	941795H	
C36	F7	10n	Ceramic Chip	50	10	941775D	
C37	F5	10n	Ceramic Chip	50	10	941775D	
C38	F2	68p	Ceramic Chip	50	5	941797F	
C39	F5	10n	Ceramic Chip	50	10	941775D	
C40	G9	10n	Ceramic Chip	50	10	941775D	
C41	H9	10n	Ceramic Chip	50	10	941775D	
C42	H8	47p	Ceramic Chip	50	5	941795H	
C43	H7	10n	Ceramic Chip	50	10	941775D	
C44	H2	68p	Ceramic Chip	50	5	941797F	
C45	J5	100n	Ceramic Chip	50	20	945146T	
C46	K9	10n	Ceramic Chip	50	10	941775D	
C47	K8	47p	Ceramic Chip	50	5	941795H	
C48	K7	10n	Ceramic Chip	50	10	941775D	
C49	K2	68p	Ceramic Chip	50	5	941797F	
C50	L9	100n	Ceramic Chip	50	20	945146T	
C51	M3	100n	Ceramic Chip	50	20	945146T	
C52	L0	100n	Ceramic Chip	50	20	945146T	
C53	M0	100n	Ceramic Chip	50	20	945146T	
C54	M9	10n	Ceramic Chip	50	10	941775D	
C55	N8	47p	Ceramic Chip	50	5	941795H	
C56	M7	10n	Ceramic Chip	50	10	941775D	
C57	M5	10n	Ceramic Chip	50	10	941775D	
C58	M2	68p	Ceramic Chip	50	5	941797F	
C59	N5	10n	Ceramic Chip	50	10	941775D	
C60	N0	10n	Ceramic Chip	50	10	941775D	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C61	N9	1µ	Tantalum Chip	35	20	945049Z	
C62	P0	10n	Ceramic Chip	50	10	941775D	
C63	P0	100n	Ceramic Chip	50	20	945146T	
C64	R9	10n	Ceramic Chip	50	10	941775D	
C65	R8	47p	Ceramic Chip	50	5	941795H	
C66	R7	10n	Ceramic Chip	50	10	941775D	
C67	R2	68p	Ceramic Chip	50	5	941797F	
C68	R3	100n	Ceramic Chip	50	20	945146T	
C69	R9	100n	Ceramic Chip	50	20	945146T	
C70	R1	10n	Ceramic Chip	50	10	941775D	
C71	S9	100n	Ceramic Chip	50	20	945146T	
C72	S8	10n	Ceramic Chip	50	10	941775D	
C73	T8	10n	Ceramic Chip	50	10	941775D	
C74	V8	100n	Ceramic Chip	50	20	945146T	
C75	W9	100n	Ceramic Chip	50	20	945146T	
C76	X1	100n	Ceramic Chip	50	20	945146T	
C77	Y1	100n	Ceramic Chip	50	20	945146T	
C78	Y1	100n	Ceramic Chip	50	20	945146T	
C79	Y3	100n	Ceramic Chip	50	20	945146T	
C80	Y2	10µ	Tantalum Chip	35	10	945053C	
C81	Y3	100n	Ceramic Chip	50	20	945146T	
C82	Z1	100n	Ceramic Chip	50	20	945146T	
C83	Z1	100n	Ceramic Chip	50	20	945146T	
C84	Z3	100n	Ceramic Chip	50	20	945146T	
C85	Z2	10µ	Tantalum Chip	35	10	945053C	
C86	Z1	10n	Ceramic Chip	50	10	941775D	
C87	Z1	10n	Ceramic Chip	50	10	941775D	
C88	Z3	100n	Ceramic Chip	50	20	945146T	
Inductors				W			
L1		3µH3	Choke	0.2	10	940025C	
L2		1µH0	Choke	0.2	10	938966Z	
L3		3µH3	Choke	0.2	10	940025C	
Diodes							
D1	B5		BAW 56			943952U	
D2	C9		BAW 56			943952U	
D3	D8		BAW 56			943952U	
D4	D0		BAW 56			943952U	
D5	E0		BAS 16			943951D	
D6	E3		BAW 56			943952U	
D7	F8		BAW 56			943952U	
D8	F6		BAW 56			943952U	
D9	H8		BAW 56			943952U	
D10			BAW 56			943952U	
D11	M8		BAW 56			943952U	
D12	N5		BAW 56			943952U	
D13	P8		BAW 56			943952U	
D14	S1		BAS 16			943951D	
D15	S1		BAW 56			943952U	
D16	S7		BAS 16			943951D	
D17	S7		BAS 16			943951D	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Transistors							
TR1	B7		BC 849, NPN			943941W	
TR2	B7		BC 849, NPN			943941W	
TR3	C2		BC 849, NPN			943941W	
TR4	M0		BC 849, NPN			943941W	
TR5	T8		BC 849, NPN			943941W	
TR6	T9		BC 849, NPN			943941W	
Integrated Circuits		CAUTION:	*SSD - STATIC SENSITIVE DEVICES				
ML1	V6	*SSD	4508, Dual 4-Bit Latch			945046K	
ML2	Y6	*SSD	4508, Dual 4-Bit Latch			945046K	
ML3	W3	*SSD	40109, Quad Level Shifter			945045D	
ML4	X3	*SSD	4028, BCD to Decimal Decoder			943992C	
ML5	X2	*SSD	74HC85, 4-Bit Magnitude Comparator			943978S	
ML6	X6	*SSD	4508, Dual 4-Bit Latch			945046K	
ML7	X4	*SSD	74HC244, Octal Line Driver			943987I	
ML8	X3	*SSD	74HC00, Quad 2-Input NAND Gate			943968V	
ML9	X2	*SSD	74HC00, Quad 2-Input NAND Gate			943968V	
ML10	Y8	*SSD	4051, 8-Channel Multiplexer			943993J	
ML11	Y6	*SSD	40109, Quad Level Shifter			945045D	
ML12	Z8		339, Quad Voltage Comparator			945023R	
ML13	Z6	*SSD	40109, Quad Level Shifter			945045D	
Connectors							
PL1			Plug, 64-Way			940339G	
Miscellaneous							
W1			Cable Assembly			BA87136	
W2			Cable Assembly			BA87136	
W3			Cable Assembly			BA87136	
W4			Cable Assembly			BA87136	
W5			Cable Assembly			BA87136	
W6			Cable Assembly			BA87136	
W7			Cable Assembly			BA87136	
TP1 to TP10			Terminal, Assembly (test points)			936148X	
LK1			Comprising:				
			Plug, 4-way			945062S	
			Shorting link			943684I	



IF Filter Module: Block Diagram **Fig.18.2**

CHAPTER 19
ISB MODULE

CONTENTS

ILLUSTRATIONS

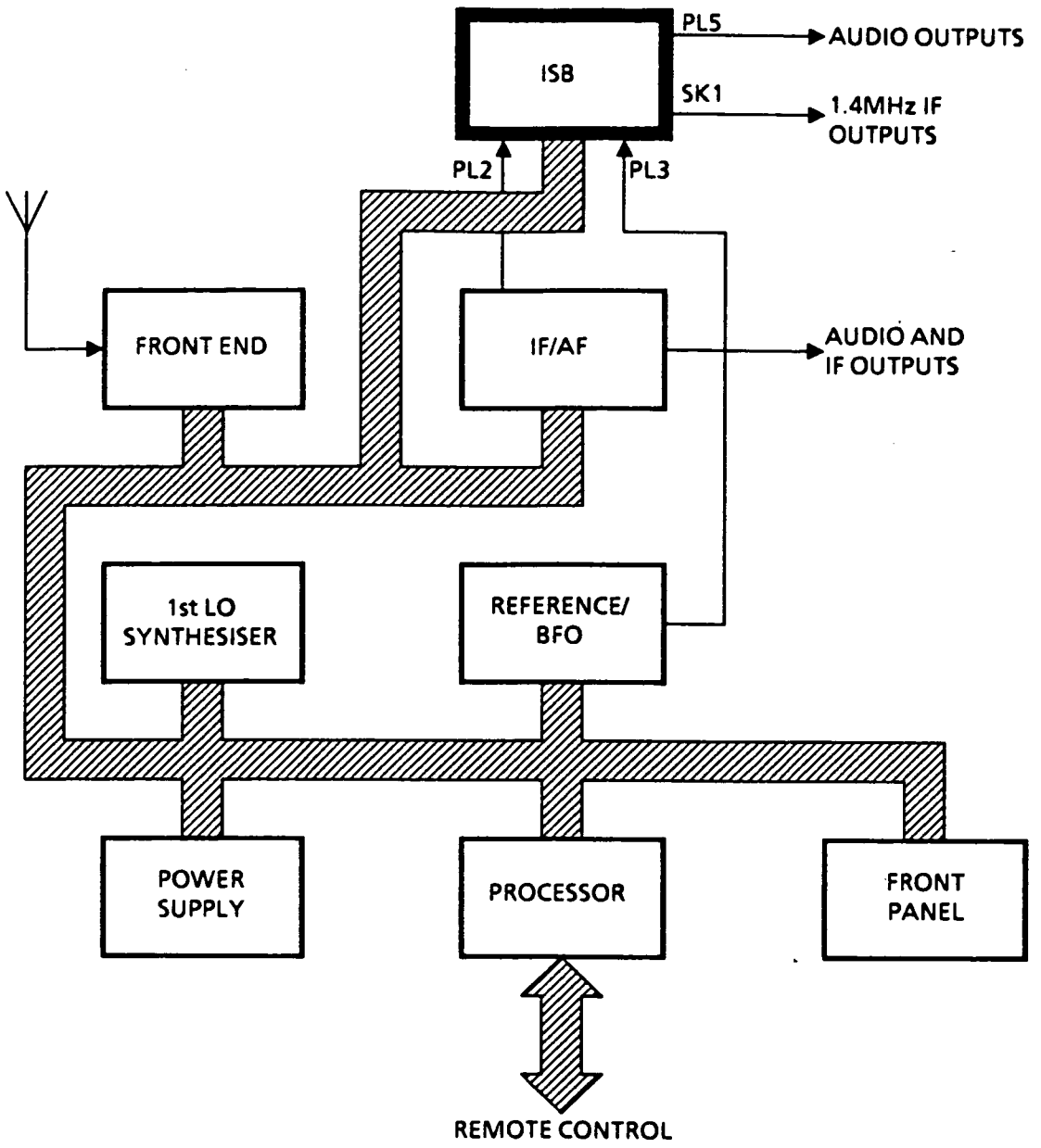


Fig. 19.1 Receiver Block Diagram

CHAPTER 19

ISB MODULE

INTRODUCTION

1 The ISB Module provides independent sideband operation for receivers in the RA3700 Series. It is substantially similar to the IF/AF Module in that it contains a second IF amplifier followed by demodulators with associated audio stages, together with the IF output and AGC circuits.

Fig 19.1 Receiver Block Diagram

MODULE DESCRIPTION

2 The following description should be read in conjunction with the ISB Module Block and Circuit Diagrams included with this chapter. Component references shown on the Block Diagram allow it to be related to the Circuit Diagram.

IF Input

3 When ISB is selected the 1.4 MHz IF input signal is taken from the output of the USB filter (FL5) in the IF/AF Module or a USB filter fitted in the IF Filter Module. As a result of sideband inversion occurring in the 1st mixer (Front End Module), the USB filter output represents the LSB of the received signal.

4 The 1.4 MHz IF input is routed to the 2nd IF amplifier stages via AMPLIFIER, BUFFER and BYPASS/FILTER SELECT circuits.

5 The AMPLIFIER is linked into the signal path when the IF input is derived from the IF/AF Module. Its nominal gain of 12 dB compensates for loss of gain through the sideband filter in the IF/AF Module. If the IF input is connected to the IF Filter Module, the AMPLIFIER is bypassed by setting links 1 and 2 accordingly. This is because the overall gain of the IF Filter Module is 0 dB, effectively resulting in no loss of gain through the sideband filter.

6 The 1.4 MHz IF input is interfaced by the emitter follower BUFFER to the BYPASS/FILTER SELECT circuit which is normally set to select the bypass input. The other input is intended for future development which may require a special filter to be fitted to a position reserved on the board.

7 In the BYPASS/FILTER SELECT circuit, the select line from the bus interface circuits is set to logic high to select the required input. This causes the shunt diode to be reversed biased and allows the now forward biased series diode to pass the signal to the IF amplifier stage.

8 For the unused input the select line is set to logic low causing its shunt diode to be forward biased and shunting the input. The select signal is prevented from affecting the other input by the now reversed biased series diode.

IF Amplifiers

9 The selected IF filter output is amplified in a two-stage differential AGC CONTROLLED AMPLIFIER. This configuration provides high gain and an AGC range of 60 dB.

10 The gain of these two differential amplifiers is controlled by a variable current source formed by ML14(c), ML3(c) and associated components. In this circuit the current through ML3(c) is proportional to the 2nd IF AGC voltage on TP8.

11 A temperature compensated bias voltage for the two tail transistors, ML2(d) and ML2(c), of the two differential amplifiers is provided by R38, R40, R27 and ML2(e). A fixed bias is also provided for both amplifiers. This is derived from ML3(d) and applied to the base of ML2(a) and ML3(a).

12 When the AGC current through ML3(c) is zero, the voltages on the base of both ML2(a) and (b) in the first amplifier stage are equal and the two transistors pass the same current giving maximum gain. As the 2nd IF AGC voltage increases, the AGC current also increases. A voltage drop occurs across R35, reducing the base voltage and therefore the current through ML2(b). This reduces the amplifier gain. The same action occurs in the second amplifier stage.

13 Thermistor R5 is included in the current source to compensate for the temperature dependent characteristics of the transistors in the two amplifier stages. The thermistor varies the AGC current in response to changes in temperature and thereby stabilises the gain of the IF amplifiers.

14 The amplified IF output is passed through an LC WIDEBAND FILTER and applied to emitter-follower BUFFER AMPLIFIER stages to provide 1.4 MHz at the rear panel IF OUT socket (SK1) at a level of 100 mV into 50 ohms

15 A buffered IF output is also taken to the demodulation circuits to produce the audio outputs.

Demodulation

16 For SSB demodulation, the BFO signal is passed through the LIMITING AMPLIFIER and fed to the carrier port of the PRODUCT DETECTOR. This removes any amplitude modulation and provides a carrier signal at the level required by the PRODUCT DETECTOR for demodulation of SSB IF signals. The IF signal is fed directly to the signal port and is mixed with the BFO signal in the PRODUCT DETECTOR to produce an audio output, which is then fed to AF stages.

AF Stages

17 The audio is first passed through an active AUDIO LOW PASS FILTER with a 3 dB point occurring at approximately 10 kHz, amplified in an AUDIO AMPLIFIER AND SQUELCH SWITCH circuit, and then directed on to the audio outputs and LINE OUTPUT AMPLIFIER by an AUDIO SELECT circuit. This circuit switches the audio through emitter follower transistor amplifiers to provide a choice of internal or external audio for the front panel loudspeaker and provide audio to optional modules. The audio levels are monitored by an AUDIO DETECTOR AND METERING circuit which rectifies and filters the audio signal to provide a DC level to the BITE multiplexer.

18 The audio power amplifier for driving the final audio outputs is contained in the Front Panel Assembly together with the volume control.

19 A two-stage operational amplifier is used as the LINE OUTPUT AMPLIFIER, its gain being adjustable by means of a preset potentiometer accessible through the top of the module. The line output is made available from a 600 ohm centre-tapped transformer.

AGC Circuit

20 The AGC circuit controls the gain of the 1st and 2nd IF amplifiers in order to maintain a constant output from the receiver as the antenna input level changes. The gain of the IF amplifiers is controlled in such a way as to obtain optimum signal to noise ratio over the entire sensitivity range of the receiver.

AGC Detection

21 The AGC DETECTOR is fed with the IF signal and provides an output in the form of a level which follows the modulation envelope of the signal.

22 Two PEAK DETECTORS followed by FAST and SLOW INTEGRATORS form the basis of the AGC control circuits.

23 When the antenna input signal increases, the output of PEAK DETECTOR 1 rises above the voltage applied by the AGC REFERENCE to the FAST INTEGRATOR, ML9(a) Pin 3, causing the output on TP19 to fall. The time constant of the integrator is determined by C49 and R85.

24 At the same time, the output of PEAK DETECTOR 2 feeds the SLOW INTEGRATOR whose output voltage falls more slowly than the FAST INTEGRATOR because of the longer time constant determined by C46 and R82.

25 In the AGC/MANUAL GAIN COMBINER the outputs of both integrators are combined such that the smallest voltage is chosen to take control. This chosen output voltage is then used, after further processing, to control the gain of the 2nd IF amplifiers. It is also passed to the IF/AF Module to control the 1st IF AGC voltage (see 'AGC Distribution').

26 After an increase in input signal, the FAST INTEGRATOR output voltage will rapidly reduce the receiver gain to restore the receiver output to the correct level. However, if it remained in control of the gain, the AGC would tend to 'follow' the signal modulation and cause distortion. To prevent this, the SLOW INTEGRATOR takes control when its output drops below that of the FAST INTEGRATOR. It does this because its PEAK DETECTOR is fed with a larger output from the AGC DETECTOR output potential divider chain (R131, R132, R136, R138).

27 When the SLOW INTEGRATOR takes control the action of ML9(c) holds the FAST INTEGRATOR output at a slightly higher level than the SLOW INTEGRATOR output, ready to respond again in the event of a further increase in signal level.

28 In addition to providing good distortion performance, this system also reduces the time the receiver is de-sensitised after a short noise spike. This is because the SLOW INTEGRATOR does not have time to respond fully and therefore have to decay with its long time constant.

29 Three AGC DECAY TIME CONSTANTS are normally switched into circuit to provide a choice of short, medium or long discharge times for the SLOW INTEGRATOR when the signal level falls.

Manual Gain

30 The MANUAL GAIN CONTROL voltage derived from the processor DAC 2 line is also combined in the AGC/MANUAL GAIN COMBINER along with any diversity AGC voltage from another receiver. A separate rear panel manual gain input is also provided for use with external equipment. This allows, for example, a control voltage from DF equipment to override the combined output voltage.

AGC Distribution

31 For the entire input signal range of the receiver the AGC DISTRIBUTION circuit distributes the AGC control voltage to the 2nd IF amplifiers as shown in Fig. 19.2 in order to achieve optimum receiver noise performance.

32 For the first 40 dB of receiver gain reduction above the AGC operating threshold the gain control is provided in the 2nd IF. Gain control for the next 80 dB is then in the 1st IF, the remaining 20 dB of gain control being again in the 2nd IF.

33 The ISB AGC B output is combined with the main AGC in the AGC DISTRIBUTION circuit in the IF/AF Module and the largest of the two, representing the strongest signal, controls the 1st IF gain. Each 2nd IF for the sidebands is then controlled separately with 40 dB of independence between them.

34 With AGC selected a signal below the AGC operating threshold results in the voltage present at the combined AGC output (TP20) being set to maximum (about +10 V). This sets the 2nd IF AGC voltage to minimum and the 1st IF AGC voltage is set to maximum by the AGC circuit in the IF/AF Module to give maximum receiver gain. As the signal level increases to above the AGC operating threshold, ML14(a) output increases to reduce the 2nd IF gain.

35 When 40 dB gain reduction is achieved by the strongest 2nd IF AGC voltage, the ISB AGC A voltage from the IF/AF Module starts to ramp down. This voltage, which controls the 1st IF AGC in the IF/AF Module, causes the threshold applied to ML14(a) Pin 3 to be reduced and results in the 2nd IF AGC voltage being held constant.

36 When the 1st IF AGC voltage and the ISB AGC A input reaches minimum, ML14(a) output once again increases to provide a reduction in 2nd IF gain up to the limit of the AGC range.

AGC Hang

37 With long AGC selected, a drop in signal level causes the AGC to 'hang' for two seconds before decaying. This function is performed by an AGC HANG circuit to which the AGC REFERENCE is applied.

38 Under AGC control, ML17(c) output charges C56 via D11. ML17(d) output is high, switching in the AGC DECAY TIME CONSTANTS to provide normal decay on the incoming signal. As soon as the signal level drops, ML17(c) output goes low. This in turn causes ML17(d) output to go low, switching the AGC DECAY TIME CONSTANTS out of circuit and the AGC hangs. This situation continues until C56 discharges via R106 and falls below the voltage set by R113 and R116, causing ML17(d) output to go high again and reconnecting the AGC DECAY TIME CONSTANTS.

39 If AGC hang is not required, TR6 is switched on to clamp ML17(d) into its high output state.

AGC Dump

40 Dump latch ML26(b) in the LINK 11 AGC AND DUMP CONTROL circuit is set by the processor after a frequency entry or mode change, or on receipt of a command from the rear panel or by remote control. The latch output activates the AGC DUMP to dump the AGC control voltage. This results in a rapid increase in gain until the IF output signal is detected once more by the AGC HANG circuit to reset the latch.

41 With the special data transmission LINK 11 AGC facility selected the decay characteristic of the AGC control voltage is modified by the action of comparator ML25(d). This occurs only in the presence of a signal 10 dB above the AGC threshold and causes the output of comparator ML25(b) to be high when enabled by the bus interface on selection of the LINK 11 AGC facility.

42 A fall in signal level is sensed by ML25(d) clocking ML25(b) output to the output of latch ML26(b), thereby activating AGC DUMP and causing a rapid discharge of the AGC control voltage. The latch output also charges C54, via R105, to provide an automatic reset facility.

Squelch and COR Operation

43 The squelch circuit operates the SQUELCH SWITCH to de-mute the audio outputs and provides an open collector 'COR' output on the rear panel connector of the Processor Module when a signal is detected above the squelch level (set by the IF gain control). Squelch is inoperative in manual AGC mode.

44 In normal AGC mode the squelch level may be set in the range -20 dB to +40 dB relative to the AGC threshold. This level is established by the DAC 2 input from the processor. In variable threshold AGC mode the squelch level is automatically set to be 3 dB above the AGC threshold.

45 For squelch levels above the AGC threshold a voltage on the DAC 2 input is taken via the MANUAL GAIN CONTROL buffer and compared in SQUELCH THRESHOLD DETECTOR 1 with the DIV AGC control voltage from the AGC/MANUAL GAIN COMBINER . In the event of squelch levels below the AGC threshold the DAC 2 voltage is compared in SQUELCH THRESHOLD DETECTOR 2 with a voltage derived from the AGC DETECTOR.

46 A SQUELCH COMPARATOR accepts the results of these comparisons and, when a signal exceeds the squelch level, presents a logic low status signal. The Processor reads the signal via the module data bus, de- muting the audio output and switching the COR output on.

47 The Processor also regularly monitors the SQUELCH COMPARATOR to detect when the signal drops below the squelch level and then, after a preset time, mutes the audio and switches off the COR.

Bus Interface

48 A unique hardwired code is received on the Module Address input to the IF/AF Module. This code is used by the ADDRESS DECODER to detect addresses on the Module Address Bus from the Processor Module and then produce read or write pulses according to the status of the R/W input. These pulses allow the Processor to read data from the 3- STATE BUFFER or write data to any DATA LATCH, using the Module Data Bus. Pulses on the strobe input ensure correct timing of write pulses. The 3-STATE BUFFER gives the Processor access to the IF/AF Module identification code and also the squelch status. The DATA LATCH outputs are used to select various functions throughout the module and to control a BITE MULTIPLEXER.

BITE Measurement System

49 The BITE measurement system, comprising the BITE MULTIPLEXER operating in conjunction with a BITE COMPARATOR, allows the Processor Module to measure various voltages and operating levels in the ISB Module. The voltage to be measured is selected by the BITE MULTIPLEXER and compared in the BITE COMPARATOR with a voltage generated by a digital to analogue converter (DAC) in the Processor Module. The Processor measures the level of the selected voltage by applying voltages representing upper and lower limits to the comparator and then monitoring the resulting output.

50 For some BITE tests, test signals generated within the receiver are injected into the ISB Module. These signals include a BFO signal applied via a BFO SWITCH AND ATTENUATOR to the IF input so that the IF amplifier gain and the back end AGC operation may be checked. For checking the demodulator a test signal is obtained from the Front End Module by tuning the receiver to 0 MHz and modulating this signal.

FAULT FINDING

General

51 Fault finding techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the ISB Module is contained in the following sections.

BITE Tests

52 The following BITE tests for the ISB Module are arranged in the order in which they are performed or presented for selection.

TEST NUMBER : 501

TITLE : BITE hardware

PERFORMED : Continuous, unit confidence test, select test

DESCRIPTION : DAC 1 line is set to 2.55 volts (i.e. max). BITE multiplexer input X1 (+ 5volts) is selected and the output of the BITE comparator is checked to ensure that it is low.

LIMITS : Less than 0.8 V at TP5.

FAULT DIRECTORY : Fault No. 2

TEST NUMBER : 502, 503, 504, 505

TITLE : + 5V rail, +15V rail, +10V rail, -15V rail.

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : The appropriate BITE multiplexer input is selected and the supply voltage is checked.

LIMITS :

Test No.	Supply	Mux. Input	Mux Limits (TP5)	
			Lower	Upper
502	+ 5 V	X2	1.78 V	2.22 V
503	+15 V	X3	1.70 V	2.21 V
504	+10 V	X4	1.90 V	2.36 V
505	- 15 V	X5	1.65 V	2.24 V

FAULT DIRECTORY : Fault No. 4

TEST NUMBER : 506

TITLE : IF amplifier

PERFORMED : Unit confidence test,select test.

DESCRIPTION : The gain of the 2nd IF amplifier is checked by tuning the receiver to 5.02 MHz and switching on the BFO input at 1.4 MHz (receiver BFO tuned to 0 kHz) through the IF amplifiers and into the AGC detector. BITE multiplexer input X10 is selected and DAC 2 input is adjusted to give a reading of between 1.90 and 1.94 V at X10. BITE multiplexer input X7 is then selected to measure the AGC detector output.

LIMITS :

Mux. Input		AGC Det. Output (TP7)	
Lower	Upper	Lower	Upper
0.2 V	-	0.2 V	-

FAULTY DIRECTORY : Fault No. 6

TEST NUMBER : 507

TITLE : 2nd IF AGC

PERFORMED : Unit confidence test, select test

DESCRIPTION : The receiver is tuned to 5.02 MHz. The first configured filter is selected and injected with the BFO signal. The first check ensures that the DIV AGC is between 1.8 and 2.1 V. If the voltage is less than 1.8 V, the BFO frequency is moved down the filter passband until the starting condition is reached. The BFO is then swept in 50 Hz steps. This attenuates the BFO signal, causing the AGC to increase the 2nd IF gain to compensate. For each step, BITE multiplexer inputs X7 and X10 are selected to measure the detected AGC and diversity AGC outputs. The detected AGC should remain constant as the diversity AGC increases. When the AGC runs out of range, the diversity AGC reaches its maximum and stays constant and for subsequent steps of the BFO the detected AGC output falls. The change in levels indicates that the 2nd IF AGC has a minimum of 30 dB AGC range (typically 40 dB).

FAULT DIRECTORY : Fault No. 7

TEST NUMBER : 508

TITLE : AGC detector

PERFORMED : Unit confidence test, select test.

DESCRIPTION : The receiver is tuned to a frequency such that the carrier appears in the centre of the LSB passband, to provide a test signal to the ISB Module. Short AGC and the peak detectors are selected. BITE multiplexer input X7 is selected to measure the AGC detector output level.

LIMITS : Peak detector output between 1.25 and 1.85 V.

FAULT DIRECTORY : Fault No. 10

TEST NUMBER : 509

TITLE : AGC distribution

PERFORMED : Unit confidence test, select test.

DESCRIPTION : The ISB Module is set to manual gain and BITE multiplexer inputs X10 (diversity AGC), and X9 (2nd IF AGC) are selected in turn at various settings of the manual gain. The levels are measured to ensure the correct distribution of gain control voltages.

LIMITS :

Manual Gain Setting	Multiplexer Inputs	
	X10	X9
2.55 V	1.76V - 2.55 V	0 V - 0.4 V
2.09 V	1.57V - 2.51 V	0.3V - 0.8 V
1.86 V	1.38V - 2.33 V	0.6V - 1.4 V
1.63 V	1.20V - 2.06 V	0.7V - 1.4 V
1.40 V	1.02V - 1.78 V	0.7V - 1.4 V
1.16 V	0.82V - 1.52 V	0.7V - 1.4 V
0.93 V	0.64V - 1.25 V	0.7V - 1.5 V
0.70 V	0.46V - 1.00 V	1.1V - 2.0 V

FAULTY DIRECTORY : Fault No. 9

TEST NUMBER	:	510
TITLE	:	AGC decay
PERFORMED	:	Unit confidence test, select test.
DESCRIPTION	:	The receiver is tuned to a frequency such that the carrier appears in the centre of the LSB passband, to provide a test signal to the ISB Module. BITE multiplexer input X10 is selected to measure the diversity AGC level. The test signal is then removed by tuning the receiver to 5.02 MHz and the diversity AGC is measured again after a delay appropriate to the decay selected. In all cases, the level is checked to ensure that it has increased by at least 350 mV (30 dB).
LIMITS	:	For 350 mV increase: Short 90 ms Medium 400 ms Long 2.5 ms Link 11 42 ms
FAULT DIRECTORY	:	Fault No. 10

TEST NUMBER	:	511
TITLE	:	AGC hang
PERFORMED	:	Unit confidence test, select test
DESCRIPTION	:	The receiver is tuned to a frequency such that the carrier appears in the centre of the LSB passband, to provide a test signal. The ISB Module is set to short decay with hang. BITE multiplexer input X10 is selected to measure the diversity AGC level. The test signal is then removed by tuning the receiver to 5.02 MHz. After 1.2 seconds the diversity AGC level is again measured to check that it is within 50 mV of the first reading. After a further 1.8 seconds another measurement is made to check that the level has increased by at least 350 mV above the first reading.
FAULT DIRECTORY	:	Fault No. 10

TEST NUMBER	:	512
TITLE	:	AGC dump
PERFORMED	:	Unit confidence test, select test
DESCRIPTION	:	The receiver is tuned to a frequency such that the carrier appears in the centre of the LSB passband, to provide a test signal. The long AGC time constant is also selected with AGC hang disabled. BITE multiplexer input X10 is selected to measure the diversity AGC level ensuring it is less than 1.63 V. The test signal is then removed by tuning the receiver to 5.02 MHz followed by an AGC dump. The diversity AGC level is again measured after a 25 ms delay ensuring that it is greater than 1.86V.
FAULT DIRECTORY	:	Fault No. 11

TEST NUMBER	:	513
TITLE	:	Product detector
PERFORMED	:	Unit confidence test,select test
DESCRIPTION	:	The receiver is tuned to a frequency such that the carrier appears in the centre of the LSB passband, to provide a test signal. The ISB Module is set to ISB mode and short time constant. A 1 kHz audio tone is produced by tuning the BFO to 1 kHz (1.401 MHz input signal). BITE multiplexer input X6 is selected to measure the audio detector output level.
LIMITS	:	0.54 V to 2.4 V at the BITE multiplexer input.
FAULT DIRECTORY	:	Fault No. 12

Fault Directory

53 Use the following fault directory to identify the fault condition and take the necessary corrective action. Note that all inputs to the module are assumed to be correct.

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
1	Fails to run BITE tests for the ISB Module.	Address decoding/module ident. not responding.	Check address decoding/module ident logic operation using oscilloscope or signature analysis routine.
2	BITE hardware fault.	Comparator/multiplexer inoperative.	Use BITE test 501 to check comparator operation. Select all BITE tests for this module to check multiplexer operation for all analogue inputs. Use signature analysis routine to check multiplexer addressing.

Fault Directory (continued)

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
3	BITE indicates failure but manual check shows no fault.	(a) BITE hardware fault. (b) Faulty BITE detector.	(a) As above. (b) Check operation of suspect BITE detector.
4	Power supply fault within module.	(a) Faulty component drawing excess current or open circuit choke L1 to L3. (b) 10V regulator on module faulty.	(a) Locate and replace faulty component. (b) Check voltages around ML1, ML17(a) and TR10.
5	Unable to select one or more functions	Module interface faulty	Check status of appropriate select line using signature analysis routine or oscilloscope.
6	Poor sensitivity	Low gain in signal path.	Run IF amplifier BITE test (506). Follow the IF gain check procedure.
7	Insufficent 2nd IF AGC range.	(a) AGC distribution incorrect. (b) Low 2nd IF gain.	(a) See Fault No. 10. (b) See Fault No. 6.
8	Detected AGC output incorrect.	(a) AGC detector inoperative. (b) Low 2nd IF gain	(a) Check voltage levels around circuit. (b) See Fault No. 6.
9	Incorrect manual gain control	(a) DAC 2 unable to set manual gain levels. (b) AGC distribution not functioning or set up correctly.	(a) Check voltage levels around manual gain control circuit. (b) Follow the AGC distribution check procedure and then check alignment.
10	AGC time constants incorrect	(a) AGC selection logic faulty (b) Slow integrator inoperative.	(a) Check switching outputs of logic control circuit. (b) Follow the AGC time constant check procedure.
11	No AGC dump.	Control voltages to link 11 and AGC dump control incorrect or AGC dump switches inoperative.	Check voltages around these circuits in accordance with the AGC time constant check procedure.
12	No SSB demodulation.	(a) Product detector faulty. (b) Limiting amplifier faulty (TR13). (c) Audio low pass filter or audio amplifier faulty.	(a) Check circuit voltages. Check IF present on TP14 and carrier present on TP8. (b) Check carrier present on TP8. (c) Check signal flow path to TP3.
13	Excessive in band IMPs.	Faulty IF amp or AGC.	Follow the in band IMP check procedure.
14	Distorted audio	Faulty demodulator (ML5) or audio stages.	Follow the distortion check procedure.
15	Squelch inoperative	(a) Squelch switch not muting audio amplifier. (b) No squelch command to processor.	(a) Check control voltage. (b) Monitor TP11 and rotate IF gain control to check operation of squelch threshold detectors/comparator.
16	Poor overall selectivity.	Misalignment in IF stages	Follow alignment procedure.

IF Gain Check Procedure

54 Select ISB and set the AGC to manual and turn the IF gain control fully clockwise. Check TP20 reads +10 V ± 250 mV. If not, carry out the AGC distribution check procedure. With amplifier TR1 in circuit, inject a 1.4 MHz test signal of –61 dBm at PL2,. terminated with 50 ohms. Connect an RF millivoltmeter set to 50 ohms input impedance to SK1 and check that the reading is in accordance with trace 3 on the signal level chart (Fig.19.3). Repeat the above procedure with the IF gain control set for +8V ± 100 mV on TP20 and a signal input of –21 dBm, again repeating for +3V ± 100 mV on TP20 and -1 dBm at the IF input, as shown in Fig.19.3 (traces 1 and 2).

55 If the output fails to meet the level shown, use the signal level chart to check the gain of each stage with the RF millivoltmeter set to high impedance. If the checks reveal a fault in the AGC controlled stages, carry out the AGC distribution check procedure to verify the 2nd AGC control voltage. For a slight deviation in gain, adjust R4 as described in the alignment procedure in an attempt to meet specification.

AGC Distribution Check Procedure

56 Set the AGC to manual, remove any signal at PL2, and turn the IF gain control fully clockwise. Check that +10V ± 250 mV is present on TP20, and 0V present on TP8. Refer to Fig. 19.2 and check that the voltages on these test points follow the graph as the IF gain control is rotated counter clockwise. If the voltages fail to follow, continue as below:

(a) Check that the voltage drop across D6 is not excessive as this will increase the time the 1st AGC voltage stays at 10V.

(b) Check the ISB IF AGC A feedback voltage from the IF/AF Module. If incorrect this may prevent the 2nd IF AGC (TP8) reaching its plateau.

57 Note that the gain reduction at the points marked on the graph in Fig. 19.2 (8V ± 250 mV on TP20) is determined by the IF/AF Module.

AGC Time Constant Check Procedure

AGC decay failure

58 Set the receiver to a frequency such that the carrier appears in the centre of the LSB passband and ISB mode. Select and short AGC. Check that the voltage on TP7 is 1.5V ± 100 mV and ML15(a) pins 2 and 3 are at 1.1V nominal. Remove the test signal by setting the receiver to 5 MHz and check that the voltages on TP7 and ML15(a) pin 2 decrease. While the AGC is regaining control, check that the voltage on TP18, and therefore the DIV AGC voltage (TP20), starts to ramp up at the rate given in the table below (a storage oscilloscope may be necessary for viewing the waveforms).

Time Constant	Voltage Change (Nominal)
Short	18.75 V/S
Medium	5V/S
Long *	0.6V/S
Link II data	47V/S
Link II normal	5V/S

* Note that a 2 second hang is automatically set in long AGC.

59 If the voltage at TP18 is correct but not at TP20, check that the manual gain voltage is not overriding the AGC/manual gain combiner.

AGC hang failure

60 Set the receiver to a frequency such that the carrier appears in the centre of the LSB passband and ISB mode. Select long AGC. Check that the voltage on TP7 is 1.5V. Remove the test signal by setting the receiver to 5 MHz and check that the voltage on TP7 decreases. The voltage on TP18 and TP20 should remain constant (hang) for a nominal 2 seconds before decaying at 0.6 V/s.

61 If the check fails, run the AGC hang BITE test (510) and monitor the level on TP10 using an oscilloscope. This should drop from +15V down to 0V for a nominal 2 seconds before reverting back to +15V and the cycle repeated. If the 0V period deviates from the 2 seconds by more than ±0.5 seconds then check the time constant components C56 and R106. If the trace is always high, check that the select line is low, switching TR6 off and thus enabling the hang circuit. If the trace is always low, check C56 is discharging via D11 and check comparator ML17(d) pin 12 is at 2.6 V. For both cases of TP10 being high or low, check the comparator operation of ML17(c) and (d).

AGC dump failure

62 Set the receiver to a frequency such that the carrier appears in the centre of the LSB passband and ISB mode. Select long AGC. Check that the voltage on TP7 is 1.5V. Remove the test signal by tuning the receiver to 5 MHz and the voltages on TP18 and TP20 should hang (assuming no failure in the AGC hang circuit). Press the ENTER key before the hang period has expired (i.e. less than 1.5 seconds) to check that the AGC dump causes the voltages on these test points to rise rapidly to 10V ± 250 mV.

63 If this check fails, run the AGC dump BITE test (511) and monitor the waveform on TP13 and TP12 using an oscilloscope. A 20 ms positive-going dump pulse should be present on TP13. If this pulse is less than 10 ns or greater than 40 ms, check the time constant components C54 and R105. If the trace is always high, check C54 is charging via R105 and produces a positive-going pulse at TP12, via D12, to reset ML26(b). If the trace is always low, check that ML26(b) SET input is being asserted to allow dump operation. If these checks prove correct and the AGC is not being dumped, check that the AGC dump signal causes the AGC dump switches (TR5, ML23 (b)) to operate correctly.

In band IMP Check Procedure

64 Excessive IMPs may be caused by one of the following:

(1) Gain fault: Carry out the IF gain check procedure to check stage gain. If a stage is providing excessive gain, check the circuit voltages around suspect stage.

(2) AGC fault: Check suspect time constant using the AGC time constant check procedure. With the receiver tuned to 0 Hz, check that the voltage on TP18 is higher than that on TP19. This verifies that the fast integrator is not in control.

Distortion Check Procedure

65 For poor distortion on ISB mode, check that a clean AGC voltage is present on TP11 and the remaining audio stages comprising the low pass filter, audio switching and output stages, do not introduce distortion to the demodulated audio signal. If these checks prove satisfactory, suspect the product detector, ML5, checking its circuit voltages before replacing.

SIGNATURE ANALYSIS ROUTINE

84

This routine checks that the module control signals are interfaced and decoded correctly from the module bus.

Processor module DIL switch settings: SW1,4,7 OFF
SW2,3,5,6,8 ON

Signature analyser connections and settings:

Start: 9A Extender assembly, negative trigger
Stop: 9A Extender assembly, negative trigger
Clock: 8A Extender assembly, positive trigger
Earth: 1A Extender assembly

Note : Signatures xxxxF signify a flashing probe indicator.

Signal	Signature	Test Node					Remarks
+5v	H9A0						
OV	0000						
		DATA BUS INTERFACES					
M-D0	503F	PL1/7A	R141	ML27/18	ML29/3		Module bus
M-D1	4764	PL1/7B	R146	ML27/16	ML29/6		Module bus
M-D2	P300	PL1/6A	R139	ML27/14	ML29/10		Module bus
M-D3	1PUA	PL1/6B	R140	ML27/12	ML29/14		Module bus
M-D4	UACU	PL1/5A	R135	ML27/9	ML28/3		Module bus
M-D5	3HPH	PL1/5B	R137	ML27/7	ML28/6		Module bus
M-D6	718F	PL1/4A	R133	ML27/5	ML28/10		Module bus
M-D7	4H04	PL1/4B	R134	ML27/3	ML28/14		Module bus
		ADDRESS DECODER					
M-A0	UF4A	PL1/12A	R163	ML33/14			Module address
M-A1	0CH4	PL1/12B	R160	ML33/10			Module address
M-A2	PU8U	PL1/11A	R157	ML33/6			Module address
M-A4	0000	PL1/10A	R159	ML30/10			Module address
M-A5	0001	PL1/10B	R156	ML30/12			Module address
M-A6	0001	PL1/9A	R153	ML30/13			Module address
M-A7	H9A0	PL1/9B	R154	ML30/15			Module address
0	0000	PL1/14A	R170	ML30/9			Module address
1	0000	PL1/14B	R171	ML30/11			Module address
2	0000	PL1/13A	R155	ML30/14			Module address
3	H9A0	PL1/13B	R168	ML30/1			Module address
M-R/W	3571	PL1/8B	R180	ML35/1	ML35/2	ML34/12	Module bus
M-STB	0000F	PL1/8A	R185	ML34/1			Module bus
A=B	H9A1	ML30/6	ML34/10	ML34/13			Addr. decoder
ML35/3	PFH1	ML35/3	ML34/2				Addr. decoder
ML34/3	H9A0	ML34/3	ML34/4	ML34/5			Addr. decoder
ML34/6	0000F	ML34/6	ML34/9				Addr. decoder

SIGNATURE ANALYSIS ROUTINE (continued)

Signal	Signature	Test Node				Remarks
		ADDRESS DECODER				
ML34/8	H9A0	ML34/8	ML33/3			Addr. decoder
ML34/11	PFH0	ML34/11	ML27/1	ML27/19		ID Buffer
D	H9A0	ML33/4	ML32/11			Addr. decoder
C	PU8U	ML33/5	ML32/12			Addr. decoder
B	0CH4	ML33/11	ML32/13			Addr. decoder
A	UF4A	ML33/13	ML32/10			Addr. decoder
		INTERNAL DATA BUS				
D0	503F	ML29/4	ML19/4	ML18/4	ML20/4	Data bus
D1	4764	ML29/5	ML19/6	ML18/6	ML20/6	Data bus
D2	P300	ML29/11	ML19/8	ML18/8	ML20/8	Data bus
D3	1PUA	ML29/13	ML19/10	ML18/10	ML20/10	Data bus
D4	UACU	ML28/4	ML19/16	ML18/16	ML20/16	Data bus
D5	3HPH	ML28/5	ML19/18	ML18/18	ML20/18	Data bus
D6	718F	ML28/11	ML19/20	ML18/20	ML20/20	Data bus
D7	4H04	ML28/13	ML19/22	ML18/22	ML20/22	Data bus
		DATA LATCH (BITE Selection) (ML20)				
0V	0000	ML20/1	ML20/3	ML20/13	ML20/15	
ML20/5	59FP	ML20/5	ML21/10			CONTROL A
ML20/7	HUC3	ML20/7	ML21/11			CONTROL B
ML20/9	9F8H	ML20/9	ML21/14			CONTROL C
ML20/11	3H12	ML20/11	ML21/13			CONTROL D
ML32/3	0000F	ML32/3	ML20/2	ML20/14		Latch Strobe
H	6HHH	ML20/17	R228			BFO Select
J	F5CA	ML20/19	ML6/9			Audio select
M	1189	ML20/21	ML12/13			Audio mute
L	6PA5	ML20/23	R20			
		DATA LATCH (AGC Selection) (ML18)				
EE	11FC	ML18/5	ML10/13			Peak 1 det.
GG	5U58	ML18/9	ML10/5			Peak 2 det.
HH	F260	ML18/11	ML23/6			Manual gain
II	0FUF	ML18/17	ML16/5			AGC decay TC
JJ	6CC2	ML18/19	ML16/6			AGC decay TC
KK	H815	ML18/21	ML16/12			AGC decay TC
LL	8U21	ML18/23	R108			Hang select
ML32/2	0000F	ML32/2	ML18/2	ML18/14		Latch Strobe

SIGNATURE ANALYSIS ROUTINE (continued)

Signal	Signature	Test Node			Remarks
		DATA LATCH (Mode and Audio Selection) (ML19)			
A	75UU	ML19/5	R14		FL16 select
B	UC6U	ML19/7	R34		Byepass select
E	4P51	ML19/17	ML12/5		Audio C select
F	66C8	ML19/19	ML12/6		Audio A select
G	72FF	ML19/21	ML12/12		Audio B select
DD	APC1	ML19/23	R97		Link 11
ML32/14	0000F	ML32/14	ML19/2	ML19/14	Latch Strobe

ALIGNMENT

66 This procedure details the adjustments required for aligning the ISB Module. The Procedures assume the 12 dB amplifier at the input of the ISB module, is linked in.

Test Equipment

67 The following items of test equipment, as detailed in Chapter 2, are required for aligning the ISB Module:

(1) Digital Multimeter.
(2) Signal Generator.
(3) RF Millivoltmeter.
(4) 50 ohm Load.
(5) BITE Kit.

Preliminary

68 Remove the ISB Module from the receiver and place it on the bench next to the receiver. Remove the top cover from the module to gain access to the preset components (leave the bottom cover fitted). Reconnect the module to the receiver using the extender assembly and coaxial leads provided with the BITE Kit. Adjust the preset components according to the procedure given below.

AGC Threshold Adjustment

69 Set the AGC to manual and turn the IF gain control fully clockwise for +10V ± 250 mV at TP20 (DIV AGC).

70 Connect the 50 ohm load and the signal generator output to PL2, set to 1.4 MHz at a level of -61 dBm (input amplifier in).

71 Adjust R4 for 100mV rms at the IF output (SK1), measured on the RF millivoltmeter set to 50 ohms input impedance.

2nd IF AGC Slope Adjustment

72 Set the AGC to manual and adjust the IF gain control for +8V ± 100 mV at TP20 (DIV AGC).

73 Connect the 50 ohm load and the signal generator output to PL2, set to 1.4 MHz at a level of -21 dBm.

74 Adjust R6 for 100 mV rms at the IF output (SK1), measured on the RF millivoltmeter set to 50 ohms input impedance.

Wideband Filter Adjustment

75 Select ISB and set the AGC to manual. Adjust the IF gain control for +10V at TP20 (DIV AGC).

76 Connect the 50 ohm load and the signal generator to PL2, set to 1.4 MHz at a level of -61 dBm.

77 Adjust L4 and L5 for peak IF output at SK1, measured on the RF millivoltmeter set to 50 ohms input impedance.

78 Increase the signal generator frequency until the RF voltmeter reading decreases by 2dB and note the frequency setting of the signal generator. Repeat for a decrease in signal generator frequency from the centre and note the frequency setting.

79 Check that the difference between the two signal generator frequency settings is 25kHz ±5kHz, symmetrical about the 1.4 MHz centre frequency.

80 Repeat the above procedure at the -30 dB points and check that the frequency difference is 200 kHz ± 5kHz. Tune the signal generator over the bandwidth to check symmetry. Re-adjust R4 and R6 as necessary.

81 If the desired bandwidth is unobtainable by the above method of adjustment, further investigation into a possible fault condition is necessary which may require the use of a tracking generator with spectrum analyser.

PARTS LIST

82 The Racal part number for a complete ISB Module is ST86490.

83 Information on the identification and handling of SMDs is provided in Chapter 2. The parts list for the ISB Module is as follows:

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R1		50k	Variable, Linear, Cermet		10	940858G	
R2		33k	Thick Film Network		2	934507U	
R3		33k	Thick Film Network		2	934507U	
R4		500R	Variable, Linear, Cermet		10	940864R	
R5		1k	-3825, Thermistor, Disc			943998W	
R6		1k0	Variable, Linear, Cermet		10	940865Y	
R7	A4	1k8	Thick Film Chip	0.125	2	943893A	182
R8	A4	10k	Thick Film Chip	0.125	2	943902F	103
R9	A4	1k2	Thick Film Chip	0.125	2	943891C	122
R10	B3	270R	Thick Film Chip	0.125	2	943883T	271
R11	B4	22R	Thick Film Chip	0.125	2	943869T	220
R12	B2	47k	Thick Film Chip	0.125	2	943910E	473
R13	B2	47k	Thick Film Chip	0.125	2	943910E	473
R14	B5	1k	Thick Film Chip	0.125	2	943890L	102
R15	C1	10k	Thick Film Chip	0.125	2	943902F	103
R16	B0	1k	Thick Film Chip	0.125	2	943890L	102
R17	C1	22k	Thick Film Chip	0.125	2	943906B	223
R18	C0	470R	Thick Film Chip	0.125	2	943886I	471
R19	C6	4k7	Thick Film Chip	0.125	2	943898N	472
R20	C2	10k	Thick Film Chip	0.125	2	943902F	103
R21	C1	100R	Thick Film Chip	0.125	2	943878J	101
R22	C1	3k3	Thick Film Chip	0.125	2	943896P	332
R23	C5	10R	Thick Film Chip	0.125	2	943865X	100
R24	C0	3k3	Thick Film Chip	0.125	2	943896P	332
R25	D8	1k	Thick Film Chip	0.125	2	943890L	102
R26	D8	4k7	Thick Film Chip	0.125	2	943898N	472
R27	D8	150R	Thick Film Chip	0.125	2	943880O	151
R28	D5	4k7	Thick Film Chip	0.125	2	943898N	472
R29	E8	3k3	Thick Film Chip	0.125	2	943896P	372
R30	E8	150R	Thick Film Chip	0.125	2	943880O	151
R31	E0	3k3	Thick Film Chip	0.125	2	943896P	332
R32	E9	10k	Thick Film Chip	0.125	2	943902F	103
R33	E9	150R	Thick Film Chip	0.125	2	943880O	151
R34	E4	1k	Thick Film Chip	0.125	2	943890L	102
R35	E8	120R	Thick Film Chip	0.125	2	943879Q	121
R36	F8	220R	Thick Film Chip	0.125	2	943882M	221
R37	F8	4k7	Thick Film Chip	0.125	2	943898N	472
R38	F8	4k7	Thick Film Chip	0.125	2	943898N	472
R39	F8	47R	Thick Film Chip	0.125	2	943873W	470
R40	G9	2k2	Thick Film Chip	0.125	2	943894R	222
R41	G8	220R	Thick Film Chip	0.125	2	943882M	221
R42			Not used				
R43			Not used				
R44	H8	4k7	Thick Film Chip	0.125	2	943898N	472
R45			Not used				
R46			Not used				
R47			Not used				
R48	H8	1k5	Thick Film Chip	0.125	2	943892J	152
R49	J8	1k	Thick Film Chip	0.125	2	943890L	102
R50	J1	33k	Thick Film Chip	0.125	2	943908Z	333
R51	J0	27k	Thick Film Chip	0.125	2	943907S	273
R52	J3	100k	Thick Film Chip	0.125	2	943914A	104
R53	J8	27k	Thick Film Chip	0.125	2	943907S	273
R54	J4	1k	Thick Film Chip	0.125	2	943890L	102
R55	J2	100k	Thick Film Chip	0.125	2	943914A	104
R56	J1	10k	Thick Film Chip	0.125	2	943902F	103

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R57	J1	33k	Thick Film Chip	0.125	2	943908Z	333
R58	J6	100k	Thick Film Chip	0.125	2	943914A	104
R59	J6	100k	Thick Film Chip	0.125	2	943914A	104
R60	J9	56k	Thick Film Chip	0.125	2	943911V	563
R61	K8	22R	Thick Film Chip	0.125	2	943869T	220
R62	K5	33k	Thick Film Chip	0.125	2	943908Z	333
R63	K9	33R	Thick Film Chip	0.125	2	943871Y	330
R64	K9	56k	Thick Film Chip	0.125	2	943911V	563
R65	K7	100k	Thick Film Chip	0.125	2	943914A	104
R66	K7	10k	Thick Film Chip	0.125	2	943902F	103
R67	K6	1k5	Thick Film Chip	0.125	2	943892J	152
R68	K5	6k8	Thick Film Chip	0.125	2	943900H	682
R69	K4	39k	Thick Film Chip	0.125	2	943909Q	393
R70	K4	150k	Thick Film Chip	0.125	2	943916I	154
R71	K9	4k7	Thick Film Chip	0.125	2	943898N	472
R72	K3	2k7	Thick Film Chip	0.125	2	943895Y	272
R73	L1	150k	Thick Film Chip	0.125	2	943916I	154
R74	L0	6k8	Thick Film Chip	0.125	2	943900H	682
R75	L0	1k8	Thick Film Chip	0.125	2	943893A	182
R76	K7	10k	Thick Film Chip	0.125	2	943902F	103
R77	L1	1k5	Thick Film Chip	0.125	2	943892J	152
R78	L1	1k	Thick Film Chip	0.125	2	943890L	102
R79	L1	100k	Thick Film Chip	0.125	2	943914A	104
R80	L0	150k	Thick Film Chip	0.125	2	943916I	154
R81	L0	10k	Thick Film Chip	0.125	2	943902F	103
R82	L5	6k8	Thick Film Chip	0.125	2	943900H	682
R83	L4	330R	Thick Film Chip	0.125	2	943884K	331
R84	L7	220k	Thick Film Chip	0.125	2	943918G	221
R85	L6	22k	Thick Film Chip	0.125	2	943906B	223
R86	L6	4k7	Thick Film Chip	0.125	2	943898N	472
R87	L5	22k	Thick Film Chip	0.125	2	943906B	223
R88	L2	1k2	Thick Film Chip	0.125	2	943891C	122
R89	L1	47k	Thick Film Chip	0.125	2	943910E	472
R90	M5	220k	Thick Film Chip	0.125	2	943918G	221
R91	M5	47k	Thick Film Chip	0.125	2	943910E	473
R92	M4	3k3	Thick Film Chip	0.125	2	943896P	332
R93	M1	4k7	Thick Film Chip	0.125	2	943898N	472
R94	M0	22k	Thick Film Chip	0.125	2	943906B	223
R95	M0	33k	Thick Film Chip	0.125	2	943908Z	333
R96	M1	8k2	Thick Film Chip	0.125	2	943901O	822
R97	M3	10k	Thick Film Chip	0.125	2	943902F	103
R98	M3	10k	Thick Film Chip	0.125	2	943902F	103
R99	M2	4k7	Thick Film Chip	0.125	2	943898N	472
R100	M2	1k8	Thick Film Chip	0.125	2	943893A	182
R101	M5	10k	Thick Film Chip	0.125	2	943902F	103
R102	M2	1M	Thick Film Chip	0.125	5	945100R	105
R103	M6	47k	Thick Film Chip	0.125	2	943910E	473
R104	M6	12k	Thick Film Chip	0.125	2	943903M	123
R105	M1	220k	Thick Film Chip	0.125	2	943918G	224
R106	M4	150k	Thick Film Chip	0.125	2	943916I	154
R107	M4	27k	Thick Film Chip	0.125	2	943907S	273
R108	M3	22k	Thick Film Chip	0.125	2	943906B	223
R109	M8	10k	Thick Film Chip	0.125	2	943902F	103
R110	N8	10k	Thick Film Chip	0.125	2	943902F	103
R111	N8	22R	Thick Film Chip	0.125	2	943869T	220
R112	N7	1k	Thick Film Chip	0.125	2	943890L	102
R113	N4	47k	Thick Film Chip	0.125	2	943910E	473

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R114	N2	33k	Thick Film Chip	0.125	2	943908Z	333
R115	N5	10k	Thick Film Chip	0.125	2	943902F	103
R116	N4	10k	Thick Film Chip	0.125	2	943902F	103
R117	N5	47k	Thick Film Chip	0.125	2	943910E	473
R118	N8	5k6	Thick Film Chip	0.125	2	943899E	473
R119	N1	10k	Thick Film Chip	0.125	2	943902F	103
R120	P9	1k	Thick Film Chip	0.125	2	943890L	102
R121	P8	1k	Thick Film Chip	0.125	2	943890L	102
R122	P9	1k	Thick Film Chip	0.125	2	943890L	102
R123	P8	10k	Thick Film Chip	0.125	2	943902F	103
R124	P8	560R	Thick Film Chip	0.125	2	943887Z	561
R125	P5	10k	Thick Film Chip	0.125	2	943902F	103
R126	P5	1k2	Thick Film Chip	0.125	2	943891C	122
R127	P5	100R	Thick Film Chip	0.125	2	943878J	101
R128	P4	10R	Thick Film Chip	0.125	2	943865X	100
R129	P9	22R	Thick Film Chip	0.125	2	943869T	220
R130	R8	39R	Thick Film Chip	0.125	2	943872F	390
R131	R8	1k	Thick Film Chip	0.125	2	943890L	102
R132	R8	5k6	Thick Film Chip	0.125	2	943899E	562
R133	R2	22k	Thick Film Chip	0.125	2	943906B	223
R134	R2	22k	Thick Film Chip	0.125	2	943906B	223
R135	R2	22k	Thick Film Chip	0.125	2	943906B	223
R136	R8	820R	Thick Film Chip	0.125	2	943889X	821
R137	R2	22k	Thick Film Chip	0.125	2	943906B	223
R138	R8	3k3	Thick Film Chip	0.125	2	943896P	332
R139	S2	22k	Thick Film Chip	0.125	2	943906B	223
R140	S2	22k	Thick Film Chip	0.125	2	943906B	223
R141	S2	22k	Thick Film Chip	0.125	2	943906B	223
R142	S9	10k	Thick Film Chip	0.125	2	943902F	103
R143	S9	1k	Thick Film Chip	0.125	2	943890L	102
R144	S8	820R	Thick Film Chip	0.125	2	943889X	821
R145	S8	47R	Thick Film Chip	0.125	2	943873W	470
R146	S2	22k	Thick Film Chip	0.125	2	943906B	223
R147	S8	470R	Thick Film Chip	0.125	2	943886I	471
R148	S8	6k8	Thick Film Chip	0.125	2	943900H	682
R149	S8	3k3	Thick Film Chip	0.125	2	943896P	332
R150	S7	330R	Thick Film Chip	0.125	2	943884K	331
R151	S7	470R	Thick Film Chip	0.125	2	943886I	471
R152	T9	3k3	Thick Film Chip	0.125	2	943896P	332
R153	T3	22k	Thick Film Chip	0.125	2	943906B	223
R154	T2	22k	Thick Film Chip	0.125	2	943906B	223
R155	T3	22k	Thick Film Chip	0.125	2	943906B	223
R156	T2	22k	Thick Film Chip	0.125	2	943906B	223
R157	T2	22k	Thick Film Chip	0.125	2	943906B	223
R158	T7	56R	Thick Film Chip	0.125	2	943875U	560
R159	T3	22k	Thick Film Chip	0.125	2	943906B	223
R160	T2	22k	Thick Film Chip	0.125	2	943906B	223
R161	T1	33k	Thick Film Chip	0.125	2	943908Z	333
R162	T7	1k	Thick Film Chip	0.125	2	943890L	102
R163	T3	22k	Thick Film Chip	0.125	2	943906B	223
R164	V9	3k3	Thick Film Chip	0.125	2	943896P	332
R165	V8	3k3	Thick Film Chip	0.125	2	943896P	332
R166	V8	390R	Thick Film Chip	0.125	2	943885B	391
R167	V8	3k3	Thick Film Chip	0.125	2	943896P	332
R168	T2	22k	Thick Film Chip	0.125	2	943906B	223
R169	T1	33k	Thick Film Chip	0.125	2	943908Z	333
R170	V3	22k	Thick Film Chip	0.125	2	943906B	223
R171	V2	22k	Thick Film Chip	0.125	2	943906B	223

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R172	V1	33k	Thick Film Chip	0.125	2	943908Z	333
R173	V7	1k2	Thick Film Chip	0.125	2	943891C	122
R174	V1	33k	Thick Film Chip	0.125	2	943908Z	333
R175	V7	2k2	Thick Film Chip	0.125	2	943894R	222
R176	V7	3k9	Thick Film Chip	0.125	2	943897W	392
R177	V2	10k	Thick Film Chip	0.125	2	943902F	103
R178	W6	100k	Thick Film Chip	0.125	2	943914A	104
R179	W6	18k	Thick Film Chip	0.125	2	943905K	183
R180	W2	22k	Thick Film Chip	0.125	2	943906B	223
R181	W2	10k	Thick Film Chip	0.125	2	943902F	103
R182	W6	10k	Thick Film Chip	0.125	2	943902F	103
R183	X6	47k	Thick Film Chip	0.125	2	943910E	473
R184	X5	10k	Thick Film Chip	0.125	2	943902F	103
R185	X2	22k	Thick Film Chip	0.125	2	943906B	223
R186	X7	220k	Thick Film Chip	0.125	2	943918G	224
R187	X6	150k	Thick Film Chip	0.125	2	943916I	154
R188	X7	330k	Thick Film Chip	0.125	2	943920L	334
R189	X5	18k	Thick Film Chip	0.125	2	943905K	183
R190	X5	15k	Thick Film Chip	0.125	2	943904D	153
R191	X5	10k	Thick Film Chip	0.125	2	943902F	103
R192	X4	10k	Thick Film Chip	0.125	2	943902F	103
R193	X4	120k	Thick Film Chip	0.125	2	943915R	124
R194	X4	100k	Thick Film Chip	0.125	2	943914A	104
R195	X4	27k	Thick Film Chip	0.125	2	943907S	273
R196	X8	47k	Thick Film Chip	0.125	2	943910E	473
R197	X9	3k3	Thick Film Chip	0.125	2	943896P	332
R198	X8	100k	Thick Film Chip	0.125	2	943914A	104
R199	Y4	1k5	Thick Film Chip	0.125	2	943892J	152
R200	Y4	1k5	Thick Film Chip	0.125	2	943892J	152
R201	Y2	330k	Thick Film Chip	0.125	2	943920L	334
R202	Y2	33k	Thick Film Chip	0.125	2	943908Z	333
R203	Y5	47k	Thick Film Chip	0.125	2	943910E	473
R204	Y4	1k5	Thick Film Chip	0.125	2	943892J	152
R205	Y4	10k	Thick Film Chip	0.125	2	943902F	103
R206	Y4	6k8	Thick Film Chip	0.125	2	943900H	682
R207	Y3	150R	Thick Film Chip	0.125	2	943880O	151
R208	Y8	8k2	Thick Film Chip	0.125	2	943901O	822
R209	Y8	4k7	Thick Film Chip	0.125	2	943898N	472
R210	Y5	1k	Thick Film Chip	0.125	2	943890L	102
R211	Y2	100k	Thick Film Chip	0.125	2	943914A	104
R212	Y2	33k	Thick Film Chip	0.125	2	943908Z	333
R213	X9	10k	Thick Film Chip	0.125	2	943902F	103
R214	Y4	8k2	Thick Film Chip	0.125	2	943901O	822
R215	Z8	100k	Thick Film Chip	0.125	2	943914A	104
R216	Y5	47k	Thick Film Chip	0.125	2	943910E	473
R217	Z3	100k	Thick Film Chip	0.125	2	943914A	104
R218	Z9	2k2	Thick Film Chip	0.125	2	943894R	222
R219	Z5	1k	Thick Film Chip	0.125	2	943890L	102
R220	Z2	10k	Thick Film Chip	0.125	2	943902F	103
R221	Z2	100k	Thick Film Chip	0.125	2	943914A	104
R222	Z5	47k	Thick Film Chip	0.125	2	943910E	473
R223	Z5	1k	Thick Film Chip	0.125	2	943890L	102
R224	Z8	10R	Thick Film Chip	0.125	2	943865X	100
R225	Z2	56k	Thick Film Chip	0.125	2	943911V	563
R226	Z2	330k	Thick Film Chip	0.125	2	943920L	334
R227	Z5	10k	Thick Film Chip	0.125	2	943902F	103
R228	Z9	1k	Thick Film Chip	0.125	2	943890L	102
R229	Z5	100k	Thick Film Chip	0.125	2	943914A	104
R230	Z4	10R	Thick Film Chip	0.125	2	943865X	100

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C1		470µ	Electrolitic Tubular	40	-10 +50	941812L	
C2		470µ	Electrolitic Tubular	40	-10 +50	941812L	
C3	A1	10n	Ceramic Chip	50	10	941775D	
C4	A3	10n	Ceramic Chip	50	10	941775D	
C5	B3	100n	Ceramic Chip	50	10	945146T	
C6	B2	10n	Ceramic Chip	50	10	941775D	
C7	B7	47p	Ceramic Chip	50	5	941795H	
C8	B6	10n	Ceramic Chip	50	10	941775D	
C9	B1	68p	Ceramic Chip	50	5	941797F	
C10	B7	10n	Ceramic Chip	50	10	941775D	
C11	C2	10n	Ceramic Chip	50	10	941775D	
C12	C0	100n	Ceramic Chip	50	20	945146T	
C13	C5	10n	Ceramic Chip	50	10	941775D	
C14	C1	100n	Ceramic Chip	50	20	945146T	
C15	C0	10n	Ceramic Chip	50	10	941775D	
C16	C8	10n	Ceramic Chip	50	10	941775D	
C17	D5	1µ	Tantalum Chip	35	20	945049Z	
C18	D5	100n	Ceramic Chip	50	20	945146T	
C19	D9	100n	Ceramic Chip	50	20	945146T	
C20	D8	10n	Ceramic Chip	50	10	941775D	
C21	E4	10n	Ceramic Chip	50	10	941775D	
C22	E5	10n	Ceramic Chip	50	10	941775D	
C23	E9	10n	Ceramic Chip	50	10	941775D	
C24	F9	10n	Ceramic Chip	50	10	941775D	
C25	E8	10n	Ceramic Chip	50	10	941775D	
C26	F8	100n	Ceramic Chip	50	20	945146T	
C27	F9	1µ	Tantalum Chip	35	20	945049Z	
C28	F8	10n	Ceramic Chip	50	10	941775D	
C29	F9	100n	Ceramic Chip	50	20	945146T	
C30	G9	10n	Ceramic Chip	50	10	941775D	
C31	G8	10n	Ceramic Chip	50	10	941775D	
C32	H8	4µ7	Tantalum Chip	35	20	945051E	
C33	H9	10n	Ceramic Chip	50	10	941775D	
C34	J0	10n	Ceramic Chip	50	10	941775D	
C35	J1	100n	Ceramic Chip	50	20	945146T	
C36	J9	10n	Ceramic Chip	50	10	941775D	
C37	J2	100n	Ceramic Chip	50	20	945146T	
C38	J8	2p2	Ceramic Chip	50	0.25	941781E	
C39	J6	10n	Ceramic Chip	50	10	941775D	
C40	J6	10n	Ceramic Chip	50	10	941775D	
C41	K4	10n	Ceramic Chip	50	10	941775D	
C42	K9	10n	Ceramic Chip	50	10	941775D	
C43	K4	10n	Ceramic Chip	50	10	941775D	
C44	K2	10n	Ceramic Chip	50	10	941775D	
C45	K1	10n	Ceramic Chip	50	10	941775D	
C46	L5	3µ3	Tantalum Chip	16	20	945050N	
C47	L8	1n5	Ceramic Chip	50	5	945148B	
C48	L8	100n	Ceramic Chip	50	20	945146T	
C49	L6	100n	Ceramic Chip	50	20	945146T	
C50	L8	22p	Ceramic Chip	50	5	941791L	
C51	L1	10n	Ceramic Chip	50	10	941775D	
C52	M3	100n	Ceramic Chip	50	20	945146T	
C53	M8	1n5	Ceramic Chip	50	5	945148B	
C54	M0	100n	Ceramic Chip	50	20	945146T	
C55	M8	10n	Ceramic Chip	50	10	941775D	
C56	N4	10µ	Tantalum Chip	35	10	945053C	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Capacitors				V			
C57	N2	100n	Ceramic Chip	50	20	945146T	
C58	N9	4µ7	Tantalum Chip	16	20	945051E	
C59	N0	100n	Ceramic Chip	50	20	945146T	
C60	N8	10n	Ceramic Chip	50	10	941775D	
C61	N1	10n	Ceramic Chip	50	10	941775D	
C62	P5	100n	Ceramic Chip	50	20	945146T	
C63	P4	100n	Ceramic Chip	50	20	945146T	
C64	P9	100n	Ceramic Chip	50	20	945146T	
C65	P8	100n	Ceramic Chip	50	20	945146T	
C66	P5	10n	Ceramic Chip	50	10	941775D	
C67	R2	10n	Ceramic Chip	50	10	941775D	
C68	S7	10n	Ceramic Chip	50	10	941775D	
C69	S9	10n	Ceramic Chip	50	10	941775D	
C70	S8	100n	Ceramic Chip	50	20	945146T	
C71	S9	10n	Ceramic Chip	50	10	941775D	
C72	S9	10n	Ceramic Chip	50	10	941775D	
C73	S7	10n	Ceramic Chip	50	10	941775D	
C74	S7	10n	Ceramic Chip	50	10	941775D	
C75	T7	100n	Ceramic Chip	50	20	945146T	
C76	T8	100n	Ceramic Chip	50	20	945146T	
C77	T7	100n	Ceramic Chip	50	20	945146T	
C78	V9	10n	Ceramic Chip	50	10	941775D	
C79	W7	6µ8	Tantalum Chip	16	20	945147K	
C80	X9	6µ8	Tantalum Chip	16	20	945147K	
C81	X7	100n	Ceramic Chip	50	20	945146T	
C82	X6	1µ	Tantalum Chip	35	20	945049Z	
C83	X8	10n	Ceramic Chip	50	10	941775D	
C84	X2	10n	Ceramic Chip	50	10	941775D	
C85	Y1	100n	Ceramic Chip	50	20	945146T	
C86	Y1	100n	Ceramic Chip	50	20	945146T	
C87	Y0	100n	Ceramic Chip	50	20	945146T	
C88	Y7	1n5	Ceramic Chip	50	5	945148B	
C89	Y7	2n7	Ceramic Chip	50	10	945149I	
C90	Y1	100n	Ceramic Chip	50	20	945146T	
C91	Y1	100n	Ceramic Chip	50	20	945146T	
C92	Y0	100n	Ceramic Chip	50	20	945146T	
C93	Z8	100n	Ceramic Chip	50	20	945146T	
C94	Z1	33µ	Tantalum Chip	10	20	945054T	
C95	Z1	10µ	Tantalum Chip	35	10	945053C	
C96	Z0	10µ	Tantalum Chip	35	10	945053C	
C97	Z4	10µ	Tantalum Chip	35	10	945053C	
C98	Z8	100n	Ceramic Chip	50	20	945146T	
C99	Z9	100n	Ceramic Chip	50	20	945146T	
Inductors				W			
L1		3µH3	Choke	0.2	10	940025C	
L2		1µH0	Choke	0.2	10	938966Z	
L3		3µH3	Choke	0.2	10	940025C	
L4		-	Coil Assembly			ST87451	
L5		-	Coil Assembly			ST87451	
Transformers							
T1			Transformer Assembly			ST87452	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Diodes							
D1	C6		BAW 56			943952U	
D2	D2		BAS 16			943951D	
D3	E5		BAW 56			943952U	
D4	K3		BAS 16			943951D	
D5	K6		BAW 56			943952U	
D6	L2		BAS 16			943951D	
D7	L7		BAS 16			943951D	
D8	M2		BZX84-C 3V3, Zener			945103W	
D9	M1		BAS 16			943951D	
D10	M6		BAS 16			943951D	
D11	N5		BAS 16			943951D	
D12	N0		BAW 56			943952U	
D13	N6		BAS 16			943951D	
D14	W6		BAS 16			943951D	
D15	X7		BAS 16			943951D	
D16	Z9		BAS 16			943951D	
Transistors							
TR1	A3		BC 849, NPN			943941W	
TR2	C1		BC 849, NPN			943941W	
TR3	J8		BC 849, NPN			943941W	
TR4	K8		BC 849, NPN			943941W	
TR5	L5		BC 849, NPN			943941W	
TR6	N3		BC 849, NPN			943941W	
TR7	N8		BC 849, NPN			943941W	
TR8	N8		BC 849, NPN			943941W	
TR9	P8		BC 849, NPN			943941W	
TR10	P4		BC 849, NPN			943941W	
TR11	P8		BC 849, NPN			943941W	
TR12	S8		BC 849, NPN			943941W	
TR13	T6		BC 849, NPN			943941W	
TR14	Y5		BC 849, NPN			943941W	
TR15	Y5		BC 849, NPN			943941W	
TR16	Z5		BC 849, NPN			943941W	
Integrated Circuits			CAUTION: *SSD - STATIC SENSITIVE DEVICES				
ML1			01, +10V Reference			945020M	
ML2	E8		3046, Transistor Array			945025P	
ML3	G8		3046, Transistor Array			945025P	
ML4	S9		3046, Transistor Array			945025P	
ML5	T8		1496, Balanced Modulator/Demodulator			945027X	
ML6	X8	*SSD	4053, Triple 2-Channel Multiplexer			945041X	
ML7	Y7		1458, Dual Operational Amplifier			945022K	
ML8	Z8		1458, Dual Operational Amplifier			945022K	
ML9	L6		1458, Dual Operational Amplifier			945022K	
ML10	M6	*SSD	4066, Quad Bilateral Switch			945043V	
ML11	N6		324, Quad Operational Amplifier			945026G	
ML12	Y6	*SSD	4066, Quad Bilateral Switch			945043V	
ML13			Not used				
ML14	K4		324, Quad Operational Amplifier			945026G	
ML15	L4	*SSD	5260, Dual Operational Amplifier			945450H	
ML16	M4	*SSD	4066, Quad Bilateral Switch			945043V	
ML17	N4		324, Quad Operational Amplifier			945026G	
ML18	S4	*SSD	4508, Dual 4-Bit Latch			945046K	

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Integrated Circuits		CAUTION: *SSD - STATIC SENSITIVE DEVICES					
ML19	V4	*SSD	4508, Dual 4-Bit Latch			945046K	
ML20	W4	*SSD	4508, Dual 4-Bit Latch			945046K	
ML21	X4	*SSD	4067, 16-Channel Multiplexer			945044M	
ML22	J0	*SSD	5260, Dual Operational Amplifier			945450H	
ML23	K2	*SSD	4066, Quad Bilateral Switch			945043V	
ML24	M2		1458, Dual Operational Amplifier			945022K	
ML25	L0		339, Quad Voltage Comparator			945023R	
ML26	N1	*SSD	4013, Dual D-Type Flip-Flop			943991L	
ML27	P2	*SSD	74HC244, Octal Line Driver			943987I	
ML28	R3	*SSD	40109, Quad Level Shifter			945045D	
ML29	S3	*SSD	40109, Quad Level Shifter			945045D	
ML30	V3	*SSD	74HC85, 4-Bit Magnitude Comparator			943978S	
ML31	V1		339, Quad Voltage Comparator			945023R	
ML32	W3	*SSD	4028, BCD to Decimal Decoder			943992C	
ML33	W1	*SSD	40109, Quad Level Shifter			945045D	
ML34	X3	*SSD	74HC00, Quad 2-Input NAND Gate			943968V	
ML35	X1	*SSD	74HC00, Quad 2-Input NAND Gate			943968V	
ML36	Z3		1458, Dual Operational Amplifier			945022K	
Connectors							
PL1			Plug, 64-Way			940339G	
PL5			Plug, 15-Way			945165Q	
Miscellaneous							
W1			Cable Assembly			BA87136	
W2			Cable Assembly			BA87136	
W3			Cable Assembly			BA87136	
W4			Cable Assembly			BA87136	
TP1			Terminal Assembly			936148X	
to			(test points)				
TP26							
LK1			Comprising:				
to			Plug, 4-Way			945062S	
LK4			Shorting Link			943684I	

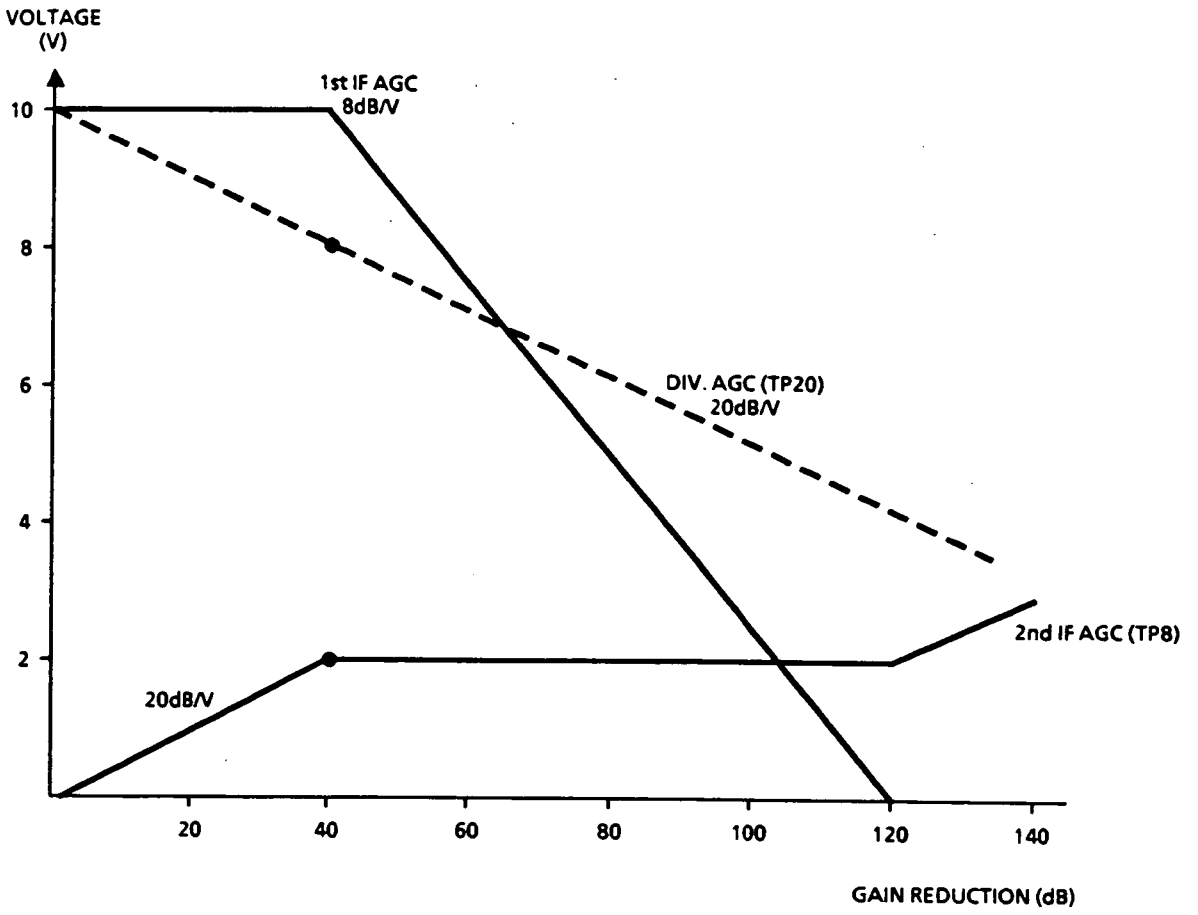
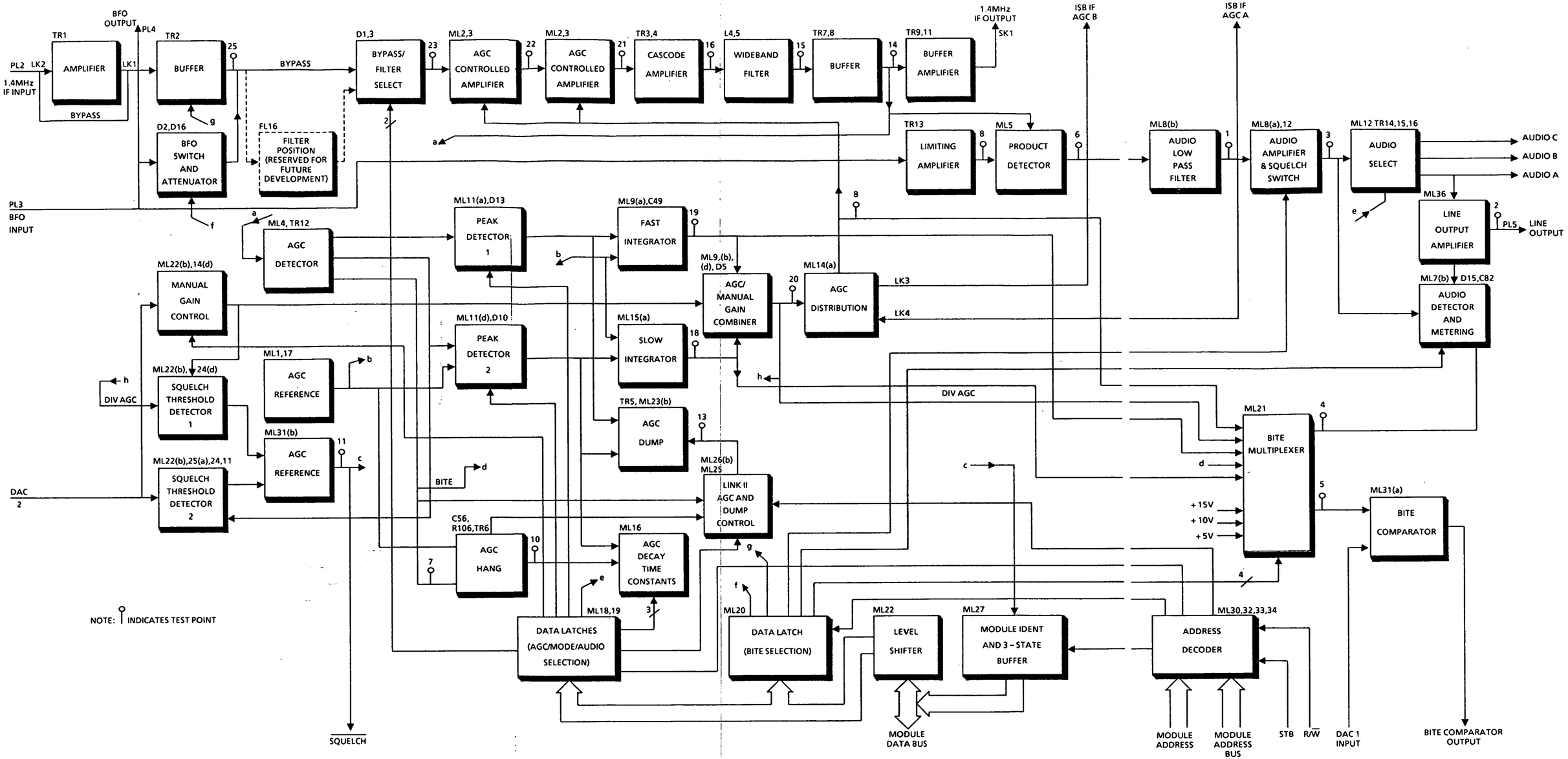


Fig. 19.2 AGC Distribution



ISB Module: Block Diagram **Fig.19.4**

CHAPTER 20

100 kHz IF MODULE

CONTENTS

ILLUSTRATIONS

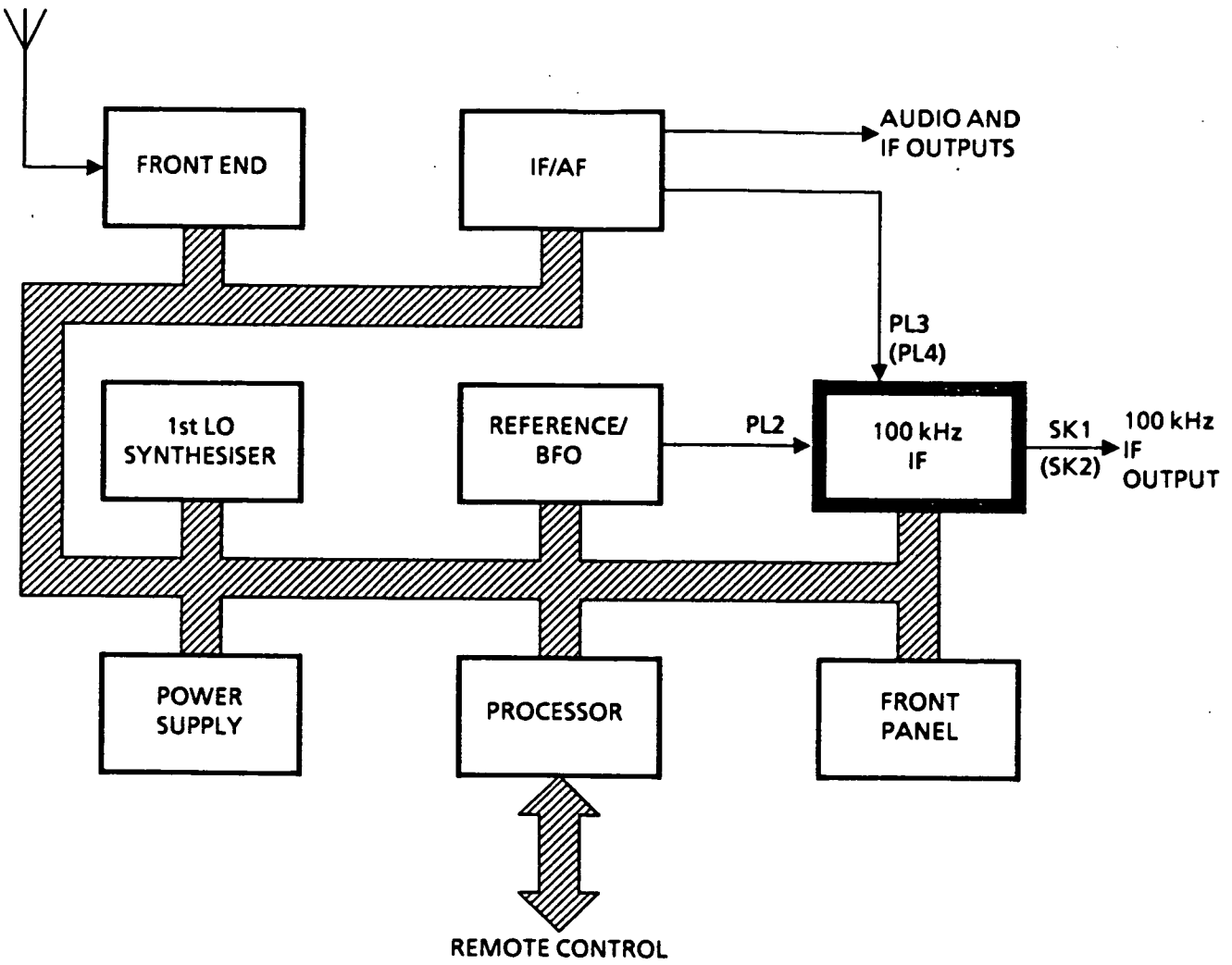


Fig. 20.1 Receiver Block Diagram

CHAPTER 20

100 kHz IF MODULE

INTRODUCTION

1 The 100 kHz IF Module accepts an IF input of 1.4 MHz from either an IF/AF or ISB Module and mixes it with the 5 MHz reference from the Reference/BFO Module to produce an IF output of 100 kHz. Two channels are provided for operation in dual or ISB receivers.

Fig. 20.1 Receiver Block Diagram

MODULE DESCRIPTION

2 The following description should be read in conjunction with the 100 kHz IF Module Block and Circuit Diagrams included in this chapter. Component references shown on the Block Diagram allow it to be related to the Circuit Diagram.

Reference Buffer

3 The 5 MHz reference signal is taken from the Reference/BFO Module and passed through a 5 MHz REFERENCE BUFFER/LEVEL SHIFTER to provide a buffered signal which is shifted to 15 V CMOS levels for the following circuits. The output level is monitored for BITE purposes.

Reference Divider

4 A DIVIDE-BY-10 stage divides the 5 MHz reference signal to produce a 500 kHz square wave of 12 V peak-to-peak.

Band Pass Filter

5 The third harmonic of the 500 kHz square wave is selected by a 3RD HARMONIC FILTER formed by two crystals and associated components. This produces the 1.5 MHz LO signal required by the mixer to convert the 1.4 MHz IF to a frequency of 100 kHz.

LO Drive Circuits

6 The 1.5 MHz LO signal is amplified by a pair of MIXER LO DRIVE AMPLIFIERS to the level required to drive the carrier port of the MIXERS directly.

Mixer Stages

7 The 1.4 MHz IF inputs are fed directly to the MIXER stages for mixing with the 1.5 MHz LO inputs to produce the output frequency of 100 kHz.

Low Pass Filters

8 Unwanted products resulting from the mixing are removed from the 100 kHz signals by a LOW PASS FILTER with a cut off frequency of 150 kHz.

Output Stages

9 Impedance matching between the LOW PASS FILTERS and the 50 ohm 100 kHz IF output sockets (SK1 and SK2) on the rear panel is performed by 100 kHz OUTPUT AMPLIFIER stages. In these two-stage amplifiers a common emitter stage is directly coupled to an emitter follower stage which has an output impedance of 50 ohms.

Bus Interface

10 A unique hardwired code is received on the Module Address input to the 100 kHz IF Module. This code is used by the ADDRESS DECODER to detect addresses on the Module Address Bus from the Processor Module and then produce read or write pulses according to the status of the R/W input. These pulses allow the Processor to read data from the 3-STATE BUFFER or write data to the DATA LATCH. Pulses on the strobe input ensure correct timing of write pulses. The 3-STATE BUFFER gives the Processor access to the 100 kHz IF Module identification code. The outputs of the DATA LATCH are used to control the BITE MULTIPLEXERS and select the BITE signal source.

BITE Measurement System

11 The BITE measurement system comprises two BITE MULTIPLEXERS, a BITE AMPLIFIER connected to a PEAK DETECTOR, and a BITE COMPARATOR. This system allows the Processor Module to measure various voltages and operating levels in the 100 kHz IF Module.

12 BITE MULTIPLEXER A allows a single BITE AMPLIFIER to boost the monitored levels of the 1.4 MHz and 100 kHz signals. A PEAK DETECTOR formed by D1, D2 and C55 doubles the amplified output level to produce the required DC level for BITE MULTIPLEXER B.

13 The voltage to be measured is selected by BITE MULTIPLEXER B and compared in the BITE COMPARATOR with a voltage generated by a digital to analogue converter (DAC) in the Processor Module. The Processor measures the level of the selected voltage by applying voltages representing upper and lower limits to the BITE COMPARATOR and then monitoring the resulting output.

FAULT FINDING

General

14 Fault finding techniques and recommended test equipment are described in Chapter 2. Diagnostic information specific to the 100 kHz IF Module is contained in the following sections.

BITE Tests

15 The following BITE tests for the 100 kHz IF Module are arranged in the order in which they are performed or presented for selection.

TEST NUMBER	:	401
TITLE	:	BITE hardware
PERFORMED	:	Continuous, unit confidence test, select test
DESCRIPTION	:	DAC 1 line is set to 2.55 volts (i.e. max). BITE multiplexer input X1 (+5 volts) is selected and the output of the BITE comparator is checked to ensure that it is low.
LIMITS	:	Less than 0.5 V at TP4.
FAULT DIRECTORY	:	Fault No. 2

TEST NUMBER : 402, 403

TITLE : + 5V rail, +15V rail

PERFORMED : Continuous, unit confidence test, select test.

DESCRIPTION : The appropriate BITE multiplexer input is selected and the supply voltage is checked.

LIMITS :

Test No.	Supply	Mux. Input	Mux. Limits (TP4)	
			Lower	Upper
402 403	+ 5 V +15 V	X2 X3	1.78 V 1.70 V	2.22 V 2.21 V

FAULT DIRECTORY : Fault No. 4

TEST NUMBER : 404, 405

TITLE : 1.4 MHz A, 1.4 MHz B

PERFORMED : Unit confidence test, select test

DESCRIPTION : The receiver is tuned to 0 MHz to provide a test signal. BITE multiplexer A input X0 (X1) is selected to allow the 1.4 MHz A (B) input to be amplified and detected. BITE multiplexer B input X8 (X9) is selected to measure the peak output.

LIMITS : Greater than 0.4 V at TP7.

FAULT DIRECTORY : Fault No. 2

TEST NUMBER : 406, 407

TITLE : 100 kHz A, 100 kHz B

PERFORMED : Unit confidence test, select test

DESCRIPTION : The receiver is tuned to 0 MHz to provide a test signal. BITE multiplexer input X2 (X3) is selected to allow the 100 kHz IF output to be amplified and detected. BITE multiplexer B input X10 (X11) is selected to measure the peak output.

LIMITS : Greater than 1.4 V at TP7.

FAULT DIRECTORY : Fault No. 6

TEST NUMBER	:	408
TITLE	:	5 MHz level
PERFORMED	:	Continuous, unit confidence test, select test
DESCRIPTION	:	BITE multiplexer B input X7 is selected to measure the 5 MHz level from the Reference/BFO Module.
LIMITS	:	Greater than 1.5 V at TP4.
FAULT DIRECTORY	:	Fault No. 5

Fault Directory

16 Use the following fault directory to identify the fault condition and take the necessary corrective action. Note that all inputs to the module are assumed to be correct.

Fault No.	Fault Symptom	Possible Causes	Suggestion Action
1	Fails to run BITE tests for 100 kHz IF Module.	Address decoding/module ident. not responding.	Check address decoding/module ident logic operation using signature analysis routine if necessary.
2	BITE hardware fault.	(a) Comparator/multiplexer A or B inoperative.	(a) Use BITE test 401 to check comparator operation. Select all BITE tests for this module to check multiplexer operation for all analogue inputs. Use signature analysis routine to check multiplexer addressing.
		(b) BITE amplifier or peak detector faulty.	(b) Select appropriate BITE tests to check output on TP7.
3	BITE indicates failure but manual check shows no fault.	BITE hardware fault.	As above.
4	Power supply fault within module.	Faulty component drawing excess current. or open circuit choke L1 or L2.	Locate and replace faulty component.
5	No 100 kHz output on channel A and B.	Mixer LO drive level low.	Follow mixer LO drive check procedure.
6	No 100 kHz output on one channel only.	(a) Mixer faulty.	(a) Check both inputs and supplies to mixer IC before replacing.
		(b) Low pass filter or 100 kHz output amplifier faulty.	(b) Follow 100 kHz output check procedure.

SIGNATURE ANALYSIS ROUTINE

23 This routine checks that the module control signals are interfaced and decoded correctly from the module bus.

Processor module DIL switch settings: SW1,4,7 OFF
SW2,3,5,6,8 ON

Signature analyser settings:

Start: 9A Extender assembly, negative trigger
Stop: 9A Extender assembly, negative trigger
Clock: 8A Extender assembly, positive trigger
Earth: 1A Extender assembly

Note: Signatures xxxxF signify a flashing probe indicator.

Signal	Signature	Test Node				Remarks
+5v	HA90					
OV	0000					
		DATA BUS INTERFACES				
M-D0	503F	PL1/7A	ML6/18	ML5/3		Module bus
M-D1	7214	PL1/7B	ML6/16	ML5/4		Module bus
M-D2	P300	PL1/6A	ML6/14	ML5/7		Module bus
M-D3	1PUA	PL1/6B	ML6/12	ML5/8		Module bus
M-D4	UACU	PL1/5A	ML6/9			Module bus
		ADDRESS DECODER				
M-A4	0000	PL1/10A	R77	ML9/10		Module address
M-A5	0001	PL1/10B	R76	ML9/12		Module address
M-A6	0001	PL1/9A	R74	ML9/13		Module address
M-A7	H9A0	PL1/9B	R73	ML9/15		Module address
MOD0	0000	PL1/14A	R82	ML9/9		Module address
MOD1	0000	PL1/14B	R81	ML9/11		Module address
MOD2	0000	PL1/13A	R80	ML9/14		Module address
MOD3	H9A0	PL1/13B	R79	ML9/1		Module address
M-R/W	3571	PL1/8B	ML7/13			Module bus
M-STB	0000F	PL1/8A	ML7/5			Module bus
A=B	H9A1	ML9/6	ML7/1	ML7/2	ML7/4	Addr. decoder
TP6	PFH0	ML7/12	ML7/3	ML6/1	ML6/19	Addr. decoder
ML7/6	H9A0	ML7/6	ML5/11			Addr. decoder
ML9/2	H9A0	ML9/2				A<B ML9
ML9/3	H9A0	ML9/3				A=B ML9
ML9/4	H9A0	ML9/4				A>B ML9

SIGNATURE ANALYSIS ROUTINE (continued)

Signal	Signature	Test Node			Remarks
		DATA LATCH (BITE Selection) ML5			
CLR	H9A0	ML5/1			
ML5/2	1H6P	ML5/2	ML8/10	ML4/10	CONTROL A
ML5/5	8F7A	ML5/5	ML8/11	ML4/11	CONTROL B
ML5/6	44U0	ML5/6	ML4/14		CONTROL C
ML5/9	A0C5	ML5/9	ML4/13		CONTROL D
ML8/13	0000	ML8/13			
ML8/14	0000	ML8/14			
		MODULE IDENT ML6			
YA1	H9A0	ML6/2			ID
YA2	H9A0	ML6/4			ID
YA3	HA90	ML6/6			ID
YA4	0000	ML6/8			ID
YB1	0000	ML6/11			ID

Mixer LO Drive Check Procedure

17 Ensure PL2 is connected to the 5 MHz reference output of the Reference/BFO Module. Connect the RF millivoltmeter to PL5 to verify the level is greater than -13 dBm.

18 Use the frequency counter to check the following test points for the correct frequency output from each stage in the LO drive signal path. Refer to the circuit diagram for signal levels.

TP12 - 5 MHz
TP17 - 500 kHz
TP15 - 1.5 MHz

100 kHz Output Check Procedure

19 Inject a 1.4 MHz test signal of -7 dBm at PL3 (PL4). Using the oscilloscope, check the waveform on the following test points. Refer to the circuit diagram for signal levels.

TP13 (14) - 100 kHz (plus ripple)
TP9 (10) - 100 kHz (smoothed)
SK1 (SK2) - 100 kHz

20 Connect the RF millivoltmeter, set to 50 ohms input impedance, to SK1 (SK2) and check that the output is -7 dBm.

PARTS LIST

21 The Racal part number for a complete 100 kHz IF Module is ST86492.

22 Information on the identification and handling of SMDs is provided in Chapter 2. The parts list for the 100 kHz IF Module is as follows:

Cct. Ref.	Grid Ref.	Value	Description	Rat.	Tol %	Racal Part Number	ID Code
Resistors				W			
R1		33k	Thick Film Network		2	934507U	
R2		33k	Thick Film Network		2	934507U	
R3	B8	10R	Thick Film Chip	0.125	2	943865X	100
R4	B8	10k	Thick Film Chip	0.125	2	943902F	103
R5	B7	10k	Thick Film Chip	0.125	2	943902F	103
R6	B2	10R	Thick Film Chip	0.125	2	943865X	100
R7	B2	10k	Thick Film Chip	0.125	2	943902F	103
R8	B1	10k	Thick Film Chip	0.125	2	943902F	103
R9	B8	1k	Thick Film Chip	0.125	2	943890L	102
R10	B2	1k	Thick Film Chip	0.125	2	943890L	102
R11	B8	6k8	Thick Film Chip	0.125	2	943900H	682
R12	B7	1k5	Thick Film Chip	0.125	2	943892J	152
R13	B1	6k8	Thick Film Chip	0.125	2	943900H	682
R14	B1	1k5	Thick Film Chip	0.125	2	943892J	152
R15	C8	470R	Thick Film Chip	0.125	2	943886I	471
R16	C2	470R	Thick Film Chip	0.125	2	943886I	471
R17	C7	3k3	Thick Film Chip	0.125	2	943896P	332
R18	C1	3k3	Thick Film Chip	0.125	2	943896P	332
R19	C6	2k7	Thick Film Chip	0.125	2	943895Y	272
R20	C8	10R	Thick Film Chip	0.125	2	943865X	100
R21	D2	10R	Thick Film Chip	0.125	2	943865X	100
R22	C0	47R	Thick Film Chip	0.125	2	943873W	470
R23	D6	47R	Thick Film Chip	0.125	2	943873W	470
R24	D2	4k7	Thick Film Chip	0.125	2	943898N	472
R25	D1	1k	Thick Film Chip	0.125	2	943890L	102
R26	D9	4k7	Thick Film Chip	0.125	2	943898N	472
R27	D7	1k	Thick Film Chip	0.125	2	943890L	102
R28	D4	10k	Thick Film Chip	0.125	2	943902F	103
R29	D5	10R	Thick Film Chip	0.125	2	943865X	100
R30	D5	1k	Thick Film Chip	0.125	2	943890L	102
R31	D1	3k3	Thick Film Chip	0.125	2	943896P	332
R32	D7	3k3	Thick Film Chip	0.125	2	943896P	332
R33	D5	47k	Thick Film Chip	0.125	2	943910E	473
R34	D2	4k7	Thick Film Chip	0.125	2	943898N	472
R35	D9	4k7	Thick Film Chip	0.125	2	943898N	472
R36	D7	3k3	Thick Film Chip	0.125	2	943896P	332
R37	D1	3k3	Thick Film Chip	0.125	2	943896P	332
R38	E4	1k	Thick Film Chip	0.125	2	943890L	102
R39	E5	10R	Thick Film Chip	0.125	2	943865X	100
R40	E5	820R	Thick Film Chip	0.125	2	943889X	821
R41	F1	10k	Thick Film Chip	0.125	2	943902F	103
R42	F1	3k3	Thick Film Chip	0.125	2	943896P	332
R43	F1	27k	Thick Film Chip	0.125	2	943907S	273
R44	F5	10k	Thick Film Chip	0.125	2	943902F	103
R45	F4	1k	Thick Film Chip	0.125	2	943890L	102
R46	F8	10k	Thick Film Chip	0.125	2	943902F	103
R47	F7	3k3	Thick Film Chip	0.125	2	943896P	332
R48	F4	6k8	Thick Film Chip	0.125	2	943900H	682
R49	F9	27k	Thick Film Chip	0.125	2	943907S	273
R50	F2	4k7	Thick Film Chip	0.125	2	943898N	472
R51	G0	820R	Thick Film Chip	0.125	2	943889X	821
R52	G7	820R	Thick Film Chip	0.125	2	943889X	821
R53	G5	10k	Thick Film Chip	0.125	2	943902F	103
R54	G4	10k	Thick Film Chip	0.125	2	943902F	103
R55	G1	10R	Thick Film Chip	0.125	2	943865X	100
R56	G9	4k7	Thick Film Chip	0.125	2	943898N	472

Outline missing

Resistors

				W			
R57	G0	39R	Thick Film Chip	0.125	2	943872F	390
R58	G4	10k	Thick Film Chip	0.125	2	943902F	103
R59	G7	39R	Thick Film Chip	0.125	2	943872F	390
R60	H8	10R	Thick Film Chip	0.125	2	943865X	100
R61	N2	120k	Thick Film Chip	0.125	2	943915R	124
R62	N2	18k	Thick Film Chip	0.125	2	943905K	183
R63	N0	10k	Thick Film Chip	0.125	2	943902F	103
R64	N0	10k	Thick Film Chip	0.125	2	943902F	103
R65	P0	10k	Thick Film Chip	0.125	2	943902F	103
R66	P0	15k	Thick Film Chip	0.125	2	943904D	153
R67	P0	10k	Thick Film Chip	0.125	2	943902F	103
R68	R5	68k	Thick Film Chip	0.125	2	943912C	683
R69	R5	820R	Thick Film Chip	0.125	2	943889X	821
R70	R5	100k	Thick Film Chip	0.125	2	943914A	104
R71	R5	10k	Thick Film Chip	0.125	2	943902F	103
R72	S5	100R	Thick Film Chip	0.125	2	943878J	101
R73	T2	22k	Thick Film Chip	0.125	2	943906B	223
R74	T2	22k	Thick Film Chip	0.125	2	943906B	223
R75	T3	100k	Thick Film Chip	0.125	2	943914A	104
R76	T2	22k	Thick Film Chip	0.125	2	943906B	223
R77	T2	22k	Thick Film Chip	0.125	2	943906B	223
R78	V3	1k	Thick Film Chip	0.125	2	943890L	102
R79	V2	22k	Thick Film Chip	0.125	2	943906B	223
R80	V2	22k	Thick Film Chip	0.125	2	943906B	223
R81	V2	22k	Thick Film Chip	0.125	2	943906B	223
R82	V1	22k	Thick Film Chip	0.125	2	943906B	223
R83	W4	100k	Thick Film Chip	0.125	2	943914A	104
R84	W5	100k	Thick Film Chip	0.125	2	943914A	104
R85	W3	100k	Thick Film Chip	0.125	2	943914A	104
R86	W3	100k	Thick Film Chip	0.125	2	943914A	104
R87	X3	100k	Thick Film Chip	0.125	2	943914A	104
R88	X4	100k	Thick Film Chip	0.125	2	943914A	104
R89	X3	100k	Thick Film Chip	0.125	2	943914A	104

Capacitors

				V		
C1	B5	47p	Ceramic Chip	50	5	941795H
C2	B4	47p	Ceramic Chip	50	5	941795H
C3	B4	68p	Ceramic Chip	50	5	941797F
C4	B8	1µ	Tantalum Chip	35	20	945049Z
C5	B8	47n	Ceramic Chip	50	10	945145M
C6	B2	1µ	Tantalum Chip	35	20	945049Z
C7	B2	47n	Ceramic Chip	50	10	945145M
C8	B4	10n	Ceramic Chip	50	10	941775D
C9	B9	10µ	Tantalum Chip	35	10	945053C
C10	C2	10µ	Tantalum Chip	35	10	945053C
C11	C0	100n	Ceramic Chip	50	20	945146T
C12	C2	100n	Ceramic Chip	50	20	945146T
C13	C7	47n	Ceramic Chip	50	10	945145M
C14	C1	47n	Ceramic Chip	50	10	945145M
C15	C7	100n	Ceramic Chip	50	20	945146T
C16	C9	100n	Ceramic Chip	50	20	945146T
C17	D0	10n	Ceramic Chip	50	10	941775D
C18	D4	10n	Ceramic Chip	50	10	941775D
C19	D5	10n	Ceramic Chip	50	10	941775D

Outline Missing

Capacitors

				V		
C20	D1	10n	Ceramic Chip	50	10	941775D
C21	D7	10n	Ceramic Chip	50	10	941775D
C22	D6	10n	Ceramic Chip	50	10	941775D
C23	E4	10n	Ceramic Chip	50	10	941775D
C24	E5	1µ	Tantalum Chip	35	20	945049Z
C25	E1	100n	Ceramic Chip	50	20	945146T
C26	E1	150p	Ceramic Chip	50	5	941801X
C27	E7	100n	Ceramic Chip	50	20	945146T
C28	E1	470p	Ceramic Chip	50	5	941807B
C29	E7	150p	Ceramic Chip	50	5	941801X
C30		100n	Ceramic Chip	50	20	945146T
C31	E1	150p	Ceramic Chip	50	5	941801X
C32	F8	470p	Ceramic Chip	50	5	941807B
C33	F4	10n	Ceramic Chip	50	10	941775D
C34	F8	100n	Ceramic Chip	50	20	945146T
C35	F8	150p	Ceramic Chip	50	5	941801X
C36	F2	10µ	Tantalum Chip	35	10	945053C
C37	F5	10n	Ceramic Chip	50	10	941775D
C38	F4	10n	Ceramic Chip	50	10	941775D
C39	F5	1µ	Tantalum Chip	35	20	945049Z
C40	G8	10µ	Tantalum Chip	35	10	945053C
C41	G2	100n	Ceramic Chip	50	20	945146T
C42	G0	1µ	Tantalum Chip	35	20	945049Z
C43	G7	1µ	Tantalum Chip	35	20	945049Z
C44	G5	10n	Ceramic Chip	50	10	941775D
C45	G9	100n	Ceramic Chip	50	20	945146T
C46	P0	10n	Ceramic Chip	50	10	941775D
C47	P4	10n	Ceramic Chip	50	10	941775D
C48	R2	10n	Ceramic Chip	50	10	941775D
C49	R5	10n	Ceramic Chip	50	10	941775D
C50	R2	10n	Ceramic Chip	50	10	941775D
C51	T5	100n	Ceramic Chip	50	20	945146T
C52	S3	100n	Ceramic Chip	50	20	945146T
C53	T4	100n	Ceramic Chip	50	20	945146T
C54	T3	10n	Ceramic Chip	50	10	941775D
C55	V3	10n	Ceramic Chip	50	10	941775D
C56	V5	100n	Ceramic Chip	50	20	945146T
C57	W3	10n	Ceramic Chip	50	10	941775D
C58	W3	1µ	Tantalum Chip	35	20	945049Z
C59	X3	1µ	Tantalum Chip	35	20	945049Z
C60	X4	10µ	Tantalum Chip	35	10	945053C
C61	X3	100n	Ceramic Chip	50	20	945146T
C62	Y3	10µ	Tantalum Chip	35	10	945053C
C63	Y4	10n	Ceramic Chip	50	10	941775D
C64		100n	Ceramic Chip	50	20	945146T
C65	Y1	100n	Ceramic Chip	50	20	945146T
C66	Y0	100n	Ceramic Chip	50	20	945146T

Inductors

			W		
L1	100µH	Choke	0.2	10	939161P
L2	100µH	Choke	0.2	10	939161P
L3	10mH	Choke	0.213	5	926285Y
L4	10mH	Choke	0.213	5	926285Y
L5	10mH	Choke	0.213	5	926285Y
L6	10mH	Choke	0.213	5	926285Y

Outline missing

Diodes

D1	V4	BAS 16	943951D
D2	W5	BAS 16	943951D

Transistors

TR1	B7	BC 849, NPN	943941W
TR2	B1	BC 849, NPN	943941W
TR3	D4	MMBT2369, NPN	943946J
TR4	F4	MMBT2369, NPN	943946J
TR5	F1	BC 849, NPN	943941W
TR6	F8	BC 849, NPN	943941W
TR7	G1	BC 849, NPN	943941W
TR8	G5	MMBT2369, NPN	943946J
TR9	G7	BC 849, NPN	943941W
TR10	S4	BC 849, NPN	943941W

Integrated Circuits CAUTION: *SSD - STATIC SENSITIVE DEVICES

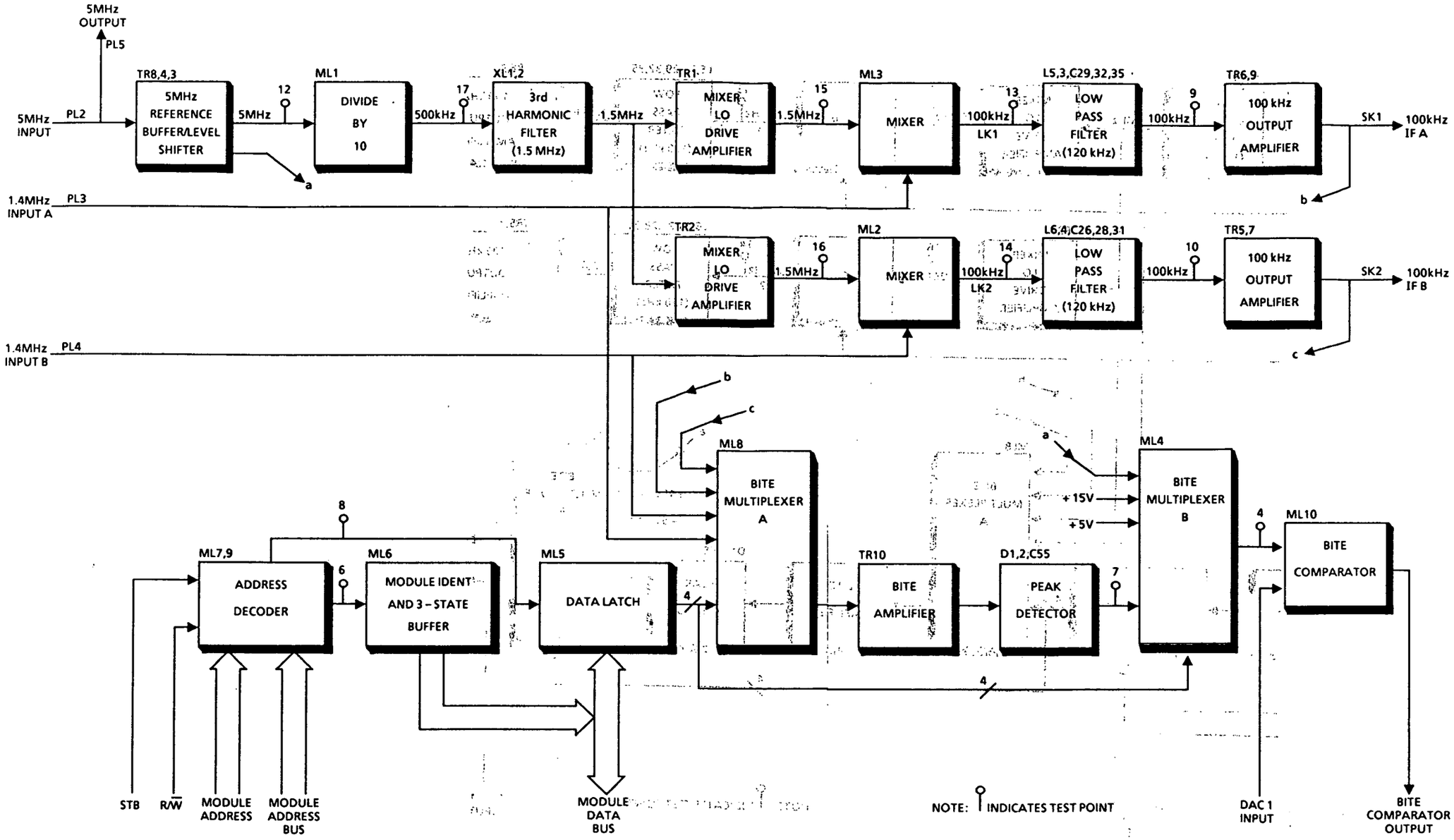
ML1	C4	*SSD	4017, Decade Counter	945419I
ML2	D1		1496, Balanced Modulator/Demodulator	945027X
ML3	D8		1496, Balanced Modulator/Demodulator	945027X
ML4	P2	*SSD	4067, 16-Channel Multiplexer	945044M
ML5	R4	*SSD	74HC273, D-Type Flip-Flop	943989G
ML6	S2	*SSD	74HC244, Octal Line Driver	943987I
ML7	T3	*SSD	74HCT10, Triple 3-Input NAND Gate	943973F
ML8	T4	*SSD	4067, 16-Channel Multiplexer/Demultiplexer	945044M
ML9	V3	*SSD	74HC85, 4-Bit Magnitude Comparator	943978S
ML10	X1		339, Quad Voltage Comparator	945023R

Connectors

PL1	Plug, 64-Way	940339G

Miscellaneous

XL1	Crystal, Quartz 1499.9 kHz	AD88156
XL2	Crystal, Quartz 1499.9 kHz	AD88156
W1	Cable Assembly	BA87136
W2	Cable Assembly	BA87136
W3	Cable Assembly	BA87136
W4	Cable Assembly	BA87135
W5	Cable Assembly	BA87135
W6	Cable Assembly	BA87136
TP1 to TP17	Terminal Assembly (test points)	936148X
LK1	Comprising:	
LK2	Plug, 4-Way	945062S
	Shorting Link	943684I



100 kHz IF Module: Block Diagram **Fig.20.2**

APPENDIX A

BANDWIDTH CONFIGURATION DATA

INTRODUCTION

This Appendix contains the bandwidth data which is stored in the receiver's non-volatile memory. The data may be programmed into the receiver using the front panel menu facility as described in Chapter 7. Alternatively, it may be input via the remote control port as described in Chapter 5.

CONFIGURATION DATA TABLES

The following tables list the bandwidth configuration data for the different filter options supplied with the IF/AF Module and the IF Filter Module. See Chapter 7 for an explanation of the parameters. This data is programmed into the receiver when it is supplied but in some circumstances it may need to be changed by the user. Examples of these circumstances are:

(1) If receivers with different filter options are to be used together in a remotely controlled system, it may be necessary to change the Bandwidth Numbers for some filters to ensure that all receivers are compatible.

(2) The user wishes to configure the receiver with additional offset filter bandwidths.

(3) An extra crystal filter is added by the user.

(4) The Processor Module in a receiver is changed.

In the following tables all frequencies are in Hz. "USB" and "LSB" refer to the signal frequency. The sidebands are reversed at the 1.4 MHz IF.

TABLE A-1

Filter Configuration Data for IF/AF Module

Option Code	Filter BD No.	BW Type	Front Panel Display	BW No.	Filter Position	Lower Passband Freq.	Upper Passband Freq.	Offset Freq.
LA	86658	USB	2.7kHz	00	04	300	3000	0
	86659	LSB	2.7kHz	00	05	-3000	-300	0
	86662	SYM	0.3kHz	00	03	-150	150	0
	86661	SYM	1.0kHz	01	02	-500	500	0
	86658	SYM	2.7kHz	02	04	-1350	1350	-1650
	86660	SYM	6.0kHz	03	01	-3000	3000	0
	bypass	SYM	12.0kHz	04	06	-6000	6000	0
LB	86658	USB	2.7kHz	00	04	300	3000	0
	86659	LSB	2.7kHz	00	05	-3000	-300	0
LC	86658	USB	2.7kHz	00	04	300	3000	0
	86657	USB	3.2kHz	01	05	200	3400	1800
	86658	LSB	2.7kHz	00	04	-3000	-300	-3300
	86657	LSB	3.2kHz	01	05	-3400	-200	-1800
	86662	SYM	0.3kHz	00	03	-150	150	0
	86661	SYM	1.0kHz	01	02	-500	500	0
	86658	SYM	2.7kHz	02	04	-1350	1350	-1650
	86657	SYM	3.2kHz	05	05	-1600	1600	0
	86660	SYM	6.0kHz	03	01	-3000	3000	0
	bypass	SYM	12.0kHz	04	06	-6000	6000	0
LD	86657	USB	3.2kHz	00	02	200	3400	1800
	86657	LSB	3.2kHz	00	02	-3400	-200	-1800
	86657	SYM	3.2kHz	05	02	-1600	1600	0
	86660	SYM	6.0kHz	03	01	-3000	3000	0

TABLE A-2

Filter Configuration Data for IF Filter Module

Option Code	Rx No.	Filter BD No.	BW Type	Front Panel Display	BW No.	Filter Position	Lower Passband Freq.	Upper Passband Freq.	Offset Freq.
MB	-	87989	SYM	0.15kHz	06	07	-70	80	0
MC	-	87989	SYM	0.15kHz	06	07	-70	80	0
	-	88005	SYM	8.0kHz	07	08	-4000	4000	0
MD	1	87989	SYM	0.15kHz	06	07	-70	80	0
	1	88005	SYM	8.0kHz	07	08	-4000	4000	0
	2	87989	SYM	0.15kHz	06	10	-70	80	0
	2	88005	SYM	8.0kHz	07	11	-4000	4000	0
ME	1	87959	SYM	3.0kHz	06	7	-1500	1500	0
	2	87959	SYM	3.0kHz	06	10	-1500	1500	0
MF	-	87962	SYM	6.0kHz	06	07	-3000	3000	0
	-	87961	SYM	5.0kHz	07	08	-2500	2500	0
	-	87960	SYM	4.0kHz	08	09	-2000	2000	0
	-	87959	SYM	3.0kHz	09	10	-1500	1500	0
MG	-	87989	SYM	0.15kHz	06	07	-70	80	0
	-	87959	SYM	3.0kHz	07	08	-1500	1500	0
MH	1	87989	SYM	0.15kHz	06	07	-70	80	0
	1	88457	SYM	0.3kHz	07	08	-150	150	0
	1	88458	SYM	1.0kHz	08	09	-500	500	0
	2	87989	SYM	0.15kHz	06	10	-70	80	0
	2	88457	SYM	0.3kHz	07	11	-150	150	0
	2	88458	SYM	1.0kHz	08	12	-500	500	0

Note: In options where Rx No. is indicated as "-" the module is intended for use in single receivers.

APPENDIX B

SECURITY CODE

In order to prevent unauthorised changes to configuration data stored in the receiver's non-volatile memory (e.g. bandwidth and remote control port data) entry of a security code is required.

The security code is 7926.