ISO²-CMOS MT8870
Integrated DTMF Receiver

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Features

- Complete DTMF receiver
- Low power consumption
- Internal gain setting amplifer
- Adjustable guard time
- Central Office Quality

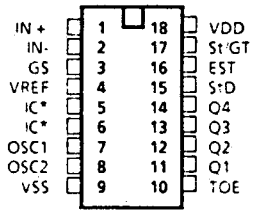
Applications

- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote Control
- Personal Computers

Description

The MT8870 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in Mitel's double poly ISO²-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface.

Pin Connections



*Connect to VSS

Ordering Information

MT8870BE 18 PIN PLASTIC
MT8870BC 18 PIN CERDIP

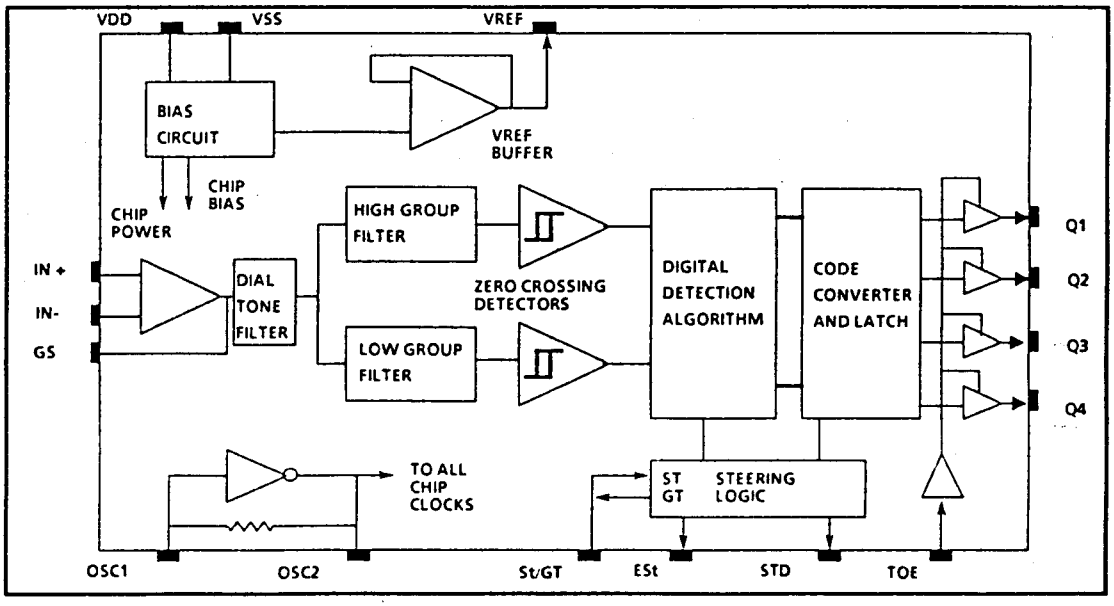


Figure 1. Functional Block Diagram

Absolute Maximum Ratings†

	Parameter	Symbol	Min	Max	Units
1	Power supply voltage V_{DD}-V_{SS}			6	V
2	Voltage on any pin		V_{SS}-0.3	V_{DD} + 0.3	V
3	Current at any pin			10	mA
4	Operating temperature		-40	+ 85	°C
5	Storage temperature		-65	+ 150	°C
6	Package power dissipation			1000	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75 °C at 16 mW / °C All leads soldered to board.

DC Electrical Characteristics

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions†
1	SUPPLY	Operating supply voltage		4.75	5.0	5.25	V	
2		Operating supply current	I_{DD}		3.0	9.0	mA	
3		Power consumption	P_O		15	45	mW	f = 3.58MHz; V_{DD} = 5V
4	INPUTS	High level input	V_{iH}	3.5			V	
5		Low level input voltage	V_{iL}			1.5	V	
6		Input leakage current	I_{iH}/I_{IL}		0.1		μA	V_{IN} = V_{SS} or V_{DD}
7		Pull up (source) current	I_{SO}		7.5	15	μA	TOE (pin 10) = 0V
8		Input impedance (IN+, IN-)	R_{iN}		10		MΩ	@ 1 kHz
9		Steering threshold voltage	V_{T-}	2.2		2.5	V	
10	OUTPUTS	Low level output voltage	V_{OL}			0.03	V	No load
11		High level output voltage	V_{OH}	4.97			V	No load
12		Output low (sink) current	I_{OL}	1	2.5		mA	V_{OUT} = 0.4V
13		Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6V
14		V_{Ref} output voltage	V_{Ref}	2.4		2.8	V	No load
15		V_{Ref} output resistance	R_{OR}		10		KΩ	

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.
V_{DD} = 5V ± 5%, V_{SS} = 0V. Voltages are with respect to ground (V_{SS}) unless otherwise stated.

Operating Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Gain Setting Amplifier

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Input leakage current	I_{IN}		100		nA	$V_{SS} \leq V_{IN} \leq V_{DD}$
2	Input resistance	R_{IN}		10		MΩ	
3	Input offset voltage	V_{OS}		25		mV	
4	Power suply rejection	PSRR		60		dB	1 KHz
5	Common mode rejection	CMRR		60		dB	$-3.0V \leq V_{IN} \leq 3.0V$
6	DC open loop voltage gain	A_{VOL}		65		dB	
7	Open loop unity gain bandwidth	f_C		1.5		MHz	
8	Output voltage swing	V_O		4.5		V_{pp}	$R_L \geq 100K\Omega$ to V_{SS}
9	Maximum capacitive load (GS)	C_L		100		pF	
10	Maximum resistive load (GS)	R_L		50		KΩ	
11	Common mode range	V_{CM}		3.0		V_{pp}	No Load

† V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25°C

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ†	Max	Units	Notes
1	SIGNAL CONDITIONS	Valid input signal levels (each tone of composite signal)		-29			dBm	1,2,3,5,6,9
				27.5			mV_{RMS}	1,2,3,5,6,9
						+1	dBm	1,2,3,5,6,9
						883	mV_{RMS}	1,2,3,5,6,9
2		Positive twist accept			10		dB	2,3,6,9
3		Negative twist accept			10		dB	2,3,6,9
4		Freq. deviation accept		± 1.5% ± 2Hz			Nom.	2,3,5,9
5		Freq. deviation reject		± 3.5%			Nom.	2,3,5,9
6		Third tone tolerance			-16		dB	2,3,4,5,9,10
7		Noise tolerance			-12		dB	2,3,4,5,7,9,10
8		Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

† V_{DD} = 5 V, V_{SS} = 0, T_A = 25°C and f_C = 3.579545 MHz using test circuit shown in Figure 2

NOTES

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones
3. Tone duration = 40 ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies
5. Both tones in composite signal have an equal amplitude
6. Tone pair is deviated by ± 1.5% ± 2Hz
7. Bandwidth limited (3KHz) Gaussian noise
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2%
9. For an error rate of better than 1 in 10,000
10. Referenced to lowest level frequency component in DTMF signal
11. Referenced to the minimum valid accept level

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	TIMING	Tone present detect time	t_{DP}	5	11	14	ms	see Figure 3
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	see Figure 3
3		Tone duration accept	t_{REC}			40	ms	User adjustable
4		Tone duration reject	t_{REC}	20			ms	User adjustable
5		Interdigit pause accept	t_{ID}			40	ms	User adjustable
6		Interdigit pause reject	t_{DO}	20			ms	User adjustable
7	OUTPUTS	Propagation delay (St to Q)	t_{PQ}		8	11	μs	TOE = V_{DD}
8		Propagation delay (St to StD)	t_{PStD}		12		μs	TOE = V_{DD}
9		Output data set up (Q to StD)	t_{QStD}		3.4		μs	TOE = V_{DD}
10		Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	RL = 10KΩ CL = 50 pF
11		Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	RL = 10KΩ CL = 50 pF
26	CLOCK	Crystal /clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
27		Clock input rise time	t_{LHCL}			110	ns	Ext. clock
28		Clock input fall time	t_{HLCL}			110	ns	Ext. clock
29		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
30		Capacitive load (OSC2)	C_{LO}			30	pF	

†V_{DD} = 5V, V_{SS} = 0V T_A = 25°C and f_C = 3.579545 MHz, using test circuit in Figure 2

‡Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

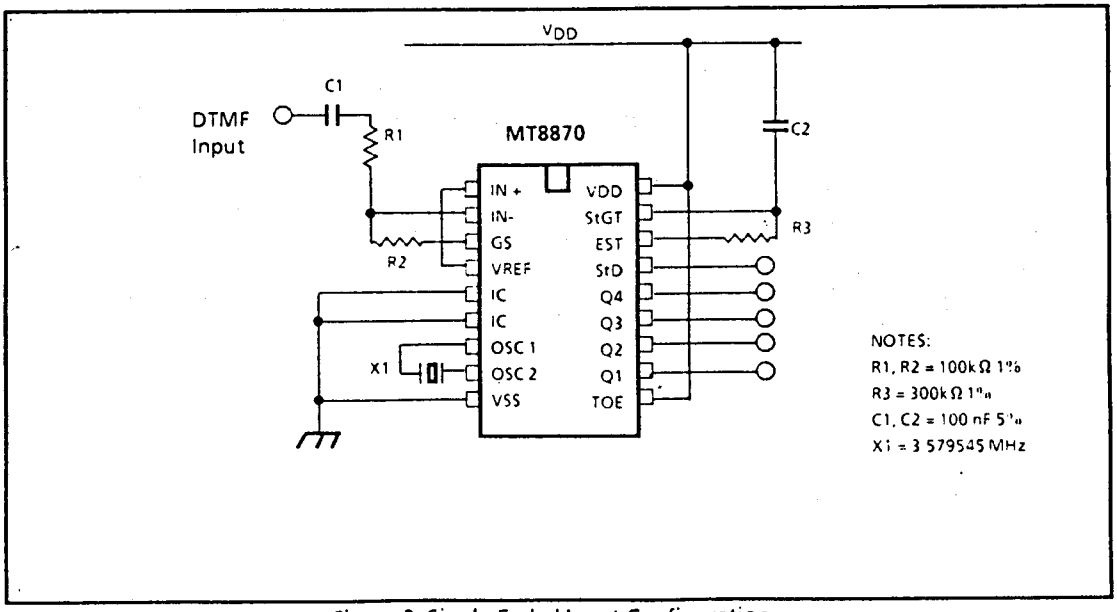
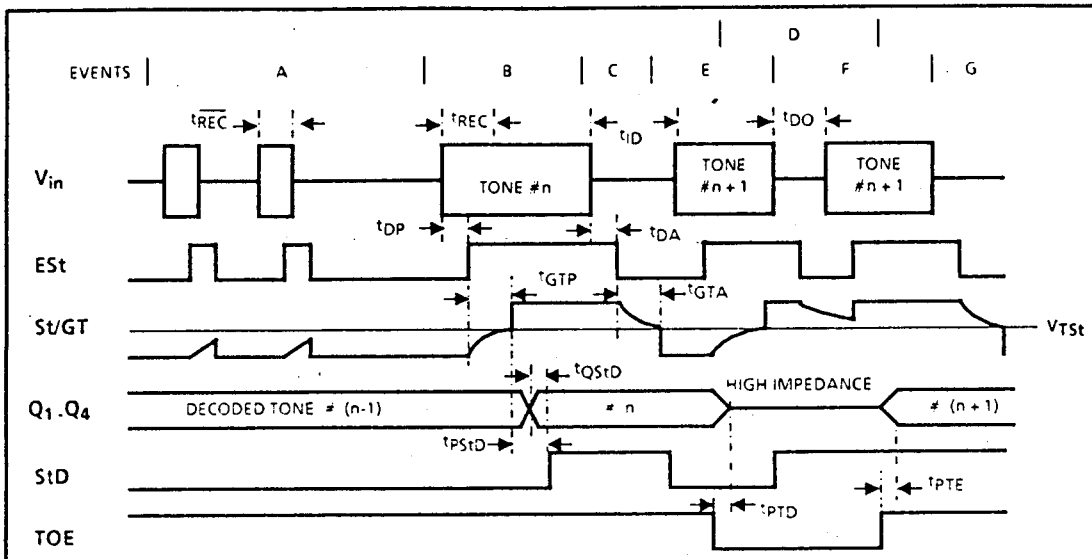


Figure 2. Single Ended Input Configuration

Pin Description

Pin #	Name	Description
1	IN +	Non-inverting op-amp input.
2	IN-	Inverting op-amp input.
3	GS	Gain select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	V_{REF}	Reference voltage output, nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig.2).
5	IC	Internal connection. Must be tied to V_{SS}.
6	IC	Internal connection. Must be tied to V_{SS}.
7	OSC1	Clock input.
8	OSC2	Clock output. A 3.5795 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit.
9	V_{SS}	Negative power supply input.
10	TOE	3- state output enable (input). Logic high enables the outputs Q1-Q4. Internal pull up.
11-14	Q1-Q4	3-state data outputs. When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Fig. 5).
15	StD	Delayed steering output.Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/Gt falls below V_{TSt}
16	ESt	Early steering output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
19	St/GT	Steering input/guard time output (bi-directional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	V_{DD}	Positive power supply input.



EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED
B) TONE ≠n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS
C) END OF TONE ≠n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE
D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE
E) TONE ≠n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE)
F) ACCEPTABLE DROPOUT OF TONE ≠n + 1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCED
G) END OF TONE ≠n + 1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DECTECTION OF VALID TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
Q_1-Q_4	4-BIT DECODED TONE OUTPUT
StD	DELAYED STEERING OUTPUT. INDICTES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSISTUTING A VALID SIGNAL.
TOE	TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS Q_1-Q_4 TO ITS HIGH IMPEDANCE STATE.
$t_{\overline{REC}}$	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID
t_{REC}	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID}	MINIMUM TIME BETWEEN VALID DTMF SIGNALS
t_{DO}	MAXIMUM ALLOWABLE DROP OUT DURING VALID DTMF SIGNAL
t_{DP}	TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS
t_{DA}	TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS
t_{GTP}	GUARD TIME, TONE PRESENT
t_{GTA}	GUARD TIME, TONE ABSENT

Figure 3. Timing Diagram

Functional Description

The MT8870 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which seperates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Seperation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor band pass filters, the band-widths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Fig. 4). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition) This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Fig. 6) to rise as the capacitor discharges.

Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponing 4-bit code (see Fig. 5) into the output latch. At this point the GT output is activated and drives v_c to VDD. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to

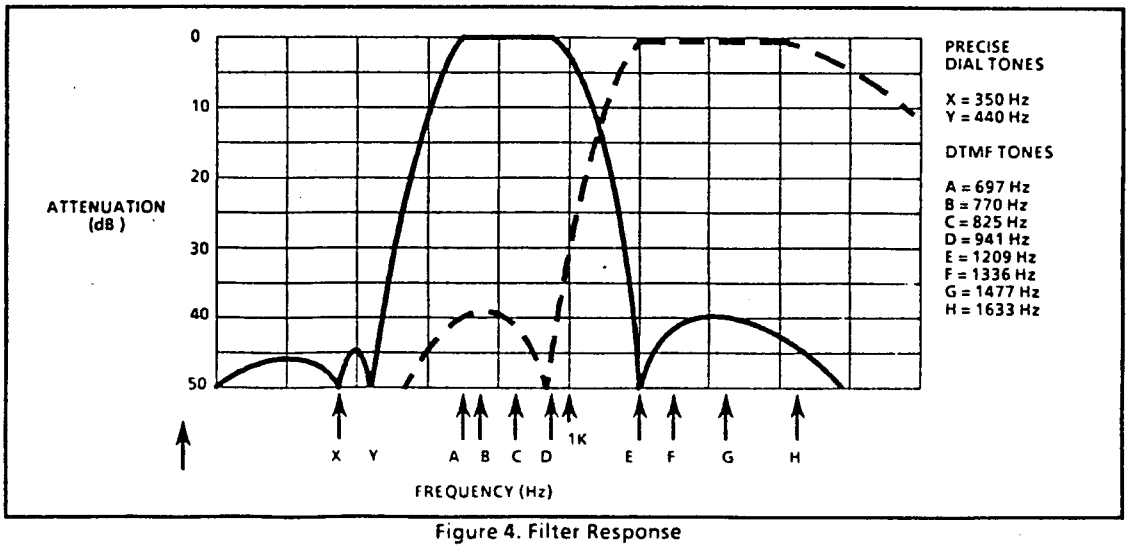


Figure 4. Filter Response

F_{LOW}	F_{HIGH}	NO	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	0	0	0	1
697	1336	2	H	0	0	1	0
697	1477	3	H	0	0	1	1
770	1209	4	H	0	1	0	0
770	1336	5	H	0	1	0	1
770	1477	6	H	0	1	1	0
852	1209	7	H	0	1	1	1
852	1336	8	H	1	0	0	0
852	1477	9	H	1	0	0	1
941	1336	0	H	1	0	1	0
941	1209	*	H	1	0	1	1
941	1477	#	H	1	1	0	0
697	1633	A	H	1	1	0	1
770	1633	B	H	1	1	1	0
852	1633	C	H	1	1	1	1
941	1633	D	H	0	0	0	0
-	-	ANY	L	Z	Z	Z	Z

L = LOGIC LOW, H = LOGIC HIGH, Z = HIGH IMEDANCE

Figure 5. Functional Decode Table

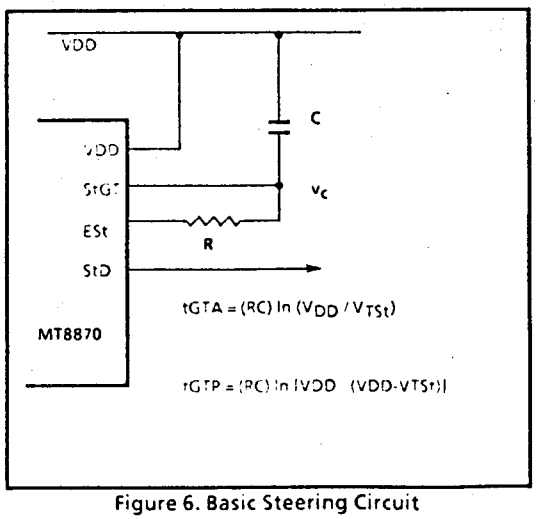


Figure 6. Basic Steering Circuit

validate the interdigit pause between signals. Thus, as well as rejecting signals too short too be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown in Fig. 6 is applicable. Component values are chosen according to the formula:

$$t_{REC} = t_{DP} + t_{GTP}$$
$$t_{ID} = t_{DA} + t_{GTA}$$

The value of t_{DP} is a device parameter (see table) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μF is recommended for most applications, leaving R to be selected by the designer.

Different steering arrangements may be used to select independantly the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast aquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 7.

Differential Input Configuration

The input arrangement of the MT8870 provides a differential-input operational amplifier as well as a bias source(V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Fig. 2 with the op-amp connected for unity gain and V_{Ref} biasing the input at $\frac{1}{2}V_{DD}$. Fig. 8 shows the differential configuration, which permits the

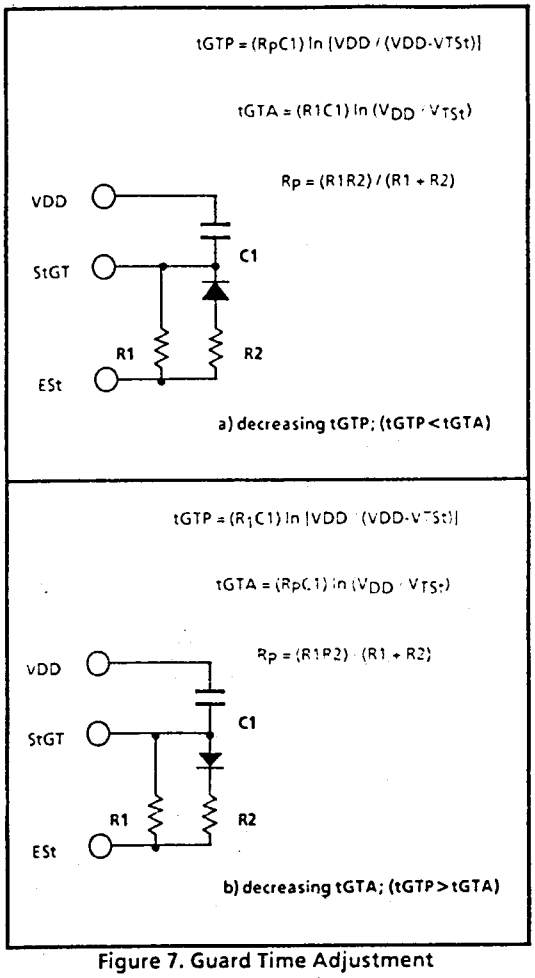


Figure 7. Guard Time Adjustment

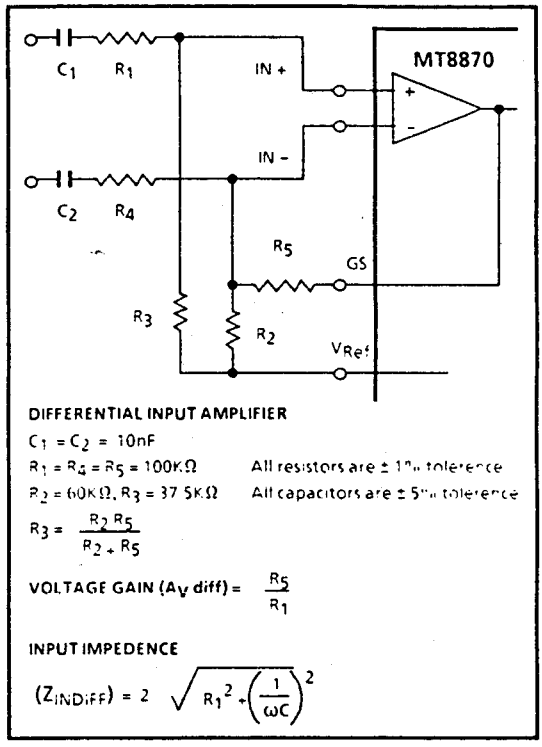


Figure 8. Differential Input Configuration

adjustment of gain with the feedback resistor R_5.

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.58 MHz crystal and is normally connected as shown in Figure 2 (Single Ended Input Configuration). However, it is possible to configure several MT8870 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Fig. 9 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, ie; precision balancing capacitors are not required.

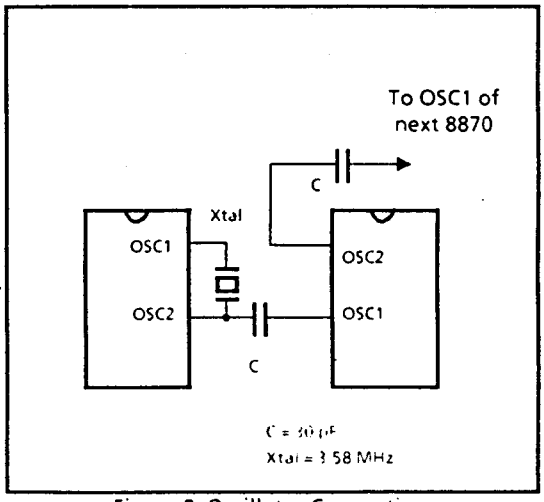


Figure 9. Oscillator Connection